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REGISTER MOVE OPERATIONSBACKGROUND

5 This invention relates to register move operations for
a computer.

Many conventional programmable processors, such as digital signal processors (DSP), include a variety of internal registers for use when processing data. One type of register, referred to as a data register, is primarily
10 used to store the results of a current operation and to supply the results to subsequent operations. The data registers are often grouped into a set of registers referred to as a register file.

A second type of register is a pointer register that
15 is typically used to store an address. Unlike the data stored by the data registers, which is often provided directly to an execution unit within the processor, the addresses stored by the pointer registers are primarily used to retrieve data from a memory system. A group of
20 pointer registers often includes a stack pointer, a frame pointer and a number of general-purpose pointer registers.

DESCRIPTION OF DRAWINGS

Figure 1 is a block diagram illustrating an example of a pipelined programmable processor according to the invention.

Figure 2 is a block diagram illustrating example pipelines for the programmable processor.

Figures 3 and 4 are flowcharts illustrating example implementations of register move instructions according to the invention.

10	DESCRIPTION
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Figure 1 is a block diagram illustrating a programmable processor 2 having one or more pipelines 4 and a control unit 6. Processor 2, as explained in detail below, supports machine instructions for moving data between a pointer register and a data register. In particular, processor 2 supports a machine instruction, referred to herein as the CC MOVE instruction, which moves data between a pointer register and a data register.

Pipelines 4 include a number of hardware pipelines
20 having a number of stages for processing instructions. The
stages may process concurrently with the other stages and
forward results to the next stage in accordance with a

clock cycle. The results of the instructions emerges at the end pipelines 4 in rapid succession.

Control unit 6 may control the flow of instructions and data through the various stages of pipelines 4. During the processing of an instruction, for example, control unit 6 may direct the various components of the pipelines to fetch and decode an instruction, perform the corresponding operation and write the results back to memory or local registers.

Figure 2 illustrates an example of a pipelined processor having a data address generation (DAG) pipeline 12, an execution unit (EU) pipeline 14 and a load/store (L/S) pipeline 16 arranged according to one embodiment of the invention. Each pipeline has, for example, five stages: instruction fetch (IF), decode (DEC), address calculation and data fetch (AC), execute (EX) and write back (WB).

Within DAG pipeline 12, instructions are fetched from memory, or from an instruction cache, during the IF stage by fetch unit 21 and decoded during the DEC stage. In addition, the DEC stage of DAG pipeline 12 may include a set of pointer registers 22 for storing memory addresses. At the next clock cycle, the decoded instructions, and any

pointer addresses used by the instruction, may be passed to the AC stage via DAG pipeline 12 to data address generator (DAG) 23. DAG 23 may calculate any additional memory addresses that are necessary to perform the operation.

5 These addresses may propagate down DAG pipeline 12 to be written back to a pointer register 22. Alternatively, the instructions may pass to EU pipeline 14 via path 15 for use by execution unit 25 or pass to L/S pipeline 16 via path 17 for loading data from memory 18. In one embodiment, DAG 23
10 may include circular buffer addressing registers used as pointer registers, such as index, base and length registers.

During the EX stage, execution unit 25 may perform the specified operation such as, for example, adding or
15 multiplying two numbers. Execution unit 25 may comprise specialized hardware for performing the operations including, for example, one or more arithmetic logic units (ALU's), floating-point units (FPU) and barrel shifters. Data registers 24 are located within the EX stage of
20 pipelines 4 and may directly supply execution unit 25 with locally stored data. In addition, data may be retrieved from data memory 18 based on a memory address generated by DAG 23, or based on an address stored in a pointer register

22, and propagated to the WB stage. During the WB stage, the results of the operation may be written to the destination. The WB stage has two paths for storing the results. Output 26 may be enabled when the results are written to data memory 18 or to data registers 24. Output 27 may be enabled when the results are written to pointer registers 22.

The CC MOVE instruction supported by processor 2 may allow software applications to move data directly between pointer registers 22 and data registers 24. Furthermore, the CC MOVE instruction may allow processors to move the data based on the state of condition flag (CC_FLAG) 29, which is typically set by a previous instruction, such as a compare instruction (CMP), other logical operations or operations that directly set the CC_FLAG 29. CC_FLAG 29 may be stored as a single bit within a storage circuit, such as a status register or flip-flop, and may be set when the CMP instruction, for example, exits the EX stage.

Figure 3 is a flowchart illustrating an example process 30 by which control unit 6 implements a CC MOVE machine instruction when the source register is a pointer register 22 and the destination register is a data register 24 according to one embodiment. Process 30 is explained

with reference to a move instruction that is conditioned upon CC_FLAG 29 being set; however, the move instruction may be conditioned upon CC_FLAG 29 being cleared, although the scope of the present invention is not limited in this respect.

Because CC_FLAG 29 is often set when the prior instruction exits the EX stage, pipelines 4 may partially process the CC MOVE instruction prior to the writing of CC_FLAG. More specifically, when the CC MOVE instruction is in the DEC stage, control unit 6 may speculate that move may occur and enable the output of pointer register 22 and pass the stored address to the AC stage upon the next clock cycle (31).

During the AC stage, control unit 6 may direct DAG 23 to forward the address to the EX stage without modification (32). Alternatively, for pointer registers within DAG 23 (not shown), control unit 6 may enable their output in the AC stage.

During the EX stage, the address may propagate to execution unit 25 via path 15. Control unit may direct execution unit 25 to forward the address to the WB stage without modification (33).

In the WB stage, control unit 6 may determine the state of CC_FLAG 29 within execution unit 25 and decide whether to enable or disable the write to the data registers 24 based on the state. If the CC_FLAG 29 is set, control unit 6 selects the appropriate data register 24 and writes the address via output 26 (34). In this manner, an address may be copied from a pointer register 22 to a data register 24 in response to a CC MOVE instruction. Notably, in order to move data from a pointer register 22 to a data register 24, the address may be propagated across pipelines 4. More specifically, the address may be propagated from a first pipeline, DAG pipeline 12, to a second pipeline, EU pipeline 14, where it may be written to data registers 24 if the condition flag is set. Because pipelines may be physically separated within a processor, there may be delays when propagating data from one pipeline to another. Therefore, the address propagates from the DAG pipeline 12 to the EU pipeline 14 prior to the WB stage in order to reduce the risk that the address is correctly written to data registers 24.

Figure 4 is a flowchart illustrating an example process 40 by which control unit 6 may implement a CC MOVE machine instruction when the source register is a data

register 24 and the destination register is a pointer register 28 according to one embodiment.

During the EX stage, control unit 6 may enable the output of the data register 24, allowing the stored data to propagate from EU pipeline 14 to DAG pipeline 12 via path 19 (41). During the WB stage, control unit 6 may determine the state of CC_FLAG 29 within execution unit 25 of EU pipeline 14 (42). Based on the state of CC_FLAG, control unit 6 may write the data to the appropriate pointer register 22 via output 27 (43). As discussed above, the data may propagate from EU pipeline 14 to DAG pipeline 12 prior to the WB stage in order to allow the address to be written to pointer registers 22. In one embodiment EX stage may include three substages, to provide the data at the WB stage.

The following examples illustrate the syntax for invoking the CC MOVE machine instruction although the scope of the present invention is not limited in this respect:

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if CC p1=r1; Move from data register to pointer register
if !CC r0=p1; Move from pointer register to data register when CC
is false
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In a typical application, a programmer develops a software application or subroutine that may invoke a

register move operation involving both a pointer register and a data register, such as the CC MOVE instruction described above. The programmer may write the software application in assembly language, as illustrated in the example above, or in a high-level software language. A compiler is typically invoked to process the high-level software application and generate the appropriate machine instructions for processor 2, including the CC MOVE machine instruction for conditionally moving data between a pointer register and a data register.

Various embodiments of the invention have been described. For example, a single machine instruction has been described that conditionally moves data between a pointer register and a data register. The processor may be implemented in a variety of systems including general purpose computing systems, digital processing systems, laptop computers, personal digital assistants (PDA's) and cellular phones. In such a system, the processor may be coupled to a memory device, such as a FLASH memory device or a static random access memory (SRAM), that stores an operating system and other software applications. These and other embodiments are within the scope of the following claims.

What is claimed is:

- 1 1. A method comprising:
2 receiving a machine instruction; and
3 in response to the machine instruction, moving data
4 between a pointer register and a data register based on a
5 state of a condition flag.
- 1 2. The method of claim 1, wherein moving the data
2 includes copying a memory address from the pointer register
3 to the data register.
- 1 3. The method of claim 1, wherein moving the data
2 includes copying the data from the data register to the
3 pointer register.
- 1 4. The method of claim 1, wherein the pointer register
2 and the data register are located within different stages
3 of different pipelined units of a processor.
- 1 5. The method of claim 1 further including selecting a
2 first path when the pointer register is a source for the
3 data and selecting a second path when the data register is
4 the source for the data.

1 6. The method of claim 1 further including propagating
2 the data through an execution unit without modification.

1 7. A method comprising:

2 receiving a machine instruction;

3 enabling an output of a pointer register designated by
4 the machine instruction, wherein the pointer register is
5 adapted to store a memory address;

6 propagating the memory address through an execution
7 unit without modification;

8 determining a state of a condition flag; and

9 writing the memory address to a data register based on
10 the state.

1 8. The method of claim 7, further including propagating
2 the address from a first pipeline to a second pipeline.

1 9. The method of claim 7, further including setting the
2 condition flag during the execution of a previous
3 instruction.

1 10. A method for moving data in a processor having a
2 plurality of pipelines comprising:
3 enabling an output of a data register in first
4 pipeline;
5 propagating data from the data register to a second
6 pipeline prior to a write back stage of the first pipeline;
7 and
8 writing the data to a pointer register located within
9 the second pipeline.

1 11. The method of claim 10 further including:
2 determining a state of a condition flag; and
3 writing the data to the pointer register based on the
4 state.

1 12. The method of claim 10, wherein the pointer register
2 and data register occupy different stages of the first and
3 second pipelines.

1 13. A method for moving data in a processor having a
2 plurality of pipelines, each pipeline having a write back
3 stage, the method comprising:

4 enabling an output of a pointer register in first
5 pipeline;
6 propagating an address from the first pipeline to a
7 second pipeline prior to a write back stage of the first
8 pipeline; and
9 writing the address to a data register located within
10 the second pipeline.

1 14. The method of claim 13 further including:
2 determining the state of a condition flag; and
3 writing the data to the pointer register based on the
4 state.

1 15. The method of claim 13, wherein the pointer register
2 and the data register occupy different stages of the first
3 and second pipelines.

1 16. The method of claim 13, wherein the pointer register
2 is located in a stage prior to the data register.

1 17. An apparatus comprising:
2 a pointer register;
3 a data register; and

1 a control unit adapted to conditionally move data
2 between the data register and pointer register in response
3 to a single machine instruction.

1 18. The apparatus of claim 17, wherein the pointer
2 register is located in a first pipeline and the data
3 register is located in a second pipeline.

1 19. The apparatus of claim 18, wherein the first and
2 second pipeline have a plurality of stages, and further
3 wherein the pointer register and data register are located
4 in different stages of the respective pipeline.

1 20. The apparatus of claim 18 further comprising a path
2 coupling the first and second pipelines to communicate an
3 address from the pointer register of the first pipeline to
4 the data register of the second pipeline.

1 21. The apparatus of claim 18 further comprising a path
2 coupling the first and second pipelines to communicate data
3 from the data register of the second pipeline to the
4 address register of the first pipeline.

1 22. The apparatus of claim 20, wherein each pipeline
2 includes a write back stage, and further wherein the path
3 communicates the address to the second pipeline prior to
4 the write back stage.

1 23. The apparatus of claim 21, wherein each pipeline
2 includes a write back stage, and further wherein the path
3 communicates the data to the first pipeline prior to the
4 write back stage.

1 24. The apparatus of claim 17 further including an
2 execution unit adapted to propagate the data from the
3 pointer register to the write back stage without
4 modification.

1 25. An article comprising a medium having computer-
2 executable instructions stored thereon for compiling a
3 software program, wherein the computer-executable
4 instructions are adapted to generate a single machine
5 instruction to cause a programmable processor to
6 conditionally move data between a pointer register and a
7 data register, wherein the instruction causes the

1 programmable processor to forward the data from a first
2 pipeline to a second pipeline.

1 26. The article of claim 25, wherein the instruction
2 causes the programmable processor to move the data from the
3 data register to the pointer register.

1 27. The article of claim 25, wherein the processor
2 comprises a pipeline and the machine instruction causes the
3 processor to select a first path through the pipeline when
4 the pointer register is a source for the data and a second
5 path through the pipeline when the data register is a
6 source for the data.

1 28. A system comprising:
2 a memory device; and
3 a processor coupled to the memory device, wherein the
4 processor includes a pointer register, a data register, and
5 a control unit adapted to conditionally move data between
6 the data register and pointer register in response to a
7 single machine instruction.

1 29. The system of claim 28, wherein the pointer register
2 is located in a first pipeline and the data register is
3 located in a second pipeline.

1 30. The system of claim 29, wherein the first and second
2 pipeline have a plurality of stages, and further wherein
3 the pointer register and data register are located in
4 different stages of the respective pipeline.

1 31. The system of claim 29 further comprising a path
2 coupling the first and second pipelines to communicate an
3 address from the pointer register of the first pipeline to
4 the data register of the second pipeline.

1 32. The system of claim 29 further comprising a path
2 coupling the first and second pipelines to communicate data
3 from the data register of the second pipeline to the
4 address register of the first pipeline.

1 33. The system of claim 31, wherein each pipeline includes
2 a write back stage, and further wherein the path
3 communicates the address to the second pipeline prior to
4 the write back stage.

1 34. The system of claim 32, wherein each pipeline includes
2 a write back stage, and further wherein the path
3 communicates the data to the first pipeline prior to the
4 write back stage.

1 35. The system of claim 28 further including an execution
2 unit adapted to propagate the data from the pointer
3 register to the write back stage without modification.

1 36. The system of claim 28, wherein the memory device
2 comprises static random access memory.

1 37. The system of claim 28, wherein the memory device
2 comprises FLASH memory.