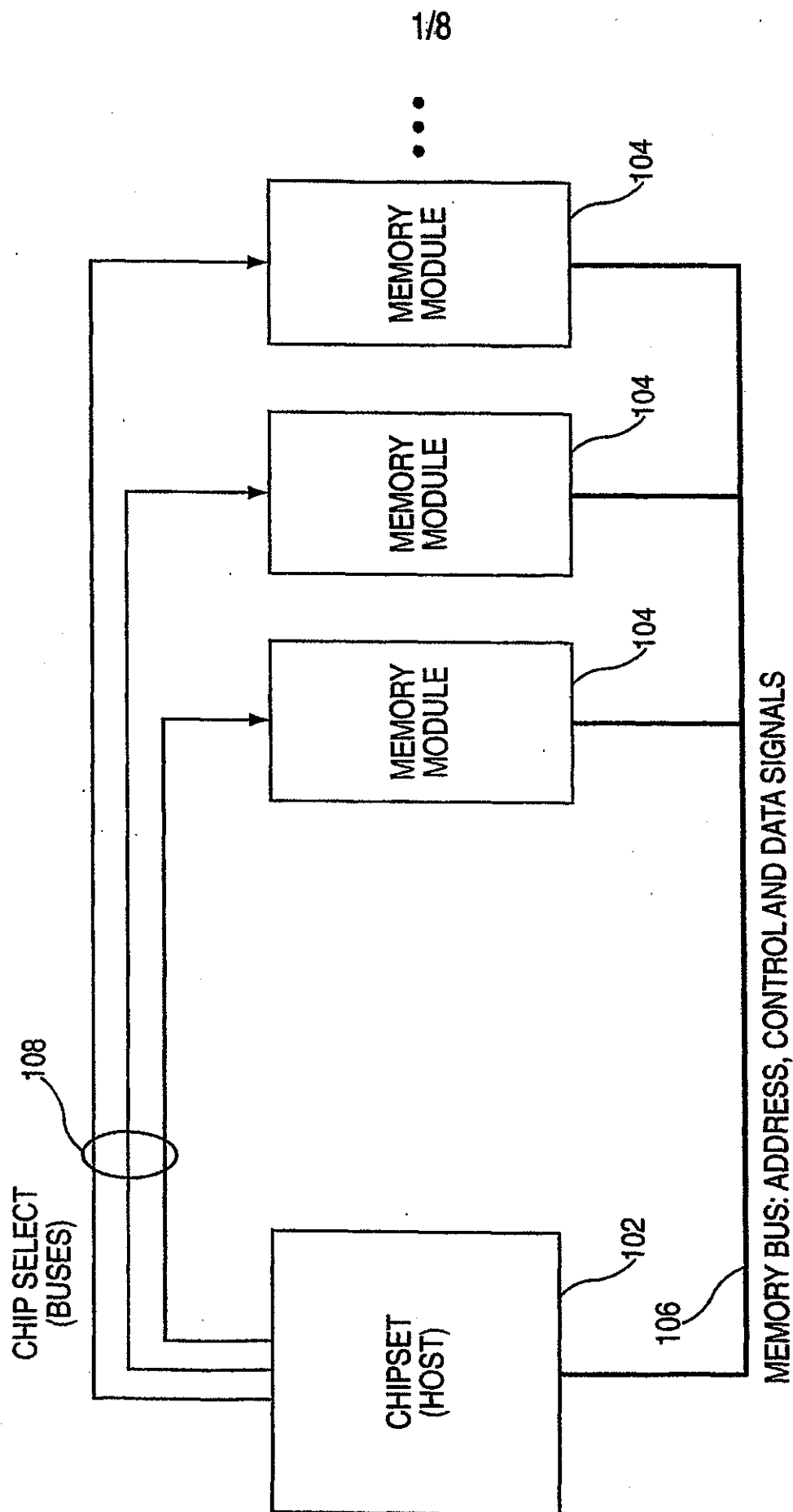




MEMORY BUS

FIG. 1
PRIOR ART

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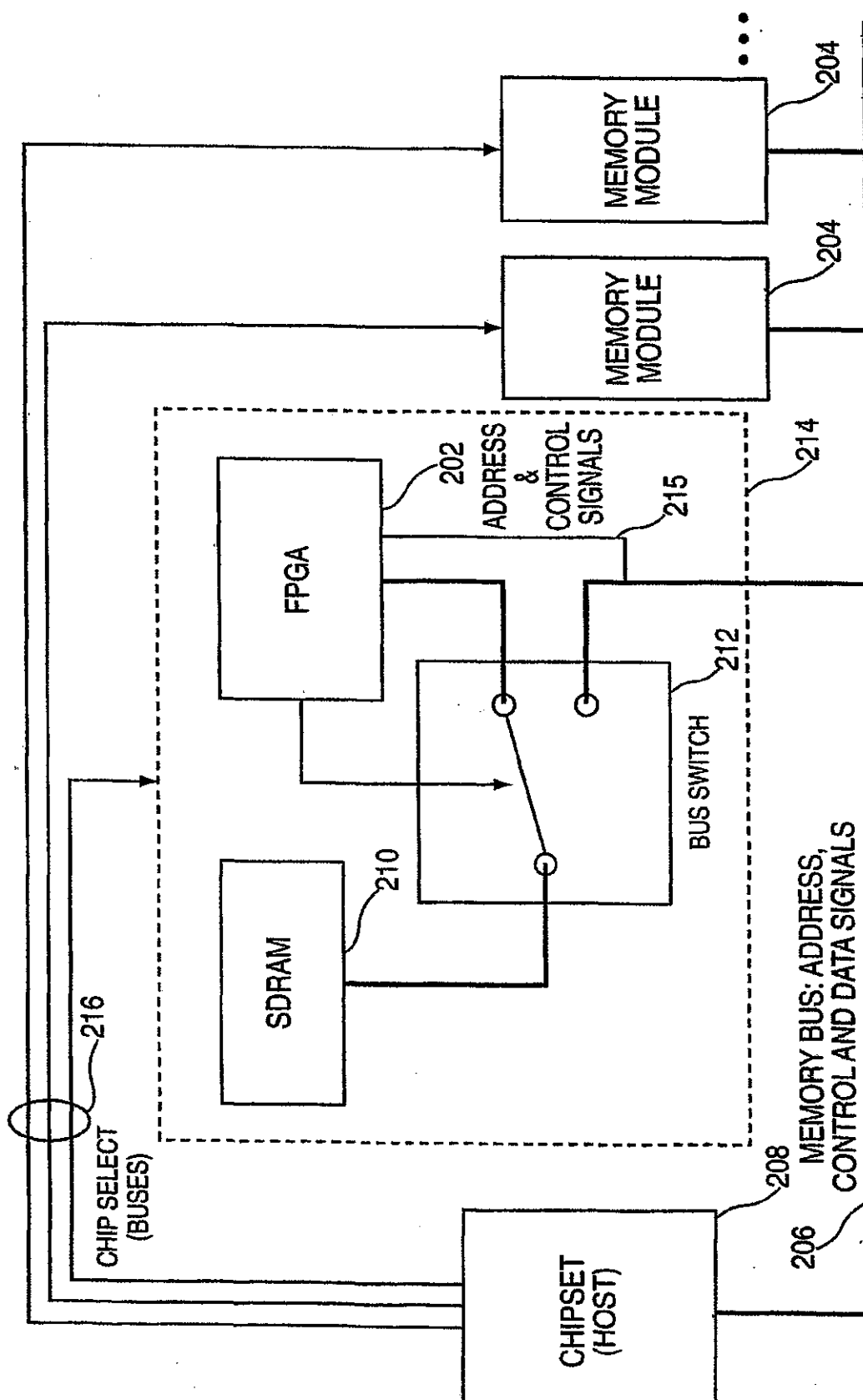
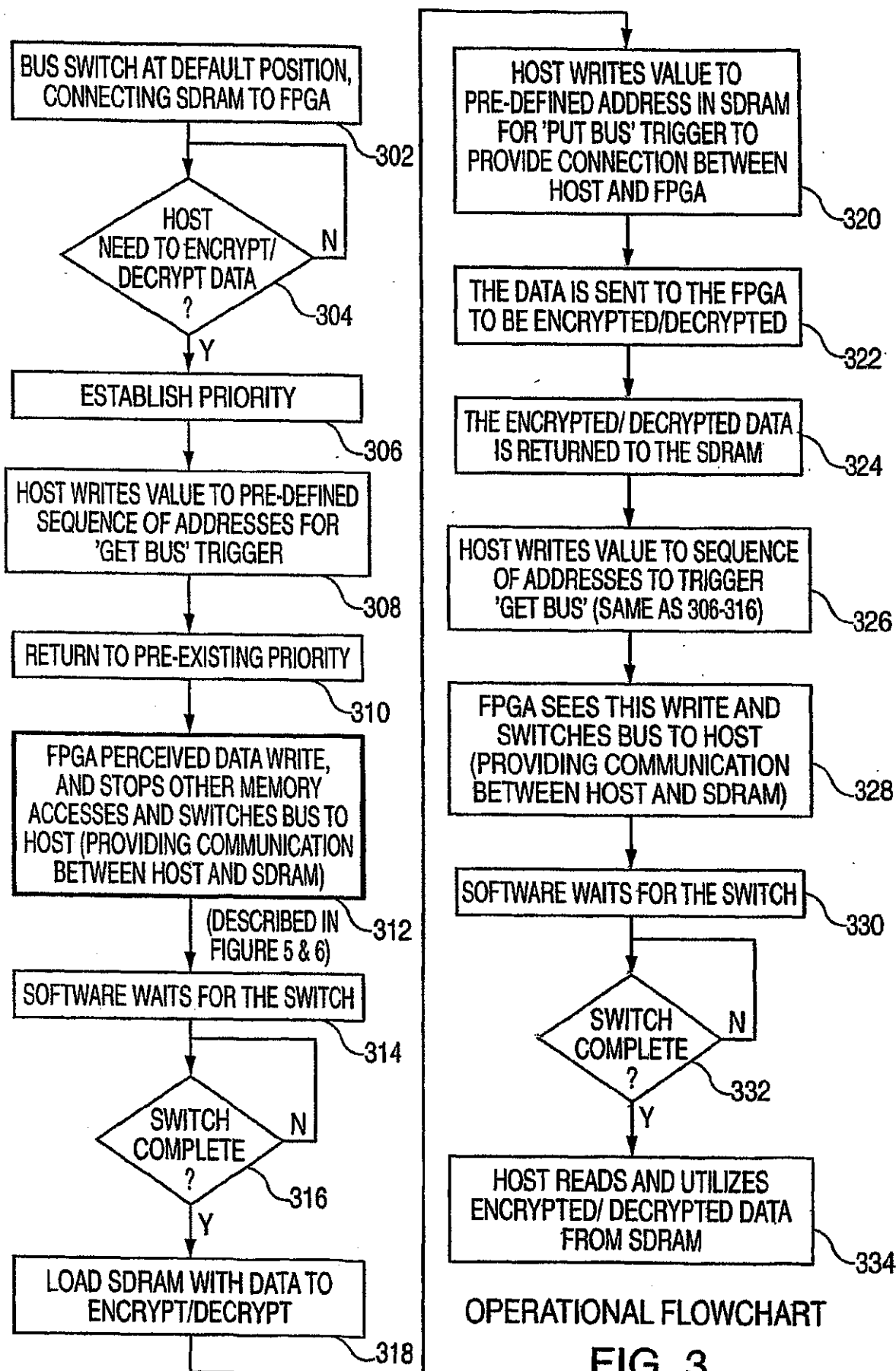


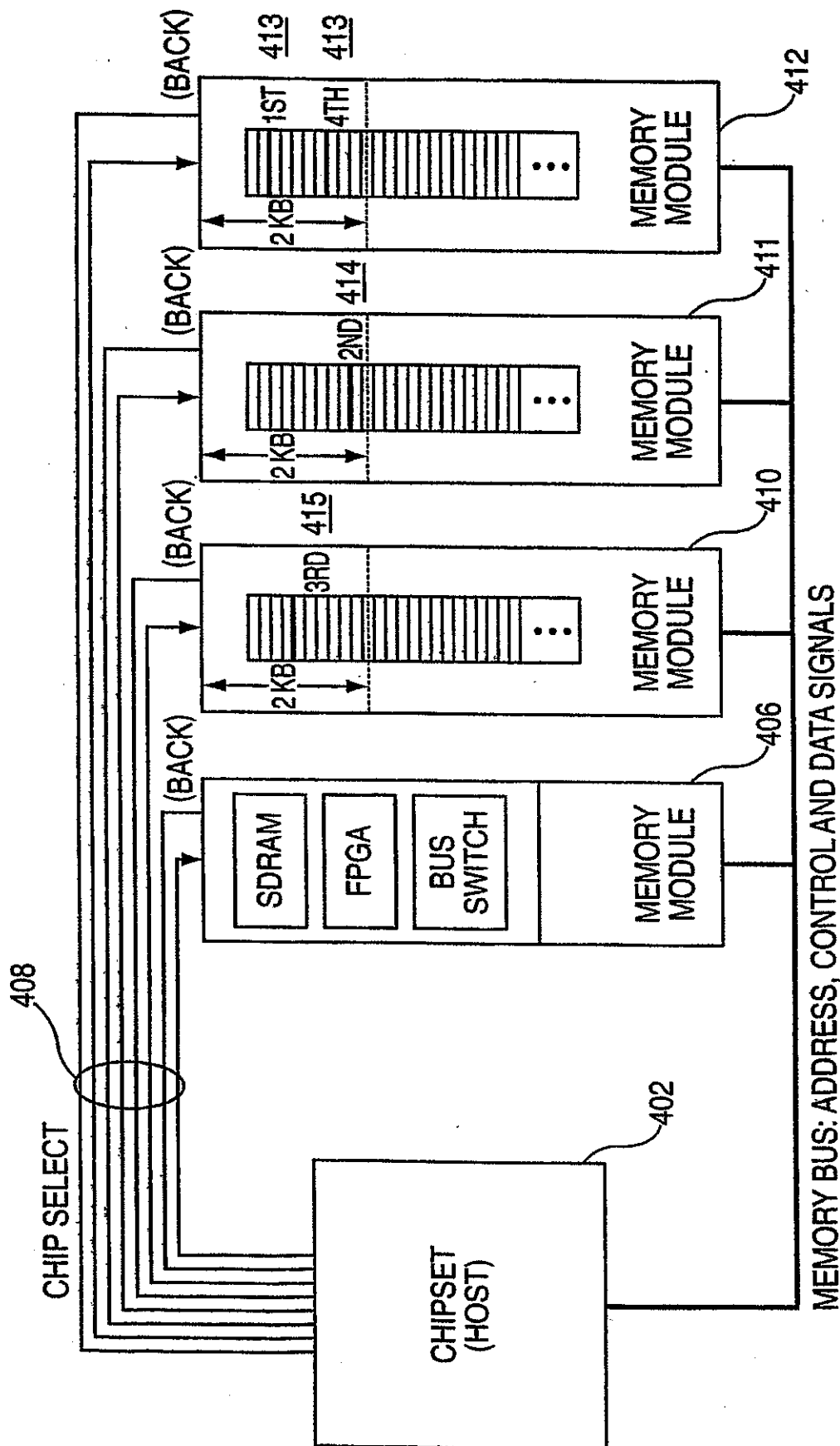
FIG. 2

MEMORY BUS PERIPHERAL (FPGA) OPERATION

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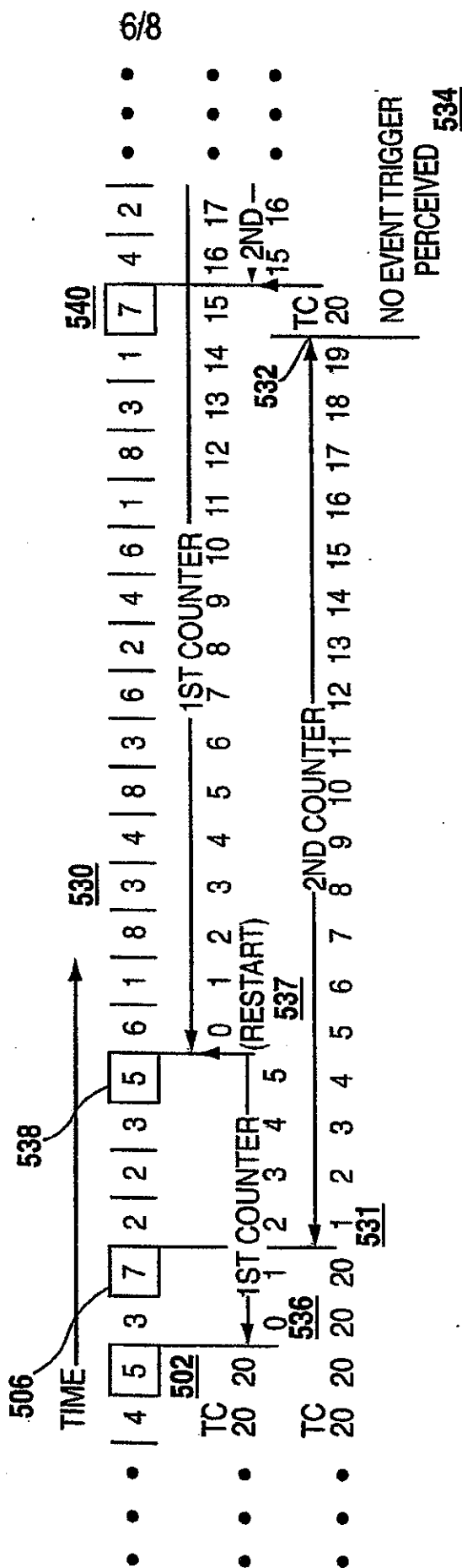
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EXAMPLE MEMORY MODULE TRIGGER ADDRESS LOCATIONS

FIG. 4

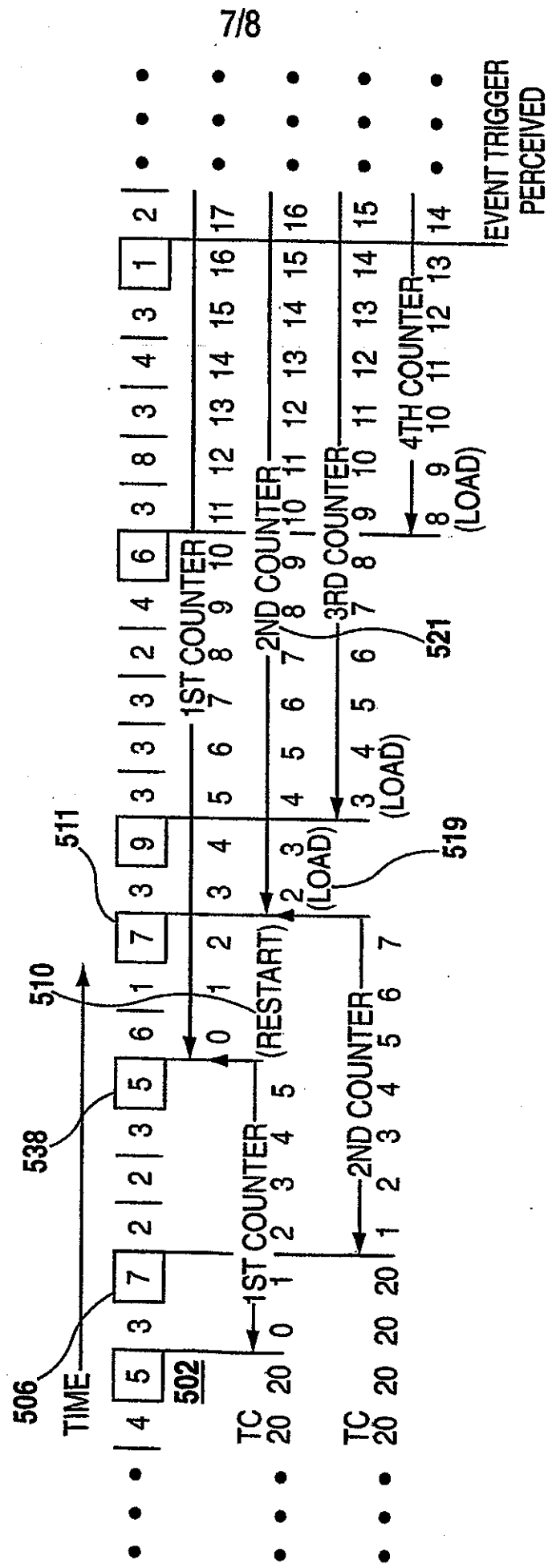
DATA VALUES WITNESSED OVER TIME: ...45372235618348362461831742...
 COMMAND SEQUENCE: 57961
 N=19, K=5



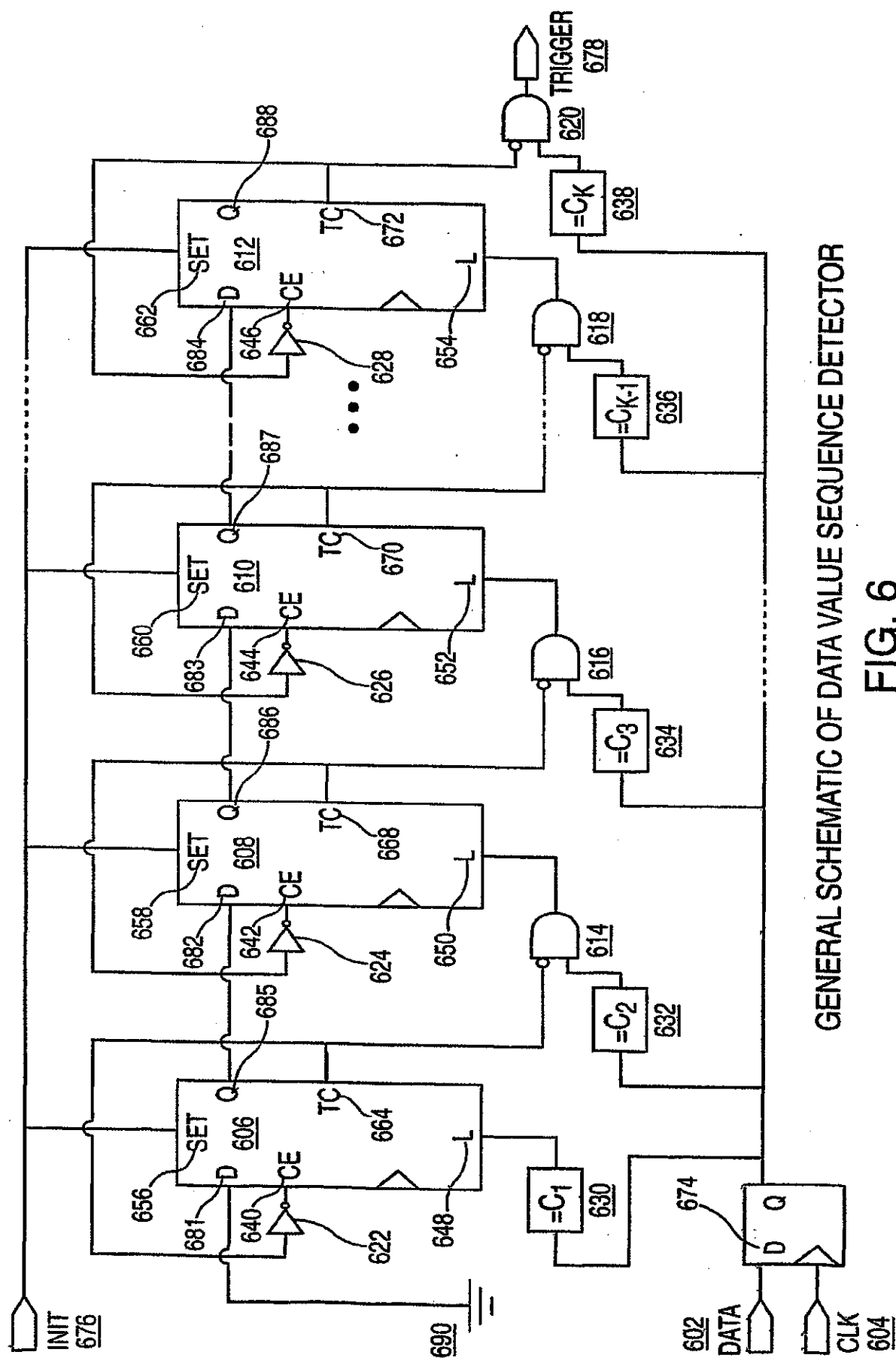
TIME CHART DESCRIPTIVE OF SEQUENCE DETECTION (EVENT NOT TRIGGERED)

FIG. 5b

DATA VALUES WITNESSED OVER TIME: ...45372235617393332463834312...
 COMMAND SEQUENCE: 57961
 N=19, K=5



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GENERAL SCHEMATIC OF DATA VALUE SEQUENCE DETECTOR
FIG. 6