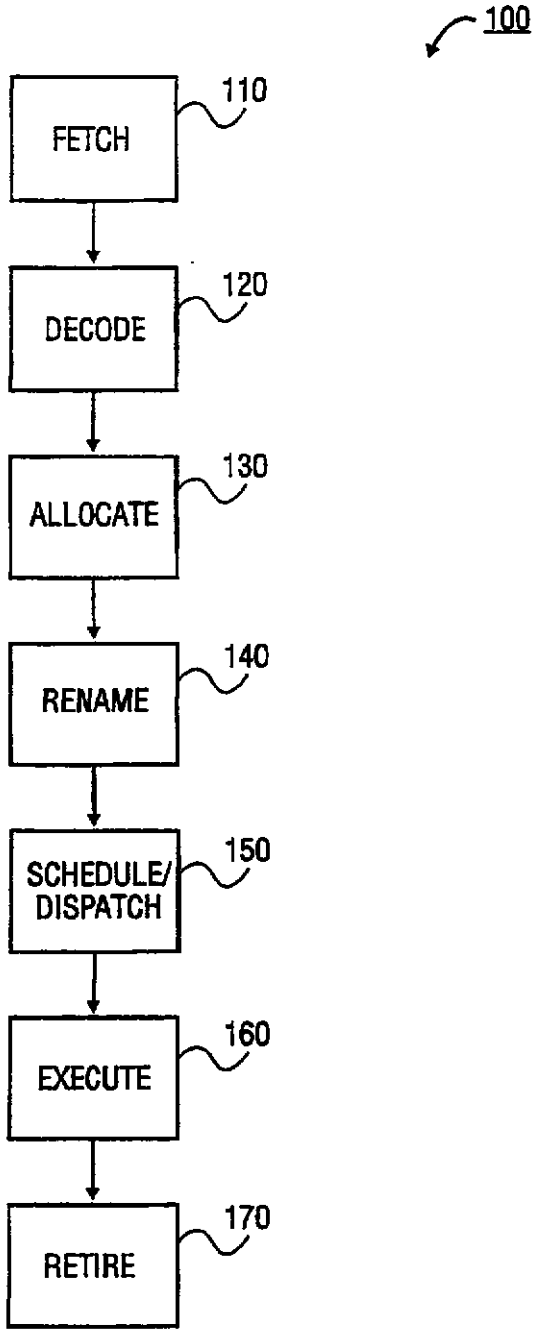

100
FETCH
110
DECODE
120
ALLOCATE
130
RENAME
140
SCHEDULE/
DISPATCH
150
EXECUTE
160
RETIRE
170

FIG. 1

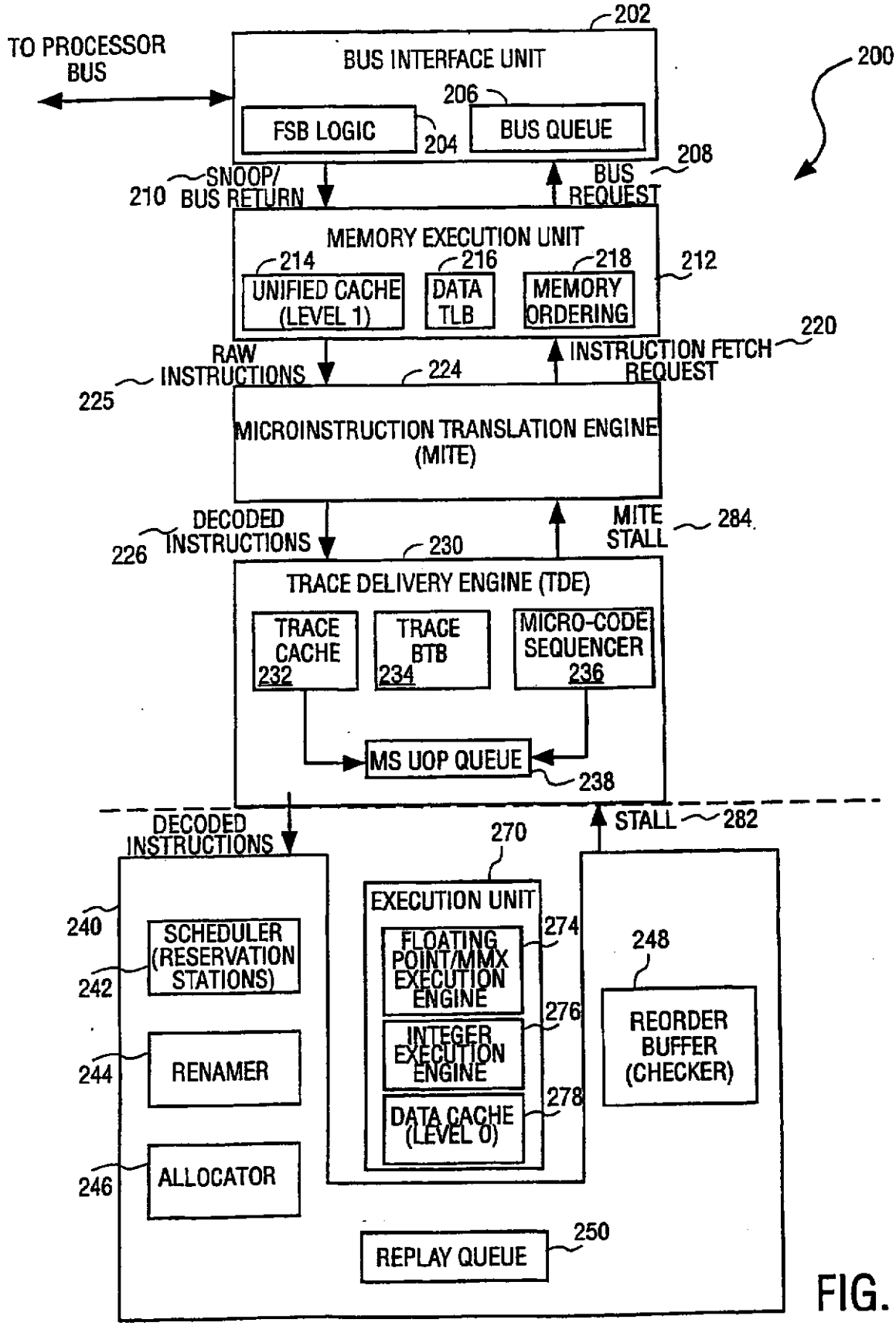

TO PROCESSOR BUS
202
BUS INTERFACE UNIT
206
FSB LOGIC
204
BUS QUEUE
200
208
210 SNOOP/ BUS RETURN
BUS REQUEST
MEMORY EXECUTION UNIT
214
UNIFIED CACHE (LEVEL 1)
216
DATA TLB
218
MEMORY ORDERING
212
220
RAW INSTRUCTIONS
224
INSTRUCTION FETCH REQUEST
225
MICROINSTRUCTION TRANSLATION ENGINE (MITE)
DECODED INSTRUCTIONS
226
230
MITE STALL
284
TRACE DELIVERY ENGINE (TDE)
TRACE CACHE 232
TRACE BTB 234
MICRO-CODE SEQUENCER 236
MS UOP QUEUE
238
DECODED INSTRUCTIONS
STALL
282
270
EXECUTION UNIT
240
SCHEDULER (RESERVATION STATIONS)
242
FLOATING POINT/MMX EXECUTION ENGINE
274
248
244
RENAMER
INTEGER EXECUTION ENGINE
276
REORDER BUFFER (CHECKER)
DATA CACHE (LEVEL 0)
278
246
ALLOCATOR
REPLAY QUEUE
250

FIG. 2

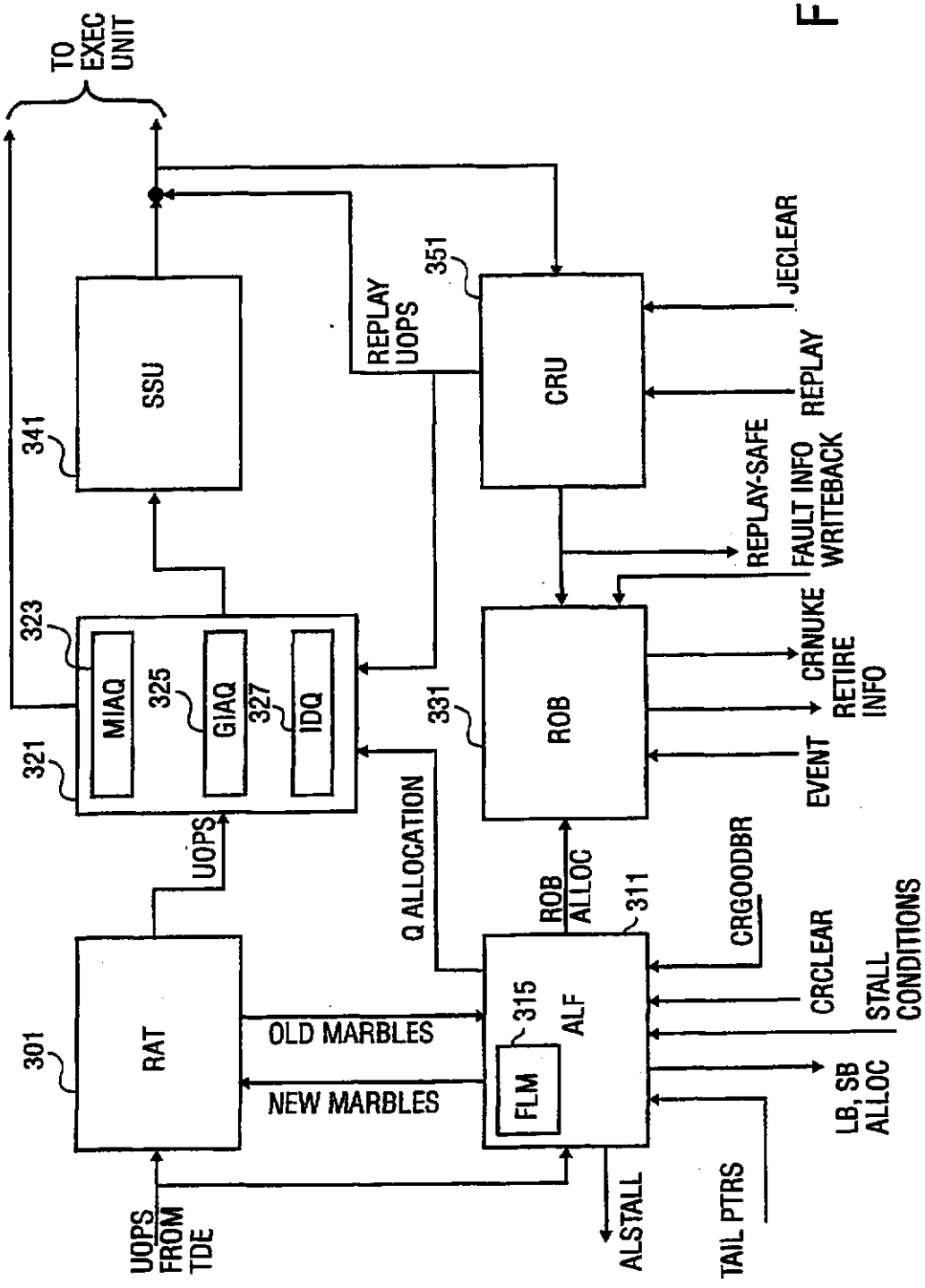

TO EXEC UNIT
SSU
341
REPLAY UOPS
351
CRU
JECLEAR
REPLAY
REPLAY-SAFE
FAULT INFO WRITEBACK
323
MIAQ
325
GIAQ
327
IDQ
321
ROB
331
CRNUKE
RETIRE INFO
EVENT
UOPS
Q ALLOCATION
ROB ALLOC
311
CRGOODBR
CRCLEAR
STALL CONDITIONS
301
RAT
OLD MARBLES
NEW MARBLES
315
ALF
FLM
LB, SB ALLOC
UOPS FROM TDE
ALSTALL
TAIL PTRS

FIG. 3

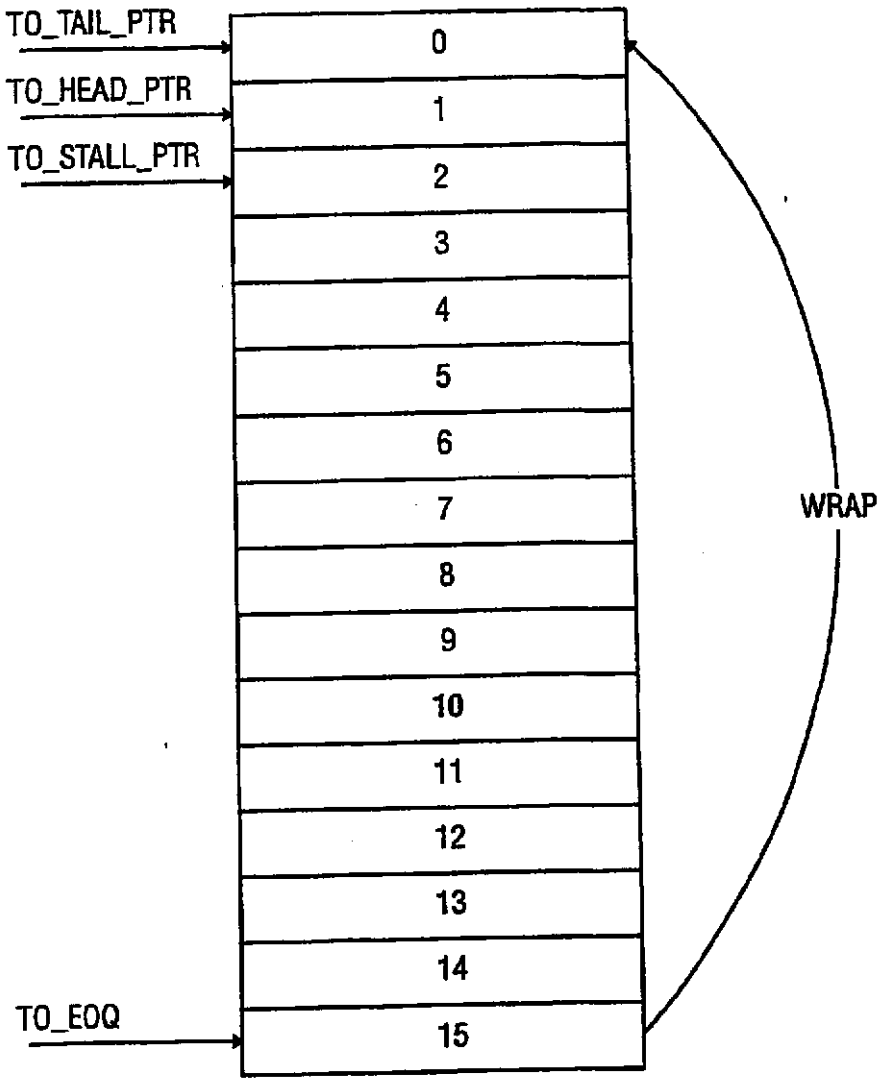

TO_TAIL_PTR
TO_HEAD_PTR
TO_STALL_PTR
TO_EOQ
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
WRAP

FIG. 4A

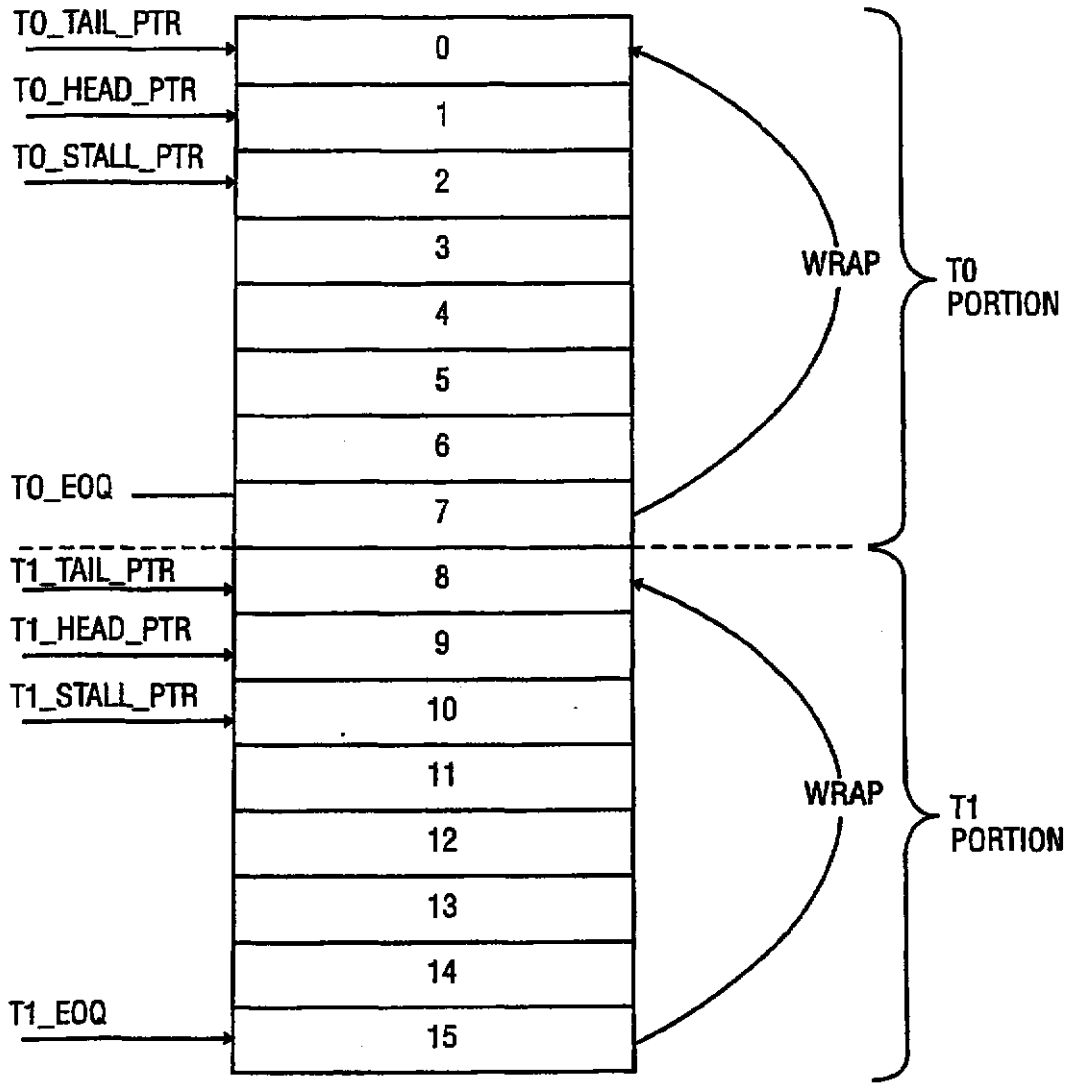

T0_TAIL_PTR
T0_HEAD_PTR
T0_STALL_PTR
T0_EOQ
T1_TAIL_PTR
T1_HEAD_PTR
T1_STALL_PTR
T1_EOQ
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
WRAP
T0 PORTION
WRAP
T1 PORTION

FIG. 4B

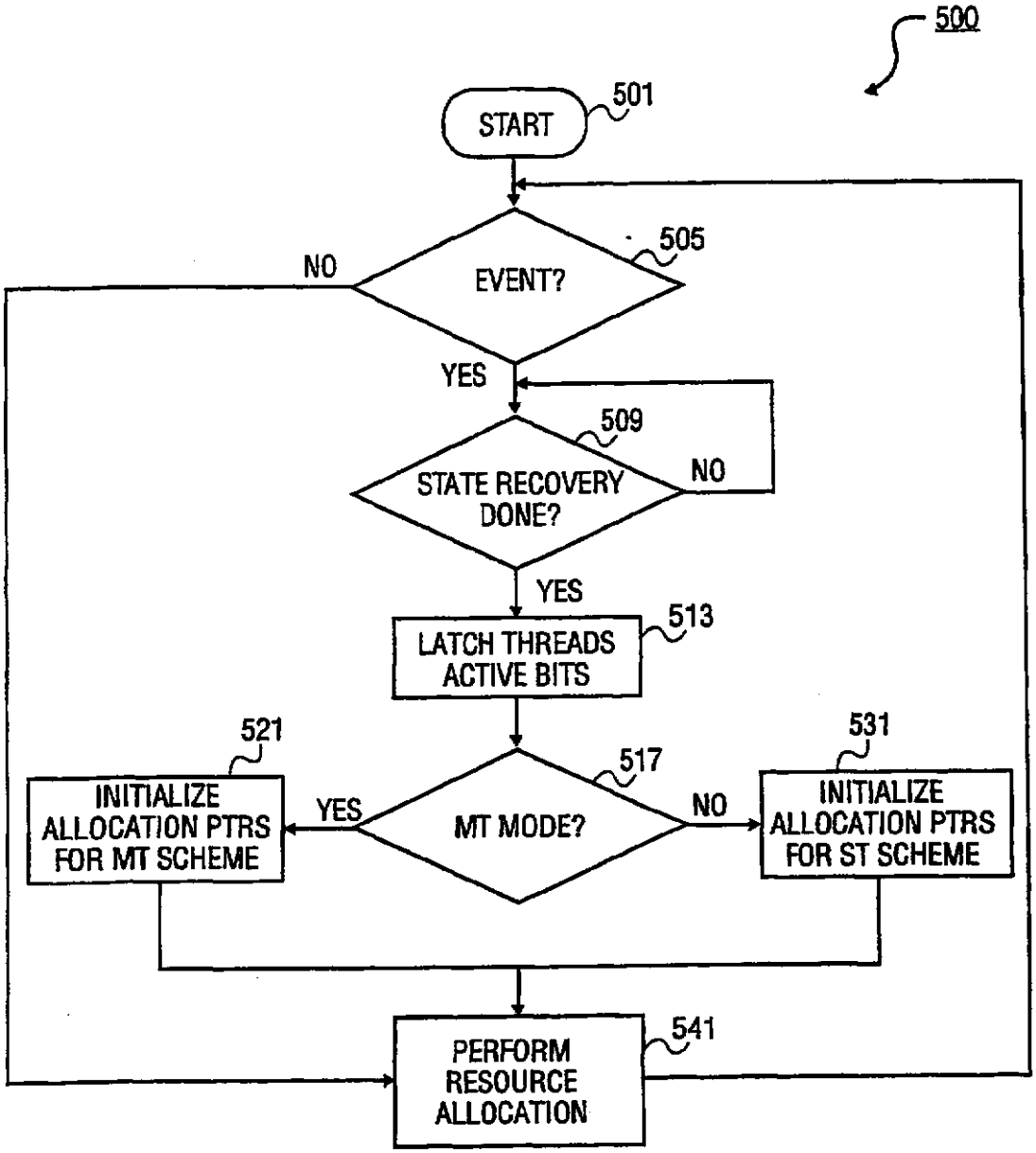

500
START
501
EVENT?
505
NO
YES
STATE RECOVERY DONE?
509
NO
YES
LATCH THREADS ACTIVE BITS
513
MT MODE?
517
YES
NO
INITIALIZE ALLOCATION PTRS FOR MT SCHEME
521
INITIALIZE ALLOCATION PTRS FOR ST SCHEME
531
PERFORM RESOURCE ALLOCATION
541

FIG. 5

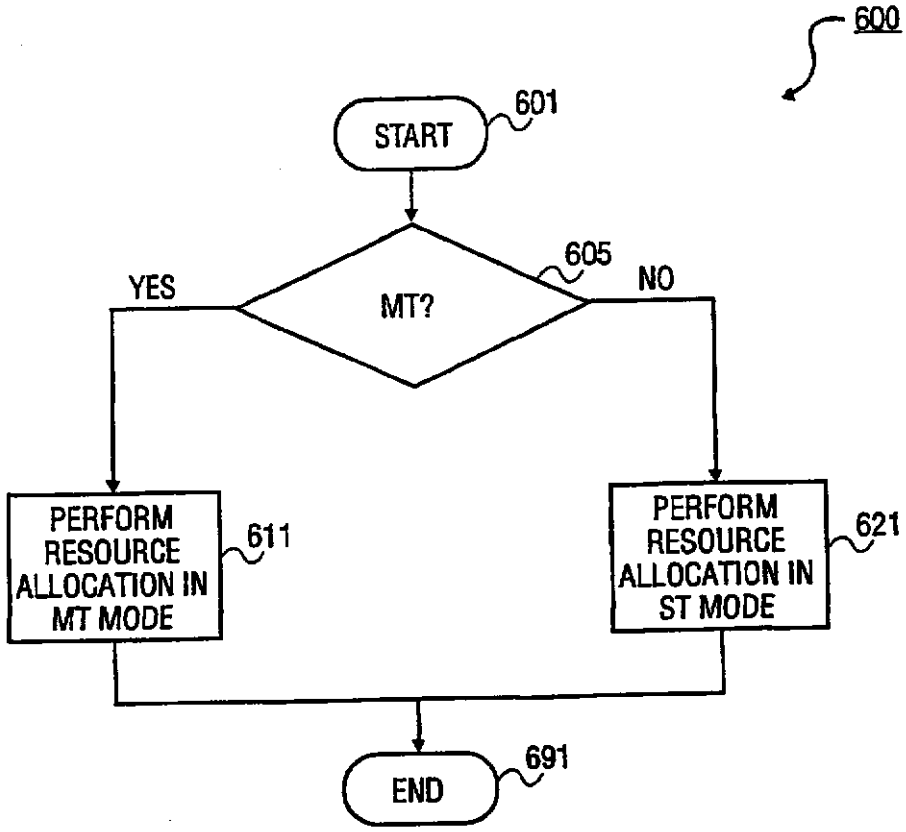

600
START
601
MT?
605
YES
NO
PERFORM RESOURCE ALLOCATION IN MT MODE
611
PERFORM RESOURCE ALLOCATION IN ST MODE
621
END
691

FIG. 6

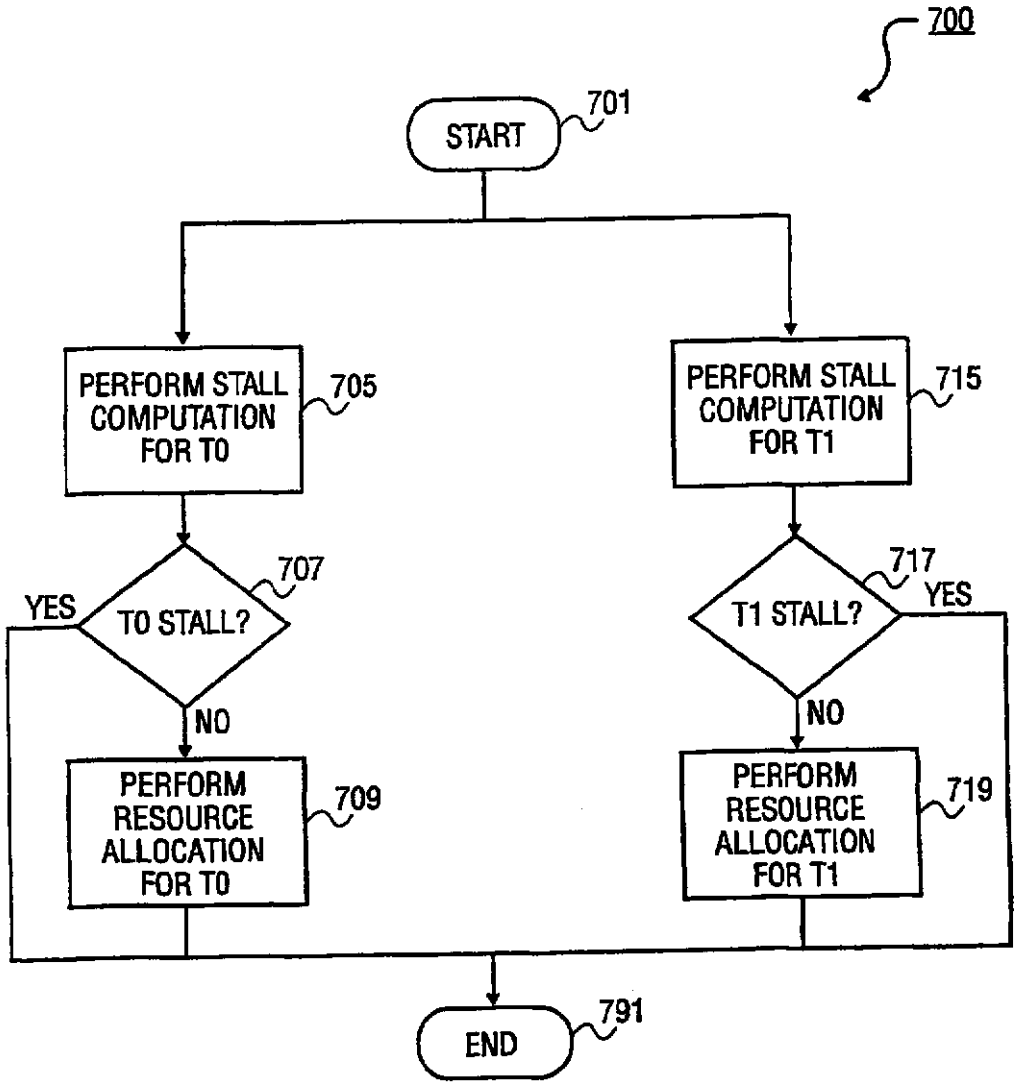

700
START
701
PERFORM STALL COMPUTATION FOR T0
705
PERFORM STALL COMPUTATION FOR T1
715
T0 STALL?
707
YES
NO
T1 STALL?
717
YES
NO
PERFORM RESOURCE ALLOCATION FOR T0
709
PERFORM RESOURCE ALLOCATION FOR T1
719
END
791

FIG. 7

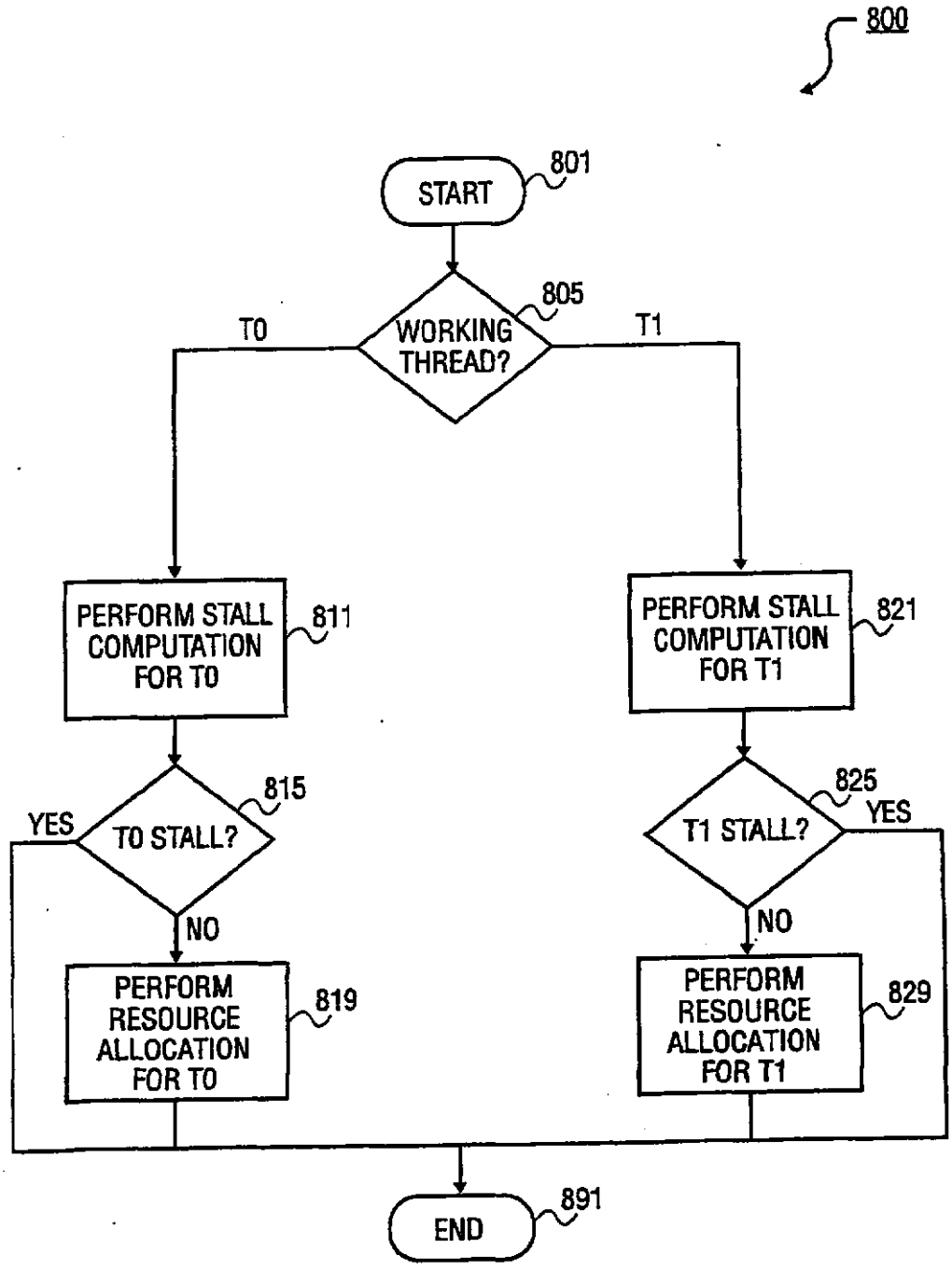

800
START
801
WORKING THREAD?
805
T0
T1
PERFORM STALL COMPUTATION FOR T0
811
PERFORM STALL COMPUTATION FOR T1
821
T0 STALL?
815
YES
NO
T1 STALL?
825
YES
NO
PERFORM RESOURCE ALLOCATION FOR T0
819
PERFORM RESOURCE ALLOCATION FOR T1
829
END
891

FIG. 8

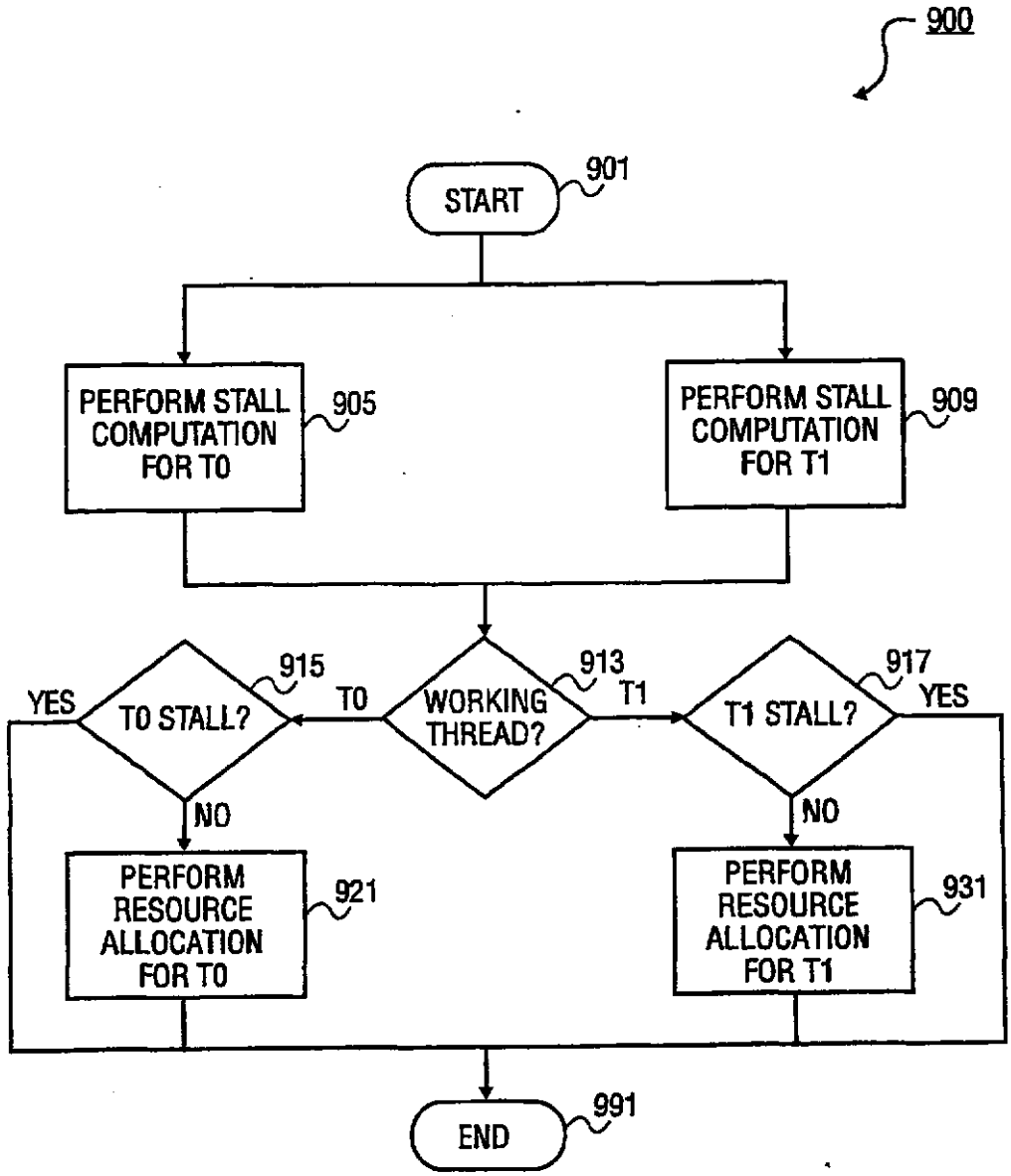

900
START
901
PERFORM STALL COMPUTATION FOR T0
905
PERFORM STALL COMPUTATION FOR T1
909
WORKING THREAD?
913
T0
T1
T0 STALL?
915
YES
NO
T1 STALL?
917
YES
NO
PERFORM RESOURCE ALLOCATION FOR T0
921
PERFORM RESOURCE ALLOCATION FOR T1
931
END
991

FIG. 9

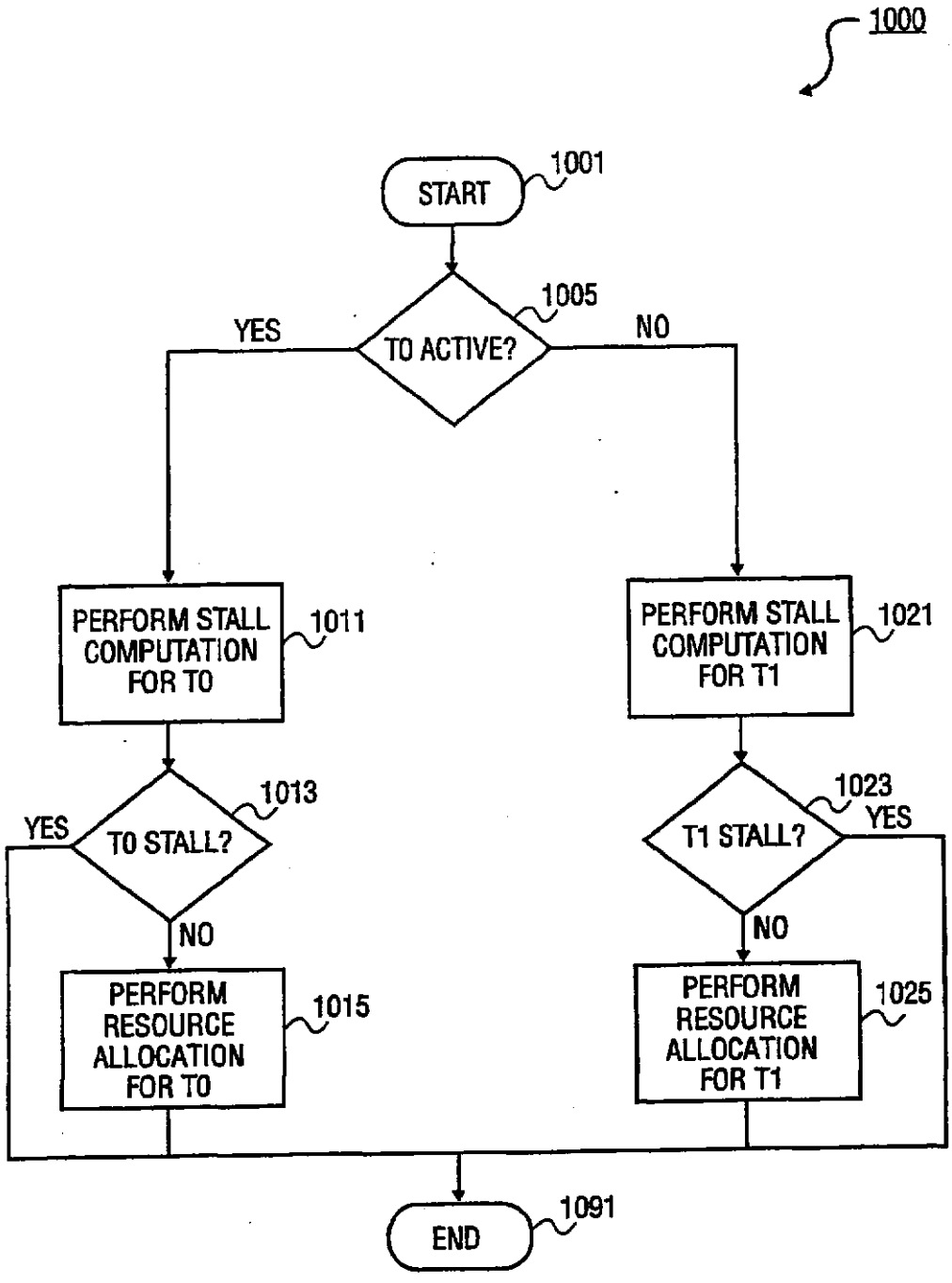

1000
START
1001
TO ACTIVE?
1005
YES
NO
PERFORM STALL COMPUTATION FOR T0
1011
PERFORM STALL COMPUTATION FOR T1
1021
T0 STALL?
1013
YES
NO
T1 STALL?
1023
YES
NO
PERFORM RESOURCE ALLOCATION FOR T0
1015
PERFORM RESOURCE ALLOCATION FOR T1
1025
END
1091

FIG. 10

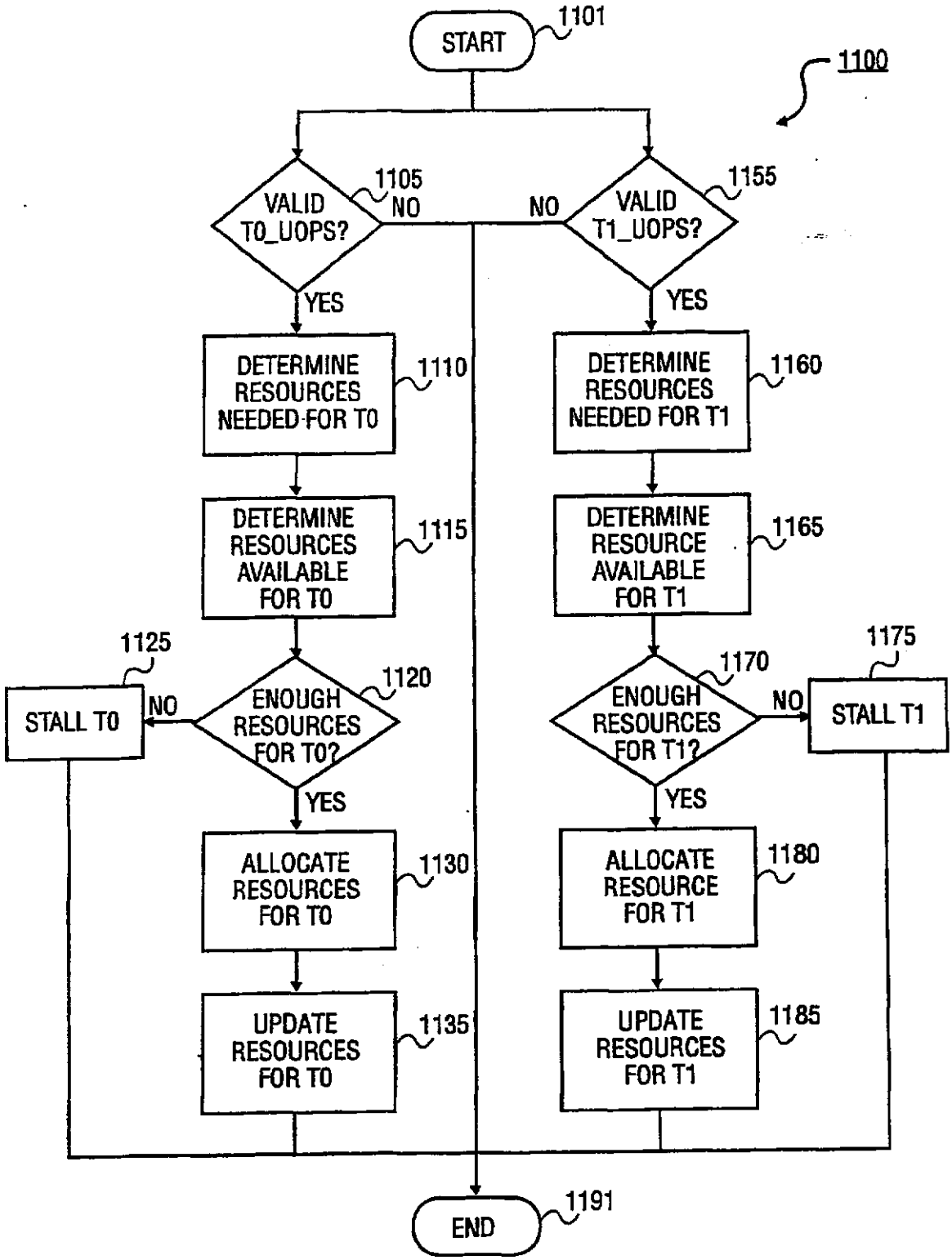

START
1101
1100
VALID T0_UOPS?
1105
NO
NO
VALID T1_UOPS?
1155
YES
YES
DETERMINE RESOURCES NEEDED FOR T0
1110
DETERMINE RESOURCES NEEDED FOR T1
1160
DETERMINE RESOURCES AVAILABLE FOR T0
1115
DETERMINE RESOURCE AVAILABLE FOR T1
1165
1125
STALL T0
NO
ENOUGH RESOURCES FOR T0?
1120
1170
ENOUGH RESOURCES FOR T1?
NO
1175
STALL T1
YES
YES
ALLOCATE RESOURCES FOR T0
1130
ALLOCATE RESOURCE FOR T1
1180
UPDATE RESOURCES FOR T0
1135
UPDATE RESOURCES FOR T1
1185
END
1191

FIG. 11

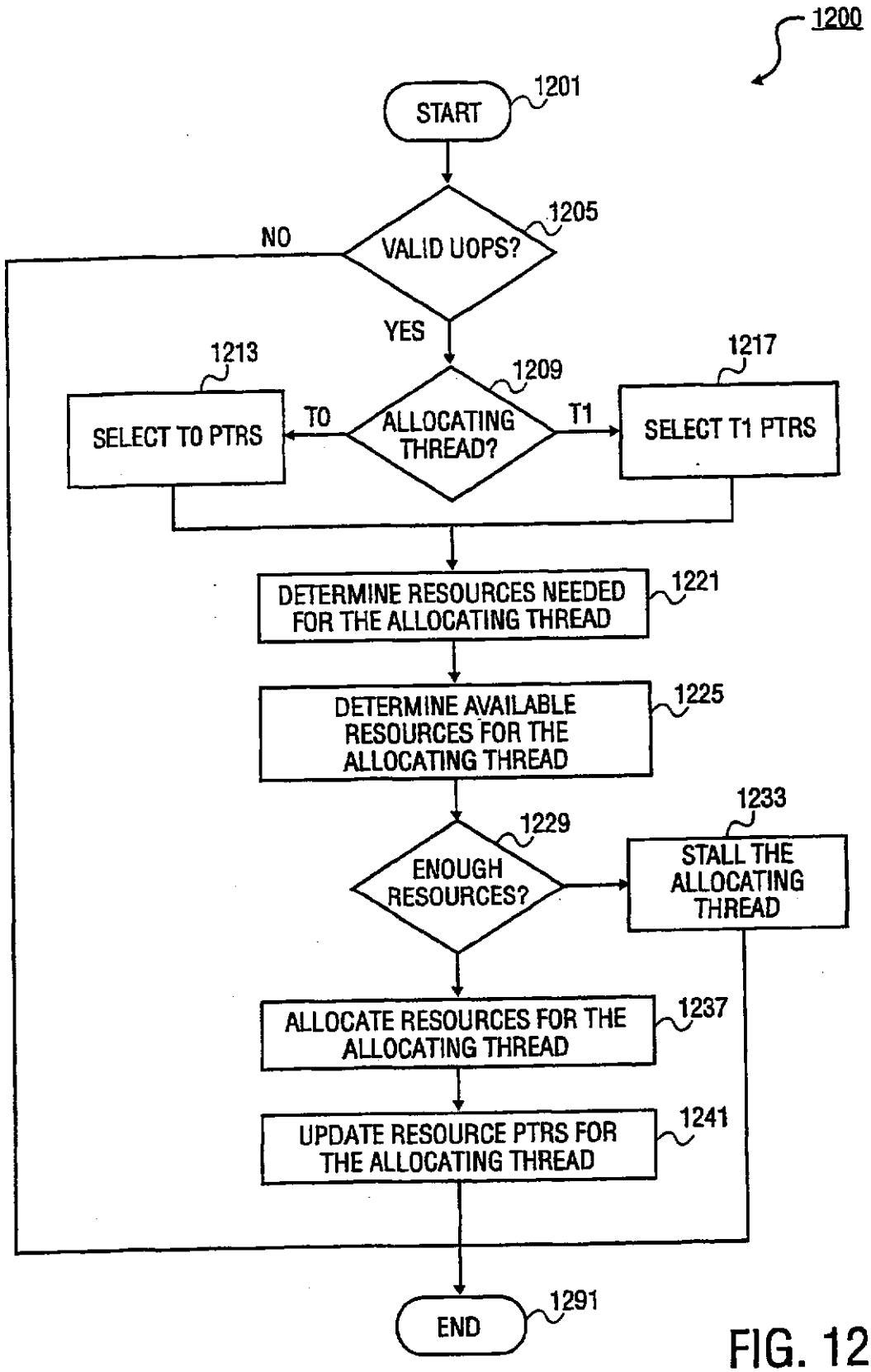

1200
START
1201
VALID UOPS?
1205
NO
YES
ALLOCATING THREAD?
1209
T0
T1
SELECT T0 PTRS
1213
SELECT T1 PTRS
1217
DETERMINE RESOURCES NEEDED FOR THE ALLOCATING THREAD
1221
DETERMINE AVAILABLE RESOURCES FOR THE ALLOCATING THREAD
1225
ENOUGH RESOURCES?
1229
STALL THE ALLOCATING THREAD
1233
ALLOCATE RESOURCES FOR THE ALLOCATING THREAD
1237
UPDATE RESOURCE PTRS FOR THE ALLOCATING THREAD
1241
END
1291

FIG. 12

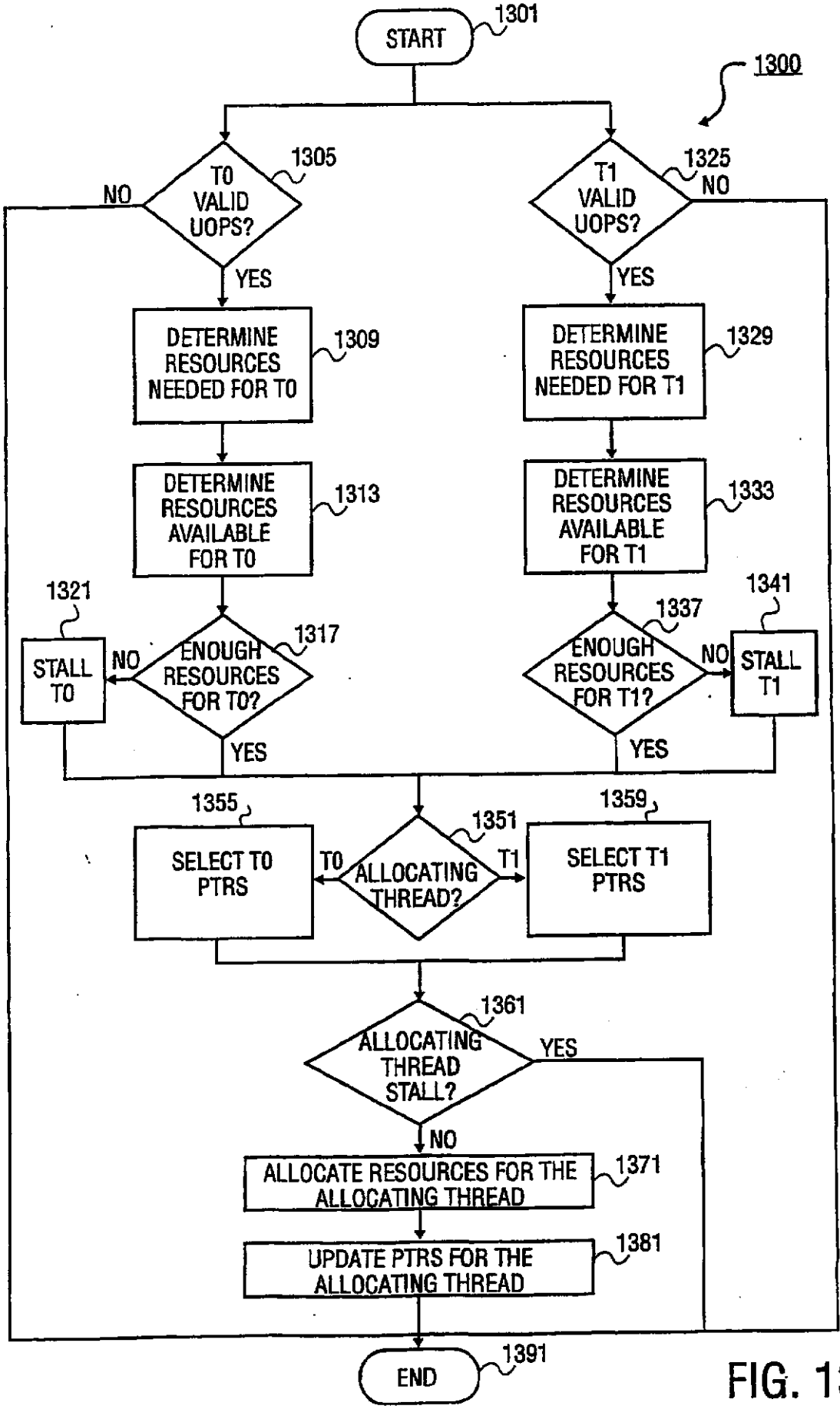

START
1301
1300
T0 VALID UOPS?
1305
NO
YES
T1 VALID UOPS?
1325
NO
YES
DETERMINE RESOURCES NEEDED FOR T0
1309
DETERMINE RESOURCES NEEDED FOR T1
1329
DETERMINE RESOURCES AVAILABLE FOR T0
1313
DETERMINE RESOURCES AVAILABLE FOR T1
1333
1321
STALL T0
NO
ENOUGH RESOURCES FOR T0?
1317
YES
1337
ENOUGH RESOURCES FOR T1?
NO
1341
STALL T1
YES
1355
SELECT T0 PTRS
T0
ALLOCATING THREAD?
1351
T1
1359
SELECT T1 PTRS
1361
ALLOCATING THREAD STALL?
YES
NO
ALLOCATE RESOURCES FOR THE ALLOCATING THREAD
1371
UPDATE PTRS FOR THE ALLOCATING THREAD
1381
END
1391

FIG. 13

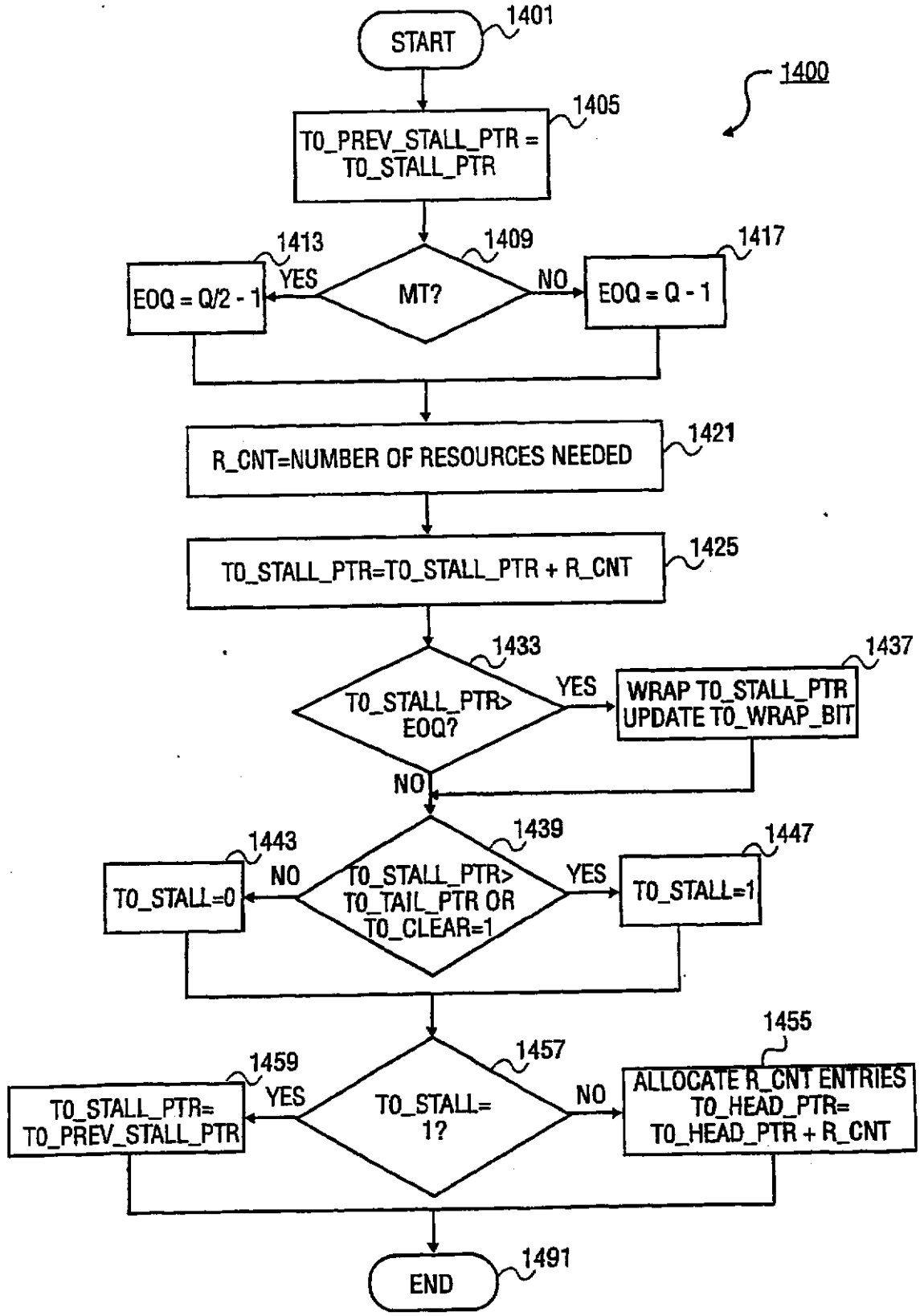

START
1401
1400
TO_PREV_STALL_PTR = TO_STALL_PTR
1405
MT?
1409
YES
EOQ = Q/2 - 1
1413
NO
EOQ = Q - 1
1417
R_CNT=NUMBER OF RESOURCES NEEDED
1421
TO_STALL_PTR=TO_STALL_PTR + R_CNT
1425
TO_STALL_PTR> EOQ?
1433
YES
WRAP TO_STALL_PTR UPDATE TO_WRAP_BIT
1437
NO
TO_STALL_PTR> TO_TAIL_PTR OR TO_CLEAR=1
1439
NO
TO_STALL=0
1443
YES
TO_STALL=1
1447
TO_STALL= 1?
1457
YES
TO_STALL_PTR= TO_PREV_STALL_PTR
1459
NO
ALLOCATE R_CNT ENTRIES TO_HEAD_PTR= TO_HEAD_PTR + R_CNT
1455
END
1491

FIG. 14

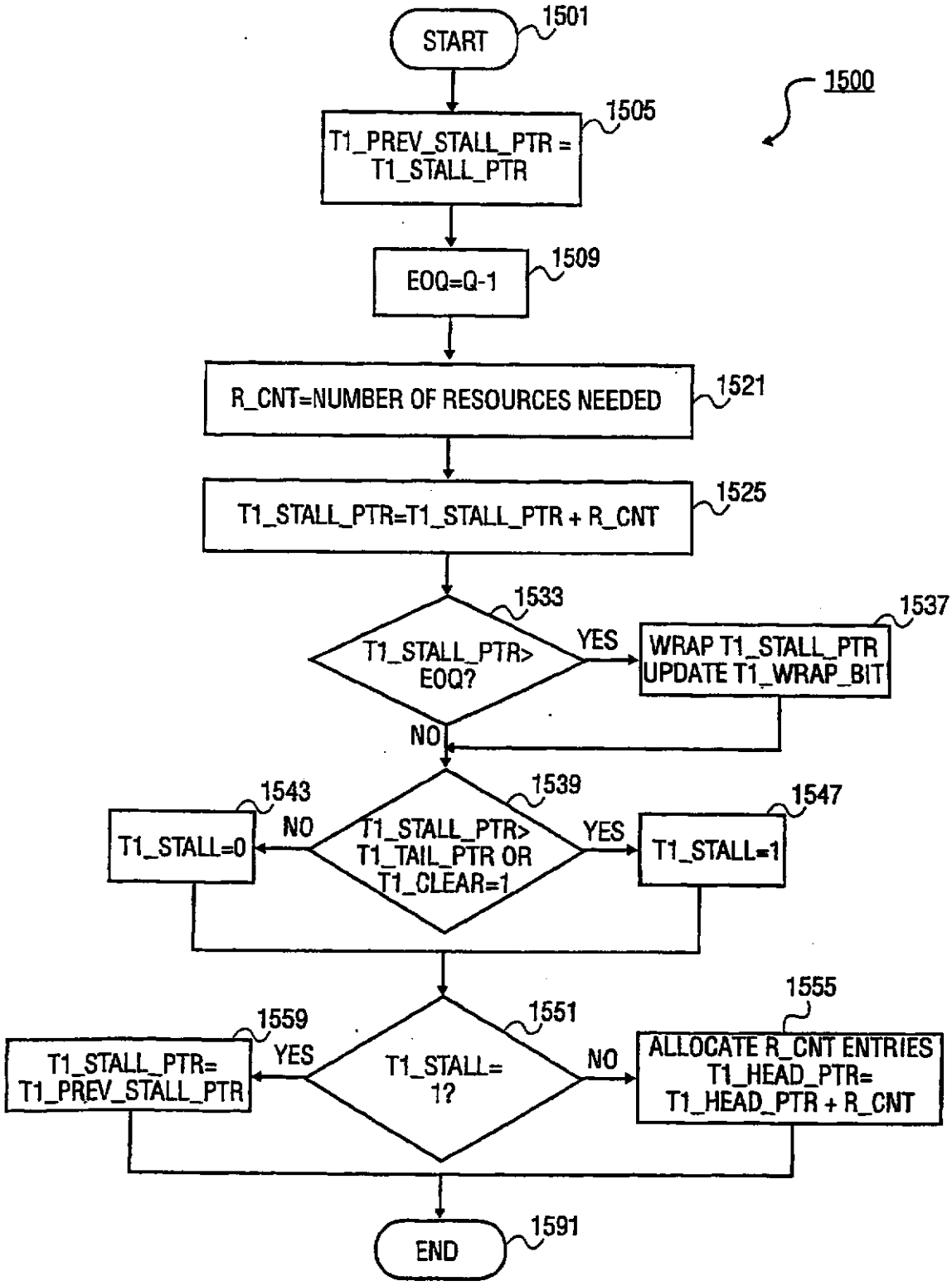

START
1501
1500
T1_PREV_STALL_PTR = T1_STALL_PTR
1505
EOQ=Q-1
1509
R_CNT=NUMBER OF RESOURCES NEEDED
1521
T1_STALL_PTR=T1_STALL_PTR + R_CNT
1525
T1_STALL_PTR> EOQ?
1533
YES
WRAP T1_STALL_PTR UPDATE T1_WRAP_BIT
1537
NO
T1_STALL_PTR> T1_TAIL_PTR OR T1_CLEAR=1
1539
NO
T1_STALL=0
1543
YES
T1_STALL=1
1547
T1_STALL= 1?
1551
YES
T1_STALL_PTR= T1_PREV_STALL_PTR
1559
NO
ALLOCATE R_CNT ENTRIES T1_HEAD_PTR= T1_HEAD_PTR + R_CNT
1555
END
1591

FIG. 15

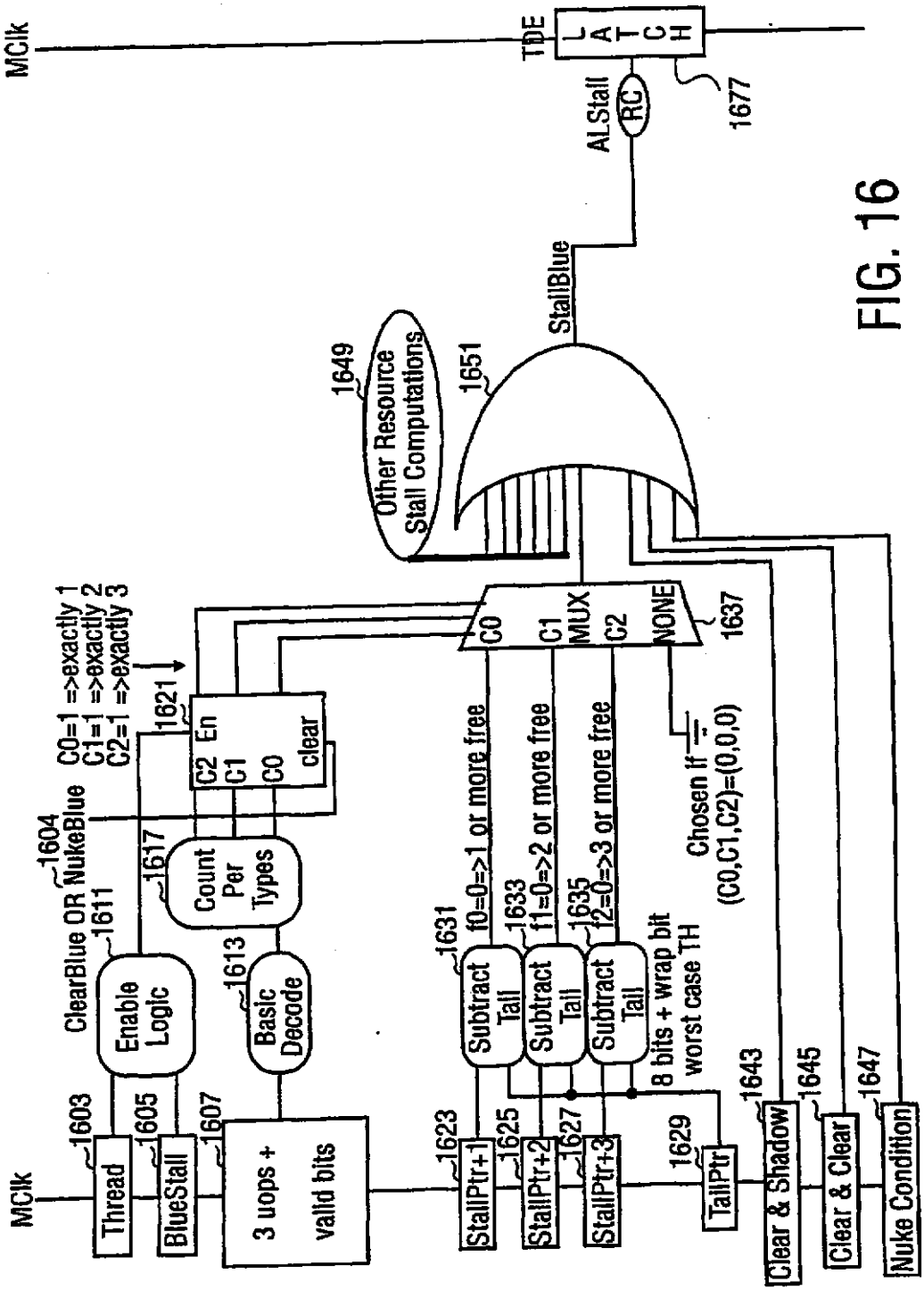

MClk
TDE
LATCH
ALStall
RC
1677
StallBlue
1649
Other Resource Stall Computations
1651
C0=1 =>exactly 1
C1=1 =>exactly 2
C2=1 =>exactly 3
1621
C2 En
C1
C0
clear
1604
NukeBlue
ClearBlue OR
1611
Enable Logic
1617
Count Per Types
1613
Basic Decode
C0
C1
MUX
C2
NONE
1637
Chosen if (C0,C1,C2)=(0,0,0)
1631
f0=0=>1 or more free
1633
f1=0=>2 or more free
1635
f2=0=>3 or more free
Subtract Tail
Subtract Tail
Subtract Tail
8 bits + wrap bit worst case TH
1643
1645
1647
MClk
1603
1605
1607
Thread
BlueStall
3 uops + valid bits
1623
1625
1627
StallPtr+1
StallPtr+2
StallPtr+3
1629
TailPtr
Clear & Shadow
Clear & Clear
Nuke Condition

FIG. 16

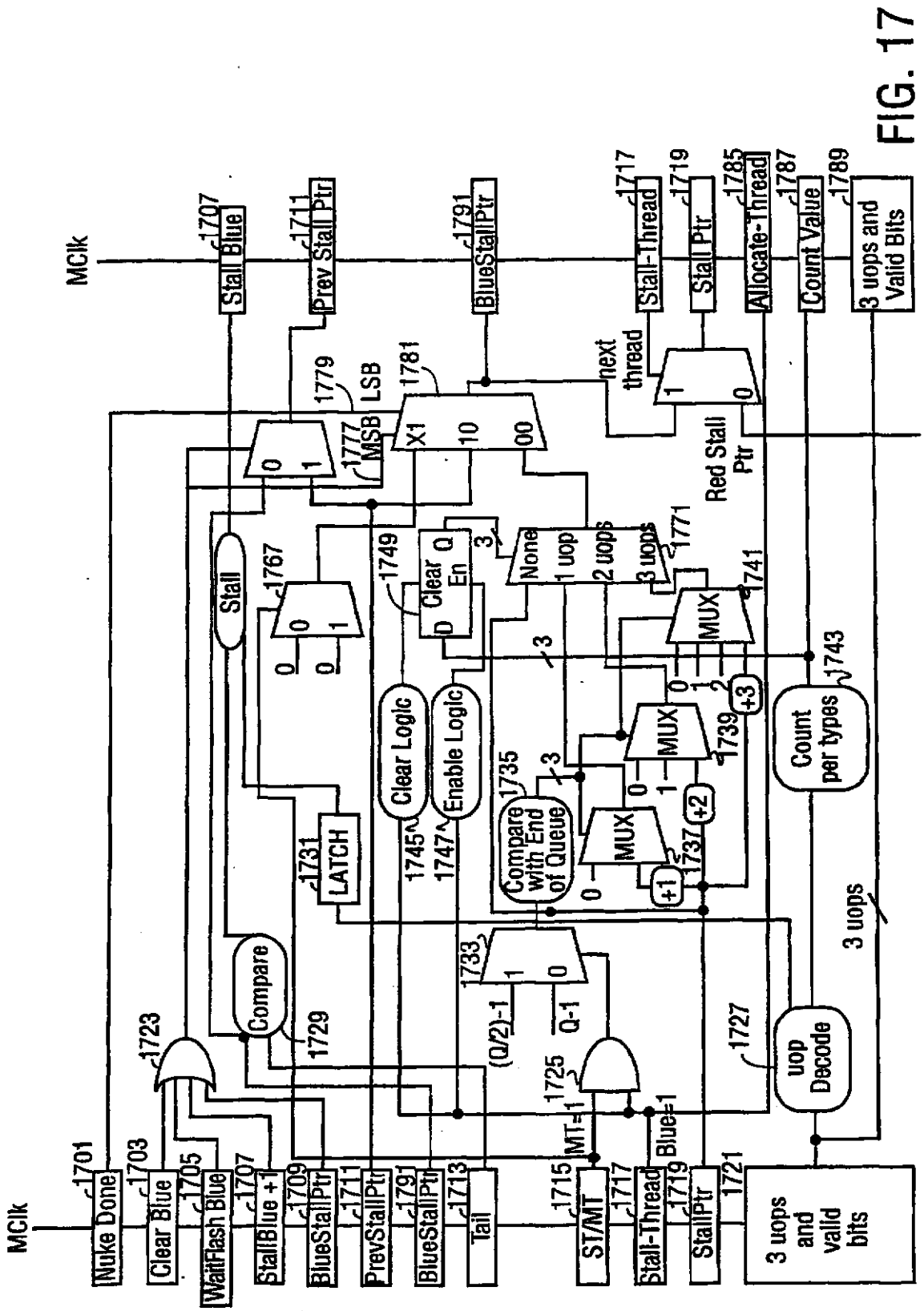

MClk
Nuke Done
Clear Blue
WaitFlash Blue
StallBlue +1
BlueStallPtr
PrevStallPtr
BlueStallPtr
Tail
ST/MT
Stall-Thread
StallPtr
3 uops and valid bits
MClk
Stall Blue
Prev Stall Ptr
BlueStallPtr
Stall-Thread
Stall Ptr
Allocate-Thread
Count Value
3 uops and Valid Bits
LSB
MSB
X1
10
00
next thread
Red Stall Ptr
Stall
Clear Q En D
None
1 uop
2 uops
3 uops
MUX
Clear Logic
Enable Logic
LATCH
Compare
Compare with End of Queue
(Q/2)-1
Q-1
MT=1
Blue=1
uop Decode
Count per types
3 uops
+1
+2
+3

FIG. 17

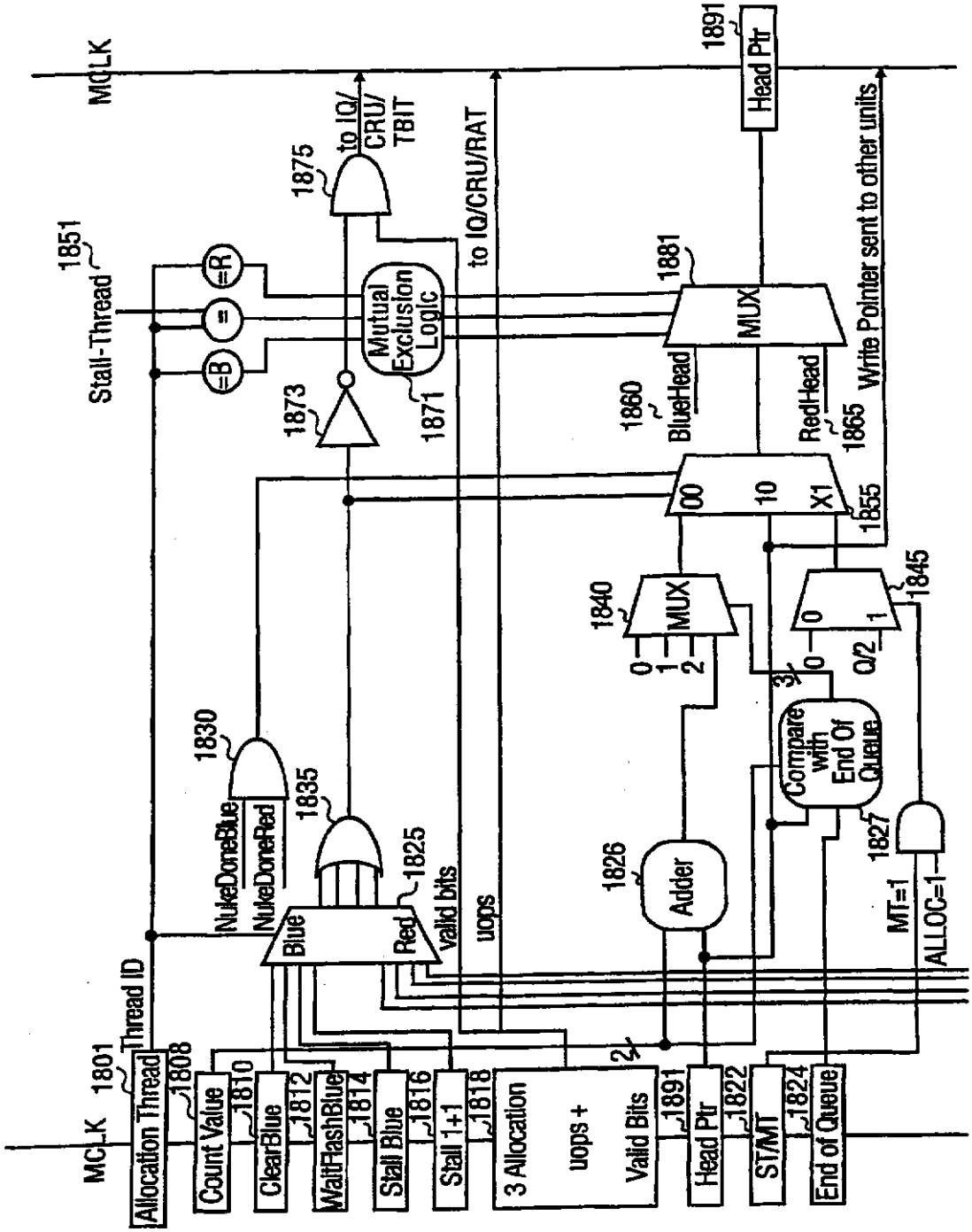

MCLK
1891
Head Ptr
1875
to IQ/ CRU/ TBIT
to IQ/CRU/RAT
Write Pointer sent to other units
1851
Stall-Thread
=R
=
=B
Mutual Exclusion Logic
1871
1873
1881
MUX
1860
BlueHead
RedHead
1865
00
10
X1
1855
1840
MUX
0
1
2
1845
0
1
Q/2
3
0
1830
1835
NukeDoneBlue
NukeDoneRed
1825
Blue
Red
Valid bits
uops
1826
Adder
Compare with End Of Queue
1827
MT=1
ALLOC=1
MCLK
1801
Thread ID
1808
Allocation Thread
Count Value
1810
ClearBlue
1812
WaitFlashBlue
1814
Stall Blue
1816
Stall 1+1
1818
3 Allocation uops +
Valid Bits
1891
Head Ptr
1822
ST/MT
1824
End of Queue

FIG. 18