SEMICONDUCTOR DEVICE AND A METHOD OF PRODUCING THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor devices of the carrier package type. It also relates to a method of producing the same.

In general, a semiconductor device of the type including a carrier package called a chip carrier can be completely installed merely by placing it directly on a circuit board for installation and connecting the wiring terminals of the circuit board with the external connection terminals of the semiconductor device. Therefore, the semiconductor device of the specified type is effective to facilitate the installing job and enables the whole apparatus in which the semiconductor device is built to be made thin, and so the demand tends to increase more and more.

Most of prior-art semiconductor devices of this type employ a carrier package of ceramic as shown in Figure 1. This carrier package 1 is constructed and used as stated below. A recess 3 is formed in the upper surface of a carrier base 2 which is formed of ceramic by, e.g. the green process. A semiconductor element

(pellet) 4 is fastened on the inner bottom surface of the recess 3. Leads 6, each of which consists of an inner lead for connection with the pellet and an outer lead for external connection, are formed by such an expedient as metallizing in a manner to extend from the perimeter of the recess 3 to the rear surface of the base. After the pellet 4 and the leads 6 are electrically connected by wires 7, the resultant structure is encapsulated by a cap 8 of metal or ceramic.

With this package, however, since there is a limitation to reduction in the thickness of the green ceramic, reduction in the thickness of the base 2 formed by the lamination thereof is naturally limited, which forms an obstacle to making the whole package thin. Moreover, since the green process referred to above includes many steps, and because of the material cost of the ceramic, the entire package is expensive.

Further, the ceramic has a greatly different coefficient of thermal expansion from a printed circuit board of a glass epoxy material or the like, which is usually used as a board for installation. Therefore, when the ceramic package is directly secured and connected to the printed circuit board of this type, a stress attributed to the difference of the coefficients of thermal expansion develops between the package and the

printed circuit board with a change in temperature, and the connection is sometimes damaged.

Moreover, such ceramic packages are manufactured individually one by one. It is therefore difficult to perform fully automatically the operations of fastening the pellet 4 onto the base 2, bonding the wires 7, fastening the cap 8, etc. Another disadvantage is that the dimensions of the packages manufactured individually are liable to errors, which render the automation more difficult.

In one aspect, this invention provides a semiconductor device comprising:

a base of glass epoxy, glass phenol, triazine, paper phenol, polyimide, or polyester, a recess being formed in a front surface of the base;

a plurality of inner leads on the front surface of the base surrounding the recess;

a plurality of outer leads on a rear surface of the base, the outer leads being respectively electrically connected to the inner leads;

a semiconductor element located in the recess, the semiconductor element being electrically connected to the inner leads; and

a resin which seals at least the semiconductor element and electrical connection parts between the semiconductor element and the inner leads.

In a second aspect, the invention provides a method of producing a semiconductor device, comprising:

preparing a base of glass epoxy, glass phenol, triazine, paper phenol, polyimide, or polyester;

forming a plurality of inner leads on the front surface of the base;

forming a plurality of outer leads on the rear surface of the base, the outer leads being respectively electrically connected to the inner leads;

forming a recess in the front surface of the base so that the recess is surrounded by the inner leads;

locating a semiconductor element in the recess;

electrically connecting the semiconductor element to the inner leads; and

sealing at least the semiconductor element and electrical connection parts between the semiconductor element and the inner leads with resin.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a perspective view, partly in section,

showing a prior-art semiconductor device of the carrier package type.

Figure 2(A) is a perspective view, partly in section, of a semiconductor device embodying the present invention, while Figure 2(B) is a rear perspective view of the semiconductor device shown in Figure 2(A).

Figures 3(A) - 3(I), Figure 4 and Figure 5 are diagrams showing different stages of a method of producing the semiconductor device shown in Figures 2(A) and 2(B), in which Figures 3(A), 3(B), 3(D), 3(F), 3(G) and 3(H) are front perspective views, Figure 3(C) is a sectional view and Figures 3(E) and 3(I) are rear perspective views, Figure 4 is a perspective view of a frame in a multiple state, and Figure 5 is a sectional view showing the state in which the assemblage is completed.

Figure 6 is a sectional view of a semiconductor device according to another embodiment.

Figure 7 is a sectional view of a semiconductor device according to still another embodiment, while Figure 8 is a rear perspective view of the semiconductor device shown in Figure 7.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor device according to the present invention and a method of producing the same will be described in conjunction with illustrated embodiments.

Figures 2(A) and 2(B) are fragmentary perspective views of a semiconductor device 10 according to the present invention. Referring to the figures, numeral 11 designates a base which is made of a glass epoxy plate (glass fibers filled with an epoxy resin). The kind usually used as a printed circuit board can be utilized for the glass epoxy plate. Conductive layers formed on both the surfaces of the circuit board are etched as will be described later, to form inner leads 12 and outer leads 13, and these inner and outer leads are connected by connective portions 14 formed by the through-hole technique, whereby leads 15 are formed. A square recess 16 is formed centrally of the upper surface of the base 11 by cutting or the like, and a semiconductor element (pellet) 17 is fixed on the inner bottom surface of the recess by a binder or the like. The electrode pads of the pellet 17 and the aforementioned inner leads 12 are connected by wires 18. Thereafter, the pellet 17, wires 18 and inner leads 12 are covered with a resin 19 supplied onto the base 11 by such a technique as potting, whereby they are encapsulated. In the leads 15, at least the inner leads 12 and the outer leads 13 are plated with gold so as to facilitate soldering at the connection of the wires 18 and the installation of the semiconductor device.

The exposed parts of the leads (except the wire bonding parts thereof) on the upper surface of the base 11 may well be coated in advance with a resin 20 for protection.

As shown in Figure 2(A), the semiconductor device constructed as above described is placed with its rear surface facing down, on conductive patterns 22 which are formed on an ordinary printed circuit board 21 made of, e. g., glass epoxy or glass phenol. The outer leads 13 are directly connected to the respectively corresponding pattern electrodes 22 by a brazing material such as a solder. Then, the installation is finished.

Now, the method of producing the semiconductor device of the above construction will be described with reference to Figures 3(A) - 3(I), Figure 4 and Figure 5.

First, as shown in Figure 3(A), a substrate 26 is prepared in which conductive copper foil layers 24 and 25 are respectively formed on the front and rear surfaces (upper and lower surfaces) of a glass epoxy plate 23. In this case, since a plurality of (five) packages are usually formed in multiple fashion and at the same time, an elongate substrate is used as the substrate 26. In the following, the method of production will be described with stress laid on a single package.

Subsequently, as shown in Figure 3(B), vertically penetrating through-holes 27 in a number corresponding

to the leads 15 are formed in a manner to extend along the outer edge of the package P to be formed and in those positions on the substrate 26 which can be connected with the leads 15 to be formed. As shown in Figure 3(C), a copper plating layer 28 which provides the connecting portion 14 is formed by electroless plating on the inner peripheral surface of each through-hole 27, in such a manner that the respective copper foils 24 and 25 of the upper and lower surfaces become electrically connected through the copper plating layer 28. Thereafter, as shown in Figures 3(D) and 3(E), the respective copper foils 24 and 25 on the upper and lower surfaces of the substrate 26 are photoetched to form the plurality of inner leads 12 and outer leads 13 which are independent of one another. Needless to say, the photoetching is such that the copper is etched by utilizing a photoresist pattern film which has been formed by the formation of a photo resist film, the exposure of the film through a mask pattern and the developing of the exposed film. In the etching step, the inner leads 12 on the front surface have shapes independent of one another, whereas the outer leads 13 are formed in such a manner that the respective leads are electrically conductive in an area 13A outside the parts extending along the outer edge of the package. In addition, the outer leads of the

respective packages are interconnected by connecting lines 29. As a result, the respective inner leads 12 are connected to the corresponding outer leads 13 through the copper plating layers 28 in the through-holes 27, and the independent leads 15 are to be constructed of the inner leads 12, the through-holes 27 and the outer leads 13. In this state, however, all the leads 15 are connected together owing to the connecting lines 29 and to the configuration of the outer leads described above.

After the leads 15 have been formed as described above, the protective resin 20 is deposited on the intermediate parts of the inner leads 12 on the upper surface of the substrate 26 in the shape of a belt by screen printing or the like, as illustrated in Figure 3(F). This protective resin 20 may be applied as needed. The parts of the inner leads 12 not coated with the protective resin 20 are subjected to foundation plating with Ni and plating with Au in the next step. These plating operations are electroplating, and the common connection of the connecting lines 29 and the outer leads 13 permits the plating of all the leads merely by connecting a power supply to a single lead.

Subsequently, as shown in Figure 3(G), the recess 16 is formed as follows. The upper surface of

the substrate 26, namely, the central part of the package is machined by spot facing into a square which is somewhat larger than the semiconductor element (pellet). In addition, as shown in Figure 3(H), slots 31 are formed by punching four sides along the outer edge of the package. The slots 31 establish a state in which the package base 11 to be formed is suspended and supported by an outer peripheral portion (frame portion) 33 through four bridging portions 32 that are formed between the slots 31. Accordingly, the resultant structure is in a state in which the package base 11 can be simply obtained by cutting the bridging portions 32, which have a small width. In addition, since the slots 31 have their inner edges extended along the through-holes 27, the inner parts of the through-holes 27 (gold-plated copper plating layers 28) are exposed as the outer edge of the package base 11 by the slots. Simultaneously therewith, the slots 31 punch the outside area 13A of the outer leads 13. As shown in Figure 3(I), therefore, the outer leads 13 are respectively separated into insulated states, and the connecting lines 29 are cut off to disconnect the respective packages from each other.

By the above steps, a multiple frame 40 is formed in which, as shown in Figure 4, the five package bases 11 are formed on the elongate substrate of the glass epoxy plate 26 in multiple fashion. Each base 11 has

the recess 16 for fastening the semiconductor element pellet thereon, in the central part of the front surface, the inner leads 12 around the recess, and the outer leads 13 connected to the inner leads 12 through the connecting portions, on the rear surface. The inner leads, the connecting portions and the outer leads constitute the leads 15. On both the sides of the base substrate 26, guide holes 34 are successively provided at suitable pitches (equal to the pitches of the bases). The guide holes 34 are formed simultaneously with the slots 31. The multiple frame 40 is loaded in an automatic assembly machine, not shown, and the steps of and after mounting the semiconductor elements (pellets) are carried out.

More specifically, as shown in Figure 5, the semiconductor element (pellet) 17 is fastened on the inner bottom surface of the recess 16 of the package base 11 with a suitable binder, whereupon the inner ends of the respective inner leads 12 and the electrode pads of the pellet 17 are connected by the wires 18. Thereafter, the sealing resin 19 is dropped on the package base 11 by potting or the like so as to seal the pellet 17, wires 18 and inner leads 12. Thus, the assemblage on each package base is completed. Subsequently, when the bridging portions 32 are properly cut, the finished packages separate from the frame portion 33 and are obtained

independently of one another.

In the assembling operations, accordingly, the semiconductor elements can be assembled on the base substrate 26 of Figure 4 by steps and facilities similar to those in the case of forming packages by the use of a multiple lead frame, and automation of the assemblage can be realized.

In a case where, in the foregoing process of production, the power supply portions of the respective packages are connected in advance in parallel with one another by common lines, and these common lines are left even after the outer leads and connective lines have been cut by the formation of the slots 31, all the packages can be simultaneously supplied with currents merely by energizing some of the common lines after the respective packages have been finished. Thus, ageing operations can be performed with ease and at high efficiency. After completion of the ageing at a temperature, at a voltage and for a period of time as predetermined, the second punching of cutting the common lines is carried out to construct the respective packages as being electrically independent (even in this case, the respective packages are held mechanically integral through the frame portion 33 by the bridging portions 32), whereby the respective packages can be tested individually and integrally.

Since the semiconductor device produced as described above uses a single substrate, the thickness of the whole device may be substantially equal to that of the substrate, and this is effective for making the device thin. In addition, since the number of steps is small and no expensive material is used, the device has the effect that it can be produced at low cost. Further, since the base of the device employs a material which is the same as or equivalent to the ordinary printed circuit board, they have substantially equal coefficients of thermal expansion, so that the damage to the connection as a result of a temperature change does not occur even in a case where the device has been installed directly on the printed circuit board. Since the package is not of ceramic, it can attain a high dimensional accuracy.

In accordance with the preferred method of producing a semiconductor device according to the present invention, the plurality of packages can be simultaneously formed on the single substrate. Therefore, the production efficiency of the semiconductor devices becomes higher than in the case of the ceramic package. In addition, efficient production is permitted in such a manner that various operations in the process for production are facilitated and that ensuring dimensional accuracy, etc. is also

facilitated.

While, in the foregoing embodiments, glass epoxy is used as the material of the substrate, there may be utilized other materials such as polyester, polyimide, paper phenol and triazine. In addition, while the leads are plated with gold to improve of the solderability thereof as well as the bondability of the wires, plating with Al, Ag or Ni may instead be performed in some cases.

Further, to provide for heat radiation where there is an enhanced density of integration or when manufacturing a semiconductor device, such as a power IC, in which importance is attached to heat radiation, the semiconductor device may be produced as follows. The photoetching processing of the copper foil 25 in the step of Figure 3(E) is so performed that the copper foil is left in a part surrounded by and separated from outer leads 13 on the rear surface of the substrate 26 (in the area to become the base 11). Thus, the copper foil formed on the rear surface of the area which will become the base 11 can act as a heat sink. Thereafter, processing similar to the foregoing steps of Figures 3(F) - 3(I) is carried out. Further, processing such as the mounting of the pellet and the potting of the resin is carried out. A sectional view of the semiconductor device produced by such method is shown in Figure 6.

In the figure, numeral 30 indicates the copper foil which serves as the heat sink. Parts indicated by the other numerals are the same as those explained in Figure 5.

Alternatively, after the heat sink 30 has been formed as described above, the recess 16 in the central part of the package base 11 is formed rather more deeply than described above, forming a square opening through the glass epoxy substrate and exposing a part of the heat sink 30. The semiconductor element 17 is fastened on the exposed surface of the heat sink, the element 17 and the inner leads 12 are connected by the wires 18, and the resin 19 which covers the element 17, the wires 18 and parts of the inner leads 12 is applied by potting. A section of a semiconductor device formed by such method is shown in Figure 7, and a rear perspective view is shown in Figure 8. Referring to the figures, the semiconductor element 17 is connected to the heat sink 30, and this semiconductor element 17 and the inner leads 12 are connected by the wires 18. The semiconductor element 17, the wires 18 and the parts of the inner leads 12 are covered with the resin 19. With such method, the semiconductor element is connected directly to the copper foil, so that the heat radiation characteristic is improved more.

When the thickness of the copper foil is insufficient to be expedient for forming the heat sink, it may

be increased by plating or by stacking another copper foil on it. Alternatively, the copper foil may be replaced with a copper plate.

As set forth above, a base substrate whose material is glass epoxy or the like is provided with leads and is formed into package bases, pellets are fastened on the bases and are subjected to wire bonding, and the resultant structure is sealed with a resin. Therefore, making the semiconductor device thin and lowering the cost thereof can be achieved, and the installation of the semiconductor device on a printed circuit board usually used is facilitated. On the other hand, there are attained the effects that the dimensional accuracy can be enhanced and that automation of production can be achieved.

Moreover, according to the preferred production method of the present invention, the aforementioned semiconductor device can be produced readily and efficiently.

U.K. patent application No. 84.11298 (published under number) has been divided out of the present application and describes matter also contained in the present application. Attention is therefore drawn to that application.

CLAIMS.

1. A semiconductor device comprising:

a base of glass epoxy, glass phenol, triazine, paper phenol, polyimide, or polyester, a recess being formed in a front surface of the base;

a plurality of inner leads on the front surface of the base surrounding the recess;

a plurality of outer leads on a rear surface of the base, the outer leads being respectively electrically connected to the inner leads;

a semiconductor element located in the recess, the semiconductor element being electrically connected to the inner leads; and

a resin which seals at least the semiconductor element and electrical connection parts between the semiconductor element and the inner leads.

2. A semiconductor device according to claim 1, wherein the recess is blind and the semiconductor element is mounted on the bottom of the recess.

3. A semiconductor device according to claim 1 or claim 2, wherein a heat sink is provided on the rear surface of the base.

4. A semiconductor device according to claim 1, wherein the recess extends completely through the base, a heat sink is provided on the rear surface of the base, and the semiconductor element is mounted on the heat sink in the recess.

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5. A semiconductor device according to any one of the preceding claims wherein the inner and outer leads are connected by a plurality of connective portions at a side surface of the base.

6. A semiconductor device according to any one of the preceding claims, wherein the semiconductor element and the inner leads are electrically connected by wires.

7. A method of producing a semiconductor device, comprising:

preparing a base of glass epoxy, glass phenol, triazine, paper phenol, polyimide, or polyester;

forming a plurality of inner leads on the front surface of the base;

forming a plurality of outer leads on the rear surface of the base, the outer leads being respectively electrically connected to the inner leads;

forming a recess in the front surface of the base so that the recess is surrounded by the inner leads;

locating a semiconductor element in the recess;

electrically connecting the semiconductor element to the inner leads; and

sealing at least the semiconductor element and electrical connection parts between the semiconductor element and the inner leads with resin.

8. A method according to claim 7, wherein the inner and outer leads are electrically connected by forming connective portions between the inner and outer leads.

9. A method according to claim 8, wherein the connective portions are formed by providing through-holes in the base and forming conductive plating layers on inner surfaces of the through-holes.

10. A method according to any one of claims 7 to 9, wherein the inner leads and outer leads are formed by forming conductive foils on the front and rear surfaces of the base and selectively etching the foils.

11. A semiconductor device substantially as any described herein with reference to Figs. 2 to 8 of the drawings.

12. A method of producing a semiconductor device substantially as any herein described with reference to Figs. 2 to 8 of the drawings.