

"A dynamic ram integrated circuit device".

The present invention relates to a D-RAM (dynamic random-access memory) integrated circuit device comprising MISFETs (metal insulator semi-conduction field-effect transistors).

5 In a typical D-RAM, a memory array comprises a plurality of memory cells arranged in a matrix, data lines and word lines. In reading out data, a minute potential change is applied to a data line from such a memory cell as comprising a single
10 transistor. In order to permit amplification of such a minute potential change, two data lines are paired in ordinary D-RAMs. When the stored data in the memory cell connected to one of a paired data lines (referred to as "pair data line"
15 hereinafter) is read out, a reference potential is applied to the other of the pair data line by a proper means such as a dummy cell. The potential difference between the lines constituting the pair data line is amplified by means of a sense amplifier.

In reading out data from the memory cells, such a potential fluctuation which may be considered as noise is applied to each of the data lines from a word line through an undesirable capacitance such as a parasitic capacitor. The effect due to the potential fluctuation is substantially reduced by means of a folded bit line arrangement. In other words, a single word line is made to cross each line of a pair data line, in order to simultaneously apply such a noise which is considered to be a common mode noise to both the lines constituting the pair data line. The common mode noise can be substantially reduced by means of a differential type sense amplifier. Consequently, it becomes possible to read out data from the memory cells with substantially no error independently of the undesirable potential fluctuation applied to the data lines from the word line.

We have discovered that a relatively large differential mode noise is applied to the pair data line located at an end part of the memory array.

The differential mode noise is produced owing to the word line selecting operation and the substrate bias voltage fluctuation.

It is an object of the present invention to provide a D-RAM integrated circuit device wherein coupling noises produced in the lines constituting



a pair data line respectively owing to the word line selecting operation and the substrate bias voltage fluctuation are made substantially equal to each other.

According to the present invention there is
5 provided a dynamic RAM integrated circuit device having a folded bit line arrangement including:

(a) a memory array having a plurality of pair data lines formed on a semiconductor substrate, a plurality of memory cells connected with the
10 corresponding one of said plurality of pair data lines and a plurality of word lines each connected with the corresponding ones of said plurality of memory cells; and

(b) an additional compensating data line
15 formed on said semiconductor substrate so as to extend close to as well as in parallel with a pair data line in said plurality of pair data lines arranged in an end of said memory array, in order to decrease the difference between the stray capacitances connected to the lines
20 constituting said pair data line arranged at an end of said memory array respectively.

As a result, it is possible to equalize the composite parasitic capacitances between data lines with each other. Consequently, coupling noises
25 from the word lines and dummy word lines and the coupling noises due to

the fluctuation in the substrate bias voltage $-V_{BB}$ are produced equally in the lines constituting each pair data line. Accordingly, it is possible to cancel out the coupling noises produced in the lines constituting a pair data line respectively by means of a differential type sense amplifier provided to each pair data line.

Thus, it is possible to prevent malfunction and increase the input level margin, since the minute voltage difference fed to the differential type sense amplifier is not affected by the coupling noises.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a block diagram of a known type D-RAM circuit;

Figure 2A is a block diagram of a first example of a circuit constituting an essential part of a D-RAM according to the present invention;

Figure 2B is a circuit diagram of a practical example of the essential part;

Figure 2C is a waveform diagram illustrating the operation of the essential part shown in Figure 2B;

Figure 2D is a block diagram of a second example of the circuit constituting an essential part of a D-RAM according to the present invention;

Figure 2E is a circuit diagram of a practical example of the essential part;

Figure 3A is a circuit diagram of a preferred embodiment of a D-RAM;

5 Figure 3B is a waveform diagram of the operation of the D-RAM shown in Figure 3A;

Figure 4A shows a layout pattern of an example of a memory array M-ARY and a dummy array D-ARY;

10 Figure 4B shows a layout pattern of an example of a part of a sense amplifier;

Figure 4C shows a layout pattern of another example of the memory array and the dummy array;

Figure 4D shows a layout pattern of another example of the part of the sense amplifier;

15 Figure 5 shows a basic pattern of a field insulating film 2;

Figure 6 shows a basic pattern of a polycrystalline silicon layer 6; and

20 Figure 7 shows sectional views of the IC structure taken along lines X_1-X_1 , X_2-X_2 and X_3-X_3 of the layout patterns shown in Figures 4A, 4B and 4C respectively.

Before describing the embodiments of the present invention, a known type of D-RAM integrated
25 circuit having a folded bit line arrangement will be described for the purpose of assisting in the understanding of the present invention.

Referring to Fig. 1, the D-RAM has a memory array comprising a plurality of memory cells M-CEL arranged in a matrix, dummy cells D-CEL, data lines $DL_{1-1} \sim \overline{DL_{1-n}}$, word lines $WL_{1-1} \sim WL_{1-m}$ and dummy word lines DWL_{1-1}, DWL_{1-2} . Each memory cell consists of a single transistor cell and has an input/output terminal connected with a data line and a selection terminal connected with a word line. Pair data lines, e.g., DL_{1-1} and $\overline{DL_{1-1}}$ are connected with input/output terminals of a differential type sense amplifier SA_1 .

An outline of the data reading-out operation in the D-RAM is as follows.

First, the potential of a word line to be selected, e.g. the word line WL_{1-1} , and the potential of the dummy word line DWL_{1-2} corresponding thereto are simultaneously changed from low levels to high levels respectively. When the potential of the word line WL_{1-1} is at a high level, the memory cells M-CEL in the first row, whose selection terminals are connected with the word line WL_{1-1} , are selected. Consequently, the potential of each of the data lines $DL_{1-1}, \overline{DL_{1-1}}, \dots$, previously set at a proper initial value is changed to a voltage corresponding to the data, "1" or "0", previously stored in the memory cells selected by means of the word line WL_{1-1} .

At the same time, the dummy cells D-CEL in the second row, whose selection terminals are connected with the dummy word line DWL_{1-2} are selected. Consequently, the initial voltage of each of the data lines $\overline{DL_{1-1}}$, $\overline{DL_{1-2}}$, ..., $\overline{DL_{1-n}}$ is changed to a given reference voltage.

As a result, a minute voltage difference with a polarity corresponding to the data previously stored in the selected memory cells is applied between the lines constituting each of pair data lines, e.g., $\overline{DL_{1-1}}$ and $\overline{DL_{1-1}}$.

The minute voltage difference applied to each of pair data lines is amplified until it becomes a sufficiently large voltage difference by means of the corresponding one of the differential type sense amplifiers SA_1 , SA_2 , ..., SA_n provided to the pair data lines respectively.

Next, a pair data line is selected from the pair data lines by means of a column switch C-SW. The signal on the selected pair data line is

transmitted to the outside of the D-RAM through a data output buffer DOB, not shown. Thus, the data stored in any memory cell is read out.

The selection of the word lines and the dummy word lines is effected by means of a row decoder circuit R-DCR, while the column switch is controlled by means of a column decoder circuit C-DCR, not shown.

The word lines WL_{1-1} , WL_{1-2} , ..., WL_{1-m} and the dummy word lines DWL_{1-1} , DWL_{1-2} cross all the data lines DL_{1-1} , $\overline{DL_{1-1}}$, ..., DL_{1-n} , $\overline{DL_{1-n}}$ each other respectively even in an actual device structure. A parasitic capacitance between a data line and a word line C_{dw} , or $C_{dw''}$ ($C_{dw} < C_{dw''}$) is formed at each of intersections between the word lines and the data lines. The parasitic capacitance between a data line and a word line C_{dw} , substantially represents the parasitic capacitance formed at the intersection where a memory cell is arranged. On the other hand, the parasitic capacitance between a data line and a word line $C_{dw''}$ represents the parasitic capacitance formed at the intersection where a memory cell is not arranged.

Including the gate-drain capacitance of a switch MISFET, not shown, in each memory cell M-CEL, the parasitic capacitance C_{dw} , has a capacitance value larger than that of the parasitic capacitance $C_{dw''}$ formed simply by the crossed wiring structure.

Because of the presence of the parasitic capacitances $C_{dw'}$, $C_{dw''}$, a coupling noise is applied to each data line when the potential of a word line rises from a low level to a high level.

It is expected in the folded bit line arrangement D-RAM that the coupling noise applied to each line of a pair data line from a word line and a dummy word line will be a common mode noise. Therefore, the noises applied to the lines constituting a pair data line respectively are expected to be substantially neglected by a differential type sense amplifier.

For instance, when the word line WL_{1-1} is selected, a coupling noise is applied to the data line DL_{1-1} from the word line WL_{1-1} through the parasitic capacitance $C_{dw'}$, while a coupling noise is applied to the data line $\overline{DL}_{1-1}$ from the word line WL_{1-1} through the parasitic capacitance $C_{dw''}$. At this time, since the dummy word line DWL_{1-2} is

also selected correspondingly to the word line WL_{1-1} , a coupling noise is applied to each of the data lines DL_{1-1} , $\overline{DL_{1-1}}$ also from the dummy word line. Therefore, it is considered that the

5 parasitic capacitance between, e.g., the data line DL_{1-1} and the selected word line WL_{1-1} and the parasitic capacitance between the data line DL_{1-1} and the dummy word line DWL_{1-2} substantially constitute a single composite parasitic capacitance

10 which applies a coupling noise to the data line DL_{1-1} .

If the parasitic capacitance C_{ddw} formed between the dummy word line DWL_{1-2} and the data line DL_{1-1} is made equal to the parasitic

15 capacitance C_{dw} formed between the word line WL_{1-1} and the data line $\overline{DL_{1-1}}$ and if the parasitic capacitance C_{ddw} formed between the dummy word line DWL_{1-2} and the data line $\overline{DL_{1-1}}$ is made equal to the parasitic capacitance C_{dw} formed between

20 the word line WL_{1-1} and the data line DL_{1-1} , the composite parasitic capacitance ($C_{dw} + C_{ddw} = C_{dw}$) connected to the data line DL_{1-1} when the word line WL_{1-1} is selected becomes equal to the

25 composite parasitic capacitance ($C_{dw} + C_{ddw} = C_{dw}$) connected to the data line $\overline{DL_{1-1}}$.

As a result, the noise applied to the data line DL_{1-1} when the word line WL_{1-1} is selected will have a level substantially equal to that of the noise applied to the data line $\overline{DL}_{1-1}$. Moreover, the noise applied to each of the pair data line DL_{1-1} and $\overline{DL}_{1-1}$ is reduced by the differential type sense amplifier SA_1 because the noise is substantially a common mode noise.

We have found as mentioned above that the noise applied to one of the lines constituting a pair data line, e.g., DL_{1-1} , arranged at an end part of the memory array does not substantially coincide with the noise applied to the other of the lines constituting the pair data line, i.e., $\overline{DL}_{1-1}$.

In other words, the data lines DL_{1-1} , $\overline{DL}_{1-1}$, ..., DL_{1-n} , $\overline{DL}_{1-n}$ in the D-RAM are formed from, e.g., the same wiring layer and arranged adjacent to each other at substantially equal distances.

Accordingly, a parasitic capacitance between data lines C_{dd} having a value which cannot be neglected is formed between data lines adjacent to each other.

In Fig. 1, the parasitic capacitance between data lines connected with each of the data lines arranged inside the memory array, i.e., each of the data lines other than the data lines DL_{1-1} and $\overline{DL_{1-n}}$ arranged at the end parts of the memory array respectively, is $2 C_{dd}$ because the parasitic capacitance has data lines arranged on both sides thereof.

On the other hand, the parasitic capacitance between data lines connected with each of the data lines DL_{1-1} and $\overline{DL_{1-n}}$ arranged at the end parts of the memory array respectively is C_{dd} because the parasitic capacitance has only one data line arranged on one side thereof.

Consequently, the coupling noises applied to the pair data line DL_{1-1} and $\overline{DL_{1-1}}$ arranged at an end part of the memory array respectively are not equal to each other. Similarly, the coupling noises applied to the pair data line at the lowermost end part respectively are not equal to each other.

When the elements are miniaturized in order to increase the memory capacitance, i.e. for increasing the density of the memory array, the parasitic capacitance C_{dd} in

the same wiring layer is increased. Therefore, the unbalance between the coupling noises produced in the above-mentioned pair data line is substantially increased.

5 When the potential of each of a word line and a dummy word line rises from a low level (0 V) to a high level (V_{cc}) in the D-RAM, the approximate values of the coupling noises (voltage varying quantities) ΔV_N , $\Delta V_N'$ applied to the pair data
10 line (DL_{1-1} , DL_{1-n}) by the effects of the composite parasitic capacitance between a data line and a word line C_{dw} , the parasitic capacitance between data lines C_{dd} and the other parasitic capacitance of the data line C_o are obtained
15 according to the two following equations:

$$\Delta V_N = \frac{C_{dw}}{C_{dw} + C_o + C_{dd}} V_{cc} \quad \dots (1)$$

$$\Delta V_N' = \frac{C_{dw}}{C_{dw} + C_o + 2C_{dd}} V_{cc} \quad \dots (2)$$

It is to be also noted that the parasitic capacitance C_o includes the junction capacitance
20 between the drain of the MISFET constituting a memory cell and a substrate. Accordingly, the fluctuation in the substrate bias voltage - V_{BB} applied to the substrate causes similar coupling noises to be generated in the data lines.

Also in this case, coupling noises to be unbalanced are generated in the outermost pair data lines DL_{1-1} , $\overline{DL_{1-1}}$ and DL_{1-n} , $\overline{DL_{1-n}}$.

Thus, if coupling noises are not equally
5 generated in the lines constituting a pair data line, the differential type sense amplifier fed with the signal on the pair data line as an input signal is liable to malfunction.

Consequently, when the data stored in a
10 memory cell appears on a pair data line in the form of a minute voltage difference, coupling noises may cause the minute voltage difference to decrease, so that the noise margin of the signal to be detected may be reduced to such an extent that
15 the lowering degree cannot be disregarded.

Such a problem occurs, for example, when the signal corresponding to the data "0" stored in a memory cell is read out to the uppermost end data line DL_{1-1} .

20 In this case, the voltage of the data line DL_{1-1} is lower than the voltage (reference voltage) of the data line $\overline{DL_{1-1}}$ paired therewith.

As will be apparent from equations (1) and (2), the coupling noise generated in the
25 uppermost end data line DL_{1-1} is larger than that

generated in the data line $\overline{DL_{1-1}}$ paired therewith.

Consequently, the minute voltage difference between the data lines DL_{1-1} , $\overline{DL_{1-1}}$ decreases owing to the unbalance between the coupling noises.

This problem also occurs in the following cases:

(a) When the signal corresponding to the data "0" stored in a memory cell is read out to the lowermost end data line $\overline{DL_{1-n}}$ and

(b) When the signal corresponding to the data "1" stored in a memory cell is read out to the data line $\overline{DL_{1-1}}$ or DL_{1-n} .

A preferred embodiment of the present invention will now be described in greater detail with reference to Fig. 2A.

Sense amplifiers $SA_1, SA_2, \dots, SA_n$ are provided to pair data lines $DL_{1-1}, \overline{DL_{1-1}}; DL_{1-2}, \overline{DL_{1-2}}; \dots; DL_{1-n}, \overline{DL_{1-n}}$ respectively. Each of the data lines $DL_{1-1}, \overline{DL_{1-1}}, \dots, \overline{DL_{1-n}}$ is connected with the input/output terminals of memory cells M-CEL provided under a given matrix

and dummy cells D-CEL respectively. Moreover,
word lines WL_{1-1} , WL_{1-2} , ..., WL_{1-m} and dummy word
lines DWL_{1-1} , DWL_{1-2} are provided so as to cross
the data lines at right angles. Each of the word
5 and dummy word lines is connected with the
selection terminals of the memory cells M-CEL
provided under a given matrix and the dummy cells
D-CEL respectively. The pair data lines DL_{1-1} ,
 $\overline{DL_{1-1}}$; DL_{1-2} , $\overline{DL_{1-2}}$; ...; DL_{1-n} , $\overline{DL_{1-n}}$ are
10 connected with a pair of common data lines CDL_1 ,
 $\overline{CDL_1}$ through pairs of MISFETs Q_{11} , $\overline{Q_{11}}$; Q_{12} , $\overline{Q_{12}}$;
...; Q_{1n} , $\overline{Q_{1n}}$ for constituting a column switch
C-SW respectively. The common data lines CDL_1 ,
 $\overline{CDL_1}$ are connected with the input terminal of a
15 data output buffer DOB and the output terminal of
a data input buffer DIB respectively. The signal
transmission and reception between the D-RAM and
an external circuit, i.e., the transmission of the
read-out data and the data to be written is taken
20 place through the data output buffer DOB and the
data input buffer DIB.

A row-column decoder RC-DCR performs the
selecting operation for selecting a word line and
a dummy word line from the word lines WL_{1-1} ,
25 WL_{1-2} , ..., WL_{1-m} and the dummy word lines DWL_{1-1} ,

DWL₁₋₂. Moreover, the row-column decoder RC-DCR performs the selecting operation for selecting a pair of MISFETs from the pairs of MISFETs Q_{11} , $\overline{Q_{11}}$; Q_{12} , $\overline{Q_{12}}$; ...; Q_{1n} , $\overline{Q_{1n}}$.

5 An address buffer ADB processes two kinds of multiplexed external address signals, i.e., row address signals $A_0 \sim A_7$ and column address signals $A_8 \sim A_{15}$ processes into pairs of complementary address signals $(a_0, \overline{a_0}) \sim (a_7, \overline{a_7})$ and $(a_8, \overline{a_8}) \sim$
10 $(a_{15}, \overline{a_{15}})$ respectively and sends them to the row-column decoder RC-DCR at timings ϕ_{AR} , ϕ_{AC} in accordance with the operation in the IC chip.

The row-column decoder RC-DCR decodes the pairs of complementary address signals for
15 performing the above-mentioned selecting operation.

In the example, pairs of dummy data lines DDL₁₋₁, $\overline{DDL_{1-1}}$ and DDL₁₋₂, $\overline{DDL_{1-2}}$ are provided in order to eliminate the above-described nonuniformity
20 in the parasitic capacitance between the lines constituting a pair data line DL₁₋₁, $\overline{DL_{1-1}}$ arranged at the uppermost end of the memory array part M-ARY (or the dummy array part D-ARY) and between the lines constituting a pair data line
25 DL_{1-n}, $\overline{DL_{1-n}}$ arranged at the lowermost end

thereof.

The pair of dummy data lines DDL_{1-1} , $\overline{DDL_{1-1}}$ is provided above the uppermost pair data line DL_{1-1} , $\overline{DL_{1-n}}$ under the same arrangement as the other data lines.

On the other hand, the pair of dummy data lines DDL_{1-n} , $\overline{DDL_{1-n}}$ is provided below the lowermost end pair data line DL_{1-n} , $\overline{DL_{1-n}}$ under the same arrangement as the other data lines.

In order to make its parasitic capacitance C_o equal to that of the data lines DL_{1-1} , DL_{1-2} , ..., DL_{1-n} , each of these dummy data lines DDL_{1-1} , $\overline{DDL_{1-1}}$, DDL_{1-2} , $\overline{DDL_{1-2}}$ is connected with a plurality of memory cells M-CEL, a single dummy memory cell D-CEL, a dummy sense amplifier DSA_1 or DSA_2 and the corresponding one of MOS transistors Q_1 , $\overline{Q_1}$, Q_2 and $\overline{Q_2}$ for forming a column switch as shown in the figure.

The practical arrangement of each of the dummy sense amplifiers DSA_1 , DSA_2 is to be the same as the sense amplifiers SA_1 , SA_2 , ..., SA_n .

In addition, each of the word lines is formed so as to cross the dummy data lines in order to make the parasitic capacitance D_{dw} between a data line and a word line of each dummy data line equal

to that of the other data lines.

The pair of dummy data lines is provided in order to make the parasitic capacitance between data lines of the outermost data lines DL_{1-1} and $\overline{DL_{1-n}}$ respectively equal to that of the other data lines, i.e., $2C_{dd}$. Therefore, it is unnecessary to read out the data in a pair of dummy data lines. Accordingly, the pairs of MOS transistors $Q_1, \overline{Q_1}$ and $Q_2, \overline{Q_2}$ for forming a column switch connected with the pairs of dummy data lines $DDL_{1-1}, \overline{DDL_{1-1}}$ and $DDL_{1-2}, \overline{DDL_{1-2}}$ respectively are maintained in an OFF state.

Referring now to Figs. 2B and 2C, each of the 1-bit memory cells M-CEL comprises a capacitor C_S for storing data and a MISFET Q_M for the address selection. The data "1" or "0" is stored according to whether the capacitor C_S has an electric charge or not.

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Data is read out by turning ON the MISFET Q_M in order to connect the capacitor C_S to the data line DL_{1-1} and sensing the change in the potential of the data line DL_{1-1} with the amount of electric charge stored in the capacitor C_S . In the following description it will be assumed for the sake of clarity that each of the data lines has only the parasitic capacitance C_O . Supposing that the potential previously charged in the parasitic capacitance C_O of the data line DL_{1-1} is a supply voltage V_{CC} , when the data stored in the capacitor C_S is "1" (the potential of the supply voltage V_{CC}), the potential (V_{DL}) "1" of the data line DL_{1-1} is kept at the supply voltage V_{CC} in addressing and, on the other hand, when the data is "0" (0 V), the potential (V_{DL}) "0" becomes $\{C_O \cdot V_{CC} - C_S(V_W - V_{th})\} / C_O$, where V_W is the gate voltage of the MISFET Q_M , and V_{th} is the threshold voltage of the MISFET Q_M . Here, the difference between the logic "1" and the logic "0", i.e., the amount of the signal to be detected ΔV_S is as follows:

$$\Delta V_S = (V_{DL}) "1" - (V_{DL}) "0" = (V_W - V_{th}) \cdot C_S / C_O$$

If $V_W = V_{CC}$, the amount of the signal ΔV_S is as follows:

$$\Delta V_S = (V_{CC} - V_{th}) \cdot C_S / C_O$$

Since the memory cell is made smaller and a large number of memory cells are connected to each data line so as to form a memory matrix having a higher integration degree as well as a larger capacitance, $C_S \ll C_O$, i.e., C_S / C_O becomes an extremely small value. Consequently, ΔV_S is an extremely minute signal.

The dummy cells D-CEL are employed as references for detecting such minute signals. Each of the dummy cells D-CEL is manufactured under the same manufacturing conditions and with the same design constant as the memory cells M-CEL except for that the capacitance value of its capacitor C_{ds} is about the half of that of the capacitor C_S . The capacitor C_{ds} is discharged to earth potential by means of a MISFET Q_{D2} prior to addressing (the other electrode being fixed at the supply voltage V_{CC}). Therefore, the signal change quantity ΔV_R applied to the data line $\overline{DL}_{1-1}$ by the dummy cell in addressing is represented by the following equation similarly to the signal change quantity ΔV_S to the data line $\overline{DL}_{1-1}$ by the memory cell:

$$\Delta V_R = (V_{DW} - V_{th}) \cdot C_{ds} / C_O$$

where V_{DW} is the gate voltage of the MISFET Q_{D2} ,
and V_{th} is the threshold voltage of the MISFET
 Q_{D2} .

5 If $V_{DW} = V_{CC}$, ΔV_R is represented by the
following equation:

$$\Delta V_R = (V_{CC} - V_{th}) \cdot C_{ds} / C_O$$

Since C_{ds} is set so as to be almost half of
 C_S , ΔV_R is equal to almost half of ΔV_S .

10 Accordingly, it is possible to discriminate data
"1" and "0" according to whether the signal change
quantity ΔV_S of the data line DL_{1-1} is smaller or
larger than the signal change quantity ΔV_R of
the data line $\overline{DL}_{1-1}$.

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The sense amplifier SA_1 is to enlarge the
potential change difference produced in addressing
into a sense period determined by a timing signal
(sense amplifier control signal) ϕ_{PA} (the
operation thereof is described later) and has
input/output nodes connected with a pair of
complementary data lines DL_{1-1} , $\overline{DL}_{1-1}$ arranged in
parallel to each other. The numbers of the
memory cells connected to the data lines DL_{1-1} ,

25 $\overline{DL}_{1-1}$ respectively are made equal to each other in

order to increase the degree of detecting accuracy, and one dummy cell is connected to each of the data lines DL_{1-1} , $\overline{DL_{1-1}}$. Moreover, each memory cell M-CEL is connected between a word line and one of the pair of complementary data lines. Since each word line crosses both the lines constituting a pair data line, if the noise component generated in the word line is transmitted to a data line by means of an electrostatic coupling, the noise components equally appear on both the data lines and are cancelled out by the differential type sense amplifier SA_1 .

Particularly, the dummy data lines are provided in the example as described above.

Therefore, the parasitic capacitance between data lines of each data line is allowed to be $2C_{dd}$ with respect to all the data lines. Consequently, it is possible to equalize the coupling noise from a word line with the coupling noise resulting from the fluctuation in the substrate bias voltage $-V_{BB}$ with respect to all the data lines. Accordingly, each sense amplifier can reliably cancel out the coupling noises.

When the memory cell connected with one of the pair of complementary data lines DL_{1-1} , $\overline{DL_{1-1}}$

is selected, one of the pair of dummy word lines DWL_{1-1} , DWL_{1-2} is selected so that a dummy cell is inevitably connected to the other data line.

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The sense amplifier SA_1 has a pair of MISFETs Q_{S8} , Q_{S9} which are cross-linked and differentially amplifies a minute signal by the positive feedback operation thereof. The positive feedback

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operation is started at the same time when a MISFET Q_{S10} is made conductive in response to the timing signal (sense amplifier control signal)

ϕ_{PA} , and the higher data-line potential (V_H) lowers at a low speed and the lower data-line potential (V_L) lowers at a high speed while

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enlarging the difference therebetween according to the potential difference applied in addressing.

When the lower data-line potential V_L reaches a threshold voltage V_{th} of the cross-linked MISFETs, the positive feedback operation completes, so that the higher data-line potential V_H rests at a potential smaller than the supply voltage V_{CC} but larger than the threshold voltage V_{th} and the lower data-line potential V_L finally reaches 0 V.

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The stored data in a memory cell once
25 destroyed in addressing is restored (rewritten) by

receiving the higher data-line potential V_H or the lower data-line potential V_L obtained by the sensing operation as it is.

When the higher data-line potential V_H is reduced by more than a given amount with respect to the supply voltage V_{CC} , a malfunction takes place in that the state is read as the logic "0" while reading and rewriting are repeated certain times. An active restoring circuit AR_1 is provided in order to prevent a malfunction of this kind. The active restoring circuit AR_1 has the function to selectively boost only the higher data-line potential V_H to the supply voltage potential V_{CC} without exerting any effect on the lower data-line potential V_L . Each of MIS type variable capacitance elements C_{B11} and C_{B12} varies its electrostatic capacitance with the voltage applied to terminals on the left side as viewed in the figure. It will be appreciated that a capacitor is formed at a voltage higher than the threshold voltage V_{th} and no capacitor is formed at a voltage lower than that.

When MISFETs Q_{S4} , Q_{S5} are made conductive in response to a timing signal (active restoring control signal) ϕ_{rg} , the variable capacitance element C_B belonging to the data line at the potential V_H is charged. Next, when a timing signal (active restoring control signal) ϕ_{rs} is at a high level, the gate potential of a MISFET Q_{S6} or Q_{S7} belonging to the data line becomes sufficiently higher than the supply voltage V_{CC} , so that the potential V_H is restored to the supply voltage V_{CC} . In this case, the threshold voltages V_{th} of the MISFETs Q_{S6} , Q_{S7} are designed so as to be smaller than those of MISFETs not marked with * in the figure in order to decrease the power loss in the MISFETs Q_{S6} , Q_{S7} .

When a timing signal ϕ_{pc} is at a high level (higher than the supply voltage V_{CC}), MISFETs Q_{S2} , Q_{S3} are made conductive, the floating capacitance C_0 of each of the pair of complementary data lines DL_{1-1} , $\overline{DL_{1-1}}$ is precharged to the supply voltage V_{CC} . Since a MISFET Q_{S1} is made conductive simultaneously therewith, if there is unbalance between the precharging operations by the MISFETs Q_{S2} and Q_{S3} respectively, the pair of complementary data lines DL_{1-1} , $\overline{DL_{1-1}}$ are short-circuited with

each other so as to be set under the same potential condition. The threshold voltage V_{th} of each of the MISFETs Q_{S1} to Q_{S3} is set so as to be lower than that of the MISFETs not marked with * in the figure in order to prevent the production of the voltage loss between the source and drain thereof.

At this time, the MISFET Q_{d2} is made conductive in response to a timing signal (discharge control signal) ϕ_{dc} , and the dummy cell D-CEL is also reset in a given state.

Row address signals A_0 to A_i supplied from an address buffer ADB by means of a timing signal (address buffer control signal) ϕ_{AR} are decoded by a row-column decoder RC-DCR, and addressing of a memory cell M-CEL and a dummy cell D-CEL is started simultaneously with the rise of a word line control signal ϕ_X .

As a result, a voltage difference of almost $\Delta V_S/2$ is produced between the pair of complementary data lines DL_{1-1} , $\overline{DL_{1-1}}$ according to the stored content of the memory cell as described above.

At the same time when the MISFET Q_{S10} starts

conducting in response to the timing signal (sense amplifier control signal) ϕ_{PA} , the sense amplifier SA_1 starts the positive feedback operation and amplifies the detection signal of $\Delta V_S/2$ generated in addressing. After the amplifying operation is almost completed, the above-described active restoring circuit AR_1 restores the level of the logic "1" to the supply voltage V_{CC} in synchronism with the timing signal (active restoring control signal) ϕ_{rs} .

Column address signal A_{i+1} to A_j sent from the address buffer ADB in synchronism with a timing signal (address buffer control signal) ϕ_{AC} are decoded by the row-column decoder RC-DCR, and then the data stored in the memory cell M-CEL at the column address selected by a timing signal (column switch control signal) ϕ_Y is transmitted to common data lines CDL_1 , CDL_1 through a column switch C-SW.

Next, a main amplifier data output buffer OA&DOB is actuated in response to a timing signal (data output buffer and main amplifier control signal) ϕ_{OP} , so that the read stored data is sent out to an output terminal D_{out} of the chip. The

main amplifier data output buffer OA&DOB is made inoperative in response to a timing signal (data output buffer control signal) ϕ_{RW} in writing.

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Precharging, addressing and sensing operations are substantially the same as the above-described reading out operation. Consequently, the stored data in the memory cell to be essentially written is read out to the pair of complementary data lines DL_{1-1} , $\overline{DL_{1-1}}$ regardless of the logical value of an input write data D_{in} . Since the read out data is to be neglected by the writing operation described later, it may be considered that the operation so far is essentially the selection of a row address.

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The pair of data lines DL_{1-1} , $\overline{DL_{1-1}}$, located on the column selected in synchronism with the timing signal (column switch control signal) ϕ_Y similarly to the reading operation are connected to the common data lines CDL_1 , $\overline{CDL_1}$ respectively through the column switch C-SW.

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Next, complementary writing input signals d_{in} , $\overline{d_{in}}$ supplied from the data input buffer DIB

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in synchronism with the timing signal (data input buffer control signal) ϕ_{RW} are written in the memory cell M-CEL through the column switch C-SW. Although the sense amplifier SA_1 is also operative at this time, the data appearing on the pair of column data lines DL_{1-1} , $\overline{DL_{1-1}}$ is determined according to the data of the input signal D_{in} because the output impedance of the data input buffer DIB is low.

Refreshing is effected in such a way that the data stored in the memory cell M-CEL and being lost is once read out to a column common data line DL , and the read-out data is restored to a given level by means of the sense amplifier SA_1 as well as the active restoring circuit AR_1 and rewritten in the memory cell M-CEL. Accordingly, the refreshing operation is the same as the row addressing and sensing period operations described in connection with the reading out operation. In this case, however, the column switch C-SW is made inoperative, and refreshing is effected for all the columns simultaneously as well as row by row in order.

Referring now to the embodiment shown in Fig. 2D, it will be seen that unlike the example shown in Fig. 2A, each of the dummy data lines provided outside the outermost data lines DL_{1-1} , $\overline{DL_{1-n}}$ in the memory array part M-ARY (or the dummy array part D-ARY) comprises a single dummy data line (DDL_{1-1} , DDL_{1-2}). These dummy data lines DDL_{1-1} , DDL_{1-2} allow the composite capacitances between data lines of all the data lines DL_{1-1} , DL_{1-2} , ..., DL_{1-n} to be substantially equal to each other. In addition, similarly to the dummy data lines $\overline{DDL_{1-1}}$ and DDL_{1-2} shown in Fig. 2A, each of the above-mentioned dummy data lines DDL_{1-1} , DDL_{1-2} is connected with a plurality of memory cells M-CEL, a single dummy cell D-CEL and the corresponding one of MOS transistors Q_1 , Q_2 for forming a column switch as shown in the figure. Moreover, the dummy data lines DDL_{1-1} , DDL_{1-2} are connected with dummy sense amplifiers DSA'_1 , DSA'_2 each comprising a part of the circuit elements constituting a sense amplifier, as shown in the figure. Thus, the parasitic capacitance C_0 of each of the dummy data lines DDL_{1-1} , DDL_{1-2} is made equal to that of each of the data lines

$DL_{1-1}, DL_{1-2}, \dots, DL_{1-n}$.

The dummy data lines DDL_{1-1}, DDL_{1-2} are provided in order to allow the parasitic capacitance between data lines of each of the outermost data lines $DL_{1-1}, \overline{DL_{1-n}}$ to be equal to that of the other data lines, i.e. $2C_{dd}$. Therefore, it is unnecessary to read out signals from the dummy data lines DDL_{1-1}, DDL_{1-2} . Consequently, the dummy data lines are not connected to the common data lines $CDL_1, \overline{CDL_1}$.

Referring now to Fig. 2E it will be seen that the dummy sense amplifier DSA'_1 is composed of the circuit elements connected with a data line in the circuit elements constituting the differential type sense amplifier SA_1 . Consequently, the dummy sense amplifier DSA'_1 is composed of about half of the circuit elements constituting the differential sense amplifier SA'_1 .

Since the operation of the circuit of this

example is the same as described with reference to Fig. 2B and Fig. 2C, the description thereof is omitted.

Fig. 3A is a circuit diagram of the D-RAM having about 64 Kbit-memory cells arranged separately in two memory cell matrixes (memory arrays M-ARY₁, M-ARY₂) each having a memory capacity of 128 rows X 256 columns=32,768 bits (32 Kbits). Principal blocks in the figure are drawn in accordance with the actual geometric arrangement.

Decoding output signals of $2^7=128$ kinds obtained according to row addressing signals $A_0 \sim A_6$ are applied to address selecting lines (word lines WL) in the row system of each of the memory arrays M-ARY₁, M-ARY₂ from row decoders (serving also as word drivers) R-DCR₁, R-DCR₂ respectively.

A column decoder C-DCR provides decoding output signals of 128 kinds according to column address signals $A_9 \sim A_{15}$. The column selecting decoding output signals are common to the right and left memory arrays as well as the upper and lower adjacent columns in each of the memory arrays, i.e., four columns in total.

The address signals A_7 and A_8 are allotted in

order to select one of these four columns. For instance, the address signal A_7 is allotted for selecting one of the right and left columns, while the address signal A_8 is allotted for selecting one of the upper and lower columns.

A ϕ_{yij} signal generating circuit ϕ_{yij} -SG decodes data into four kinds of combination according to the address signals A_7 , A_8 . Column switch selectors $CSW-S_1$, $CSW-S_2$ change over the columns according to output signals ϕ_{y00} , ϕ_{y01} , ϕ_{y10} , ϕ_{y11} of the ϕ_{yij} signal generating circuit ϕ_{yij} -SG.

Thus, the decoder for selecting the columns of the memory arrays is divided into two stages: the column decoder C-DCR and the column switch selectors $CSW-S_1$, $CSW-S_2$. The division of the decoder into two stages aims first to prevent

the production of any wasteful space in the IC chip. In other words, it aims at coincidence between the longitudinal arrangement pitch of NOR gates having a relatively large area for carrying a pair of right and left output signal lines of the column decoder C-DCR and the memory cell column arrangement pitch. Namely, the division

of the decoder into two stages allows reduction in

the number of transistors needed for constituting the NOR gates, so that the area occupied thereby can be made smaller.

5 The second aim in dividing the decoder into two stages is to decrease the load on each address signal line and improve the switching speed by reducing the number of the NOR gates connected to one address signal line.

10 The address buffer ADB process the multiplexed eight external address signals $A_0 \sim A_7$; $A_8 \sim A_{15}$ into eight kinds of pairs of complementary address signals $(a_0, \overline{a_0}) \sim (a_7, \overline{a_7})$; $(a_8, \overline{a_8}) \sim (a_{15}, \overline{a_{15}})$ respectively and transmits them to the decoder circuit at the timings ϕ_{AR} , ϕ_{AC} synchronized with
15 the operation inside the IC chip.

 In the preferred embodiment, dummy data lines DDL_{1-1} , DDL_{1-2} , DDL_{2-1} , DDL_{2-2} are provided at the outermost parts of the memory arrays $M-ARY_1$ and $M-ARY_2$, i.e., the uppermost parts and the
20 lowermost parts thereof respectively. In addition, MOS transistors Q_1 , Q_2 , Q_3 , Q_4 for forming column switches and dummy sense amplifiers DSA'_1 , DSA'_2 , DSA'_3 , DSA'_4 are provided so as to correspond thereto respectively.

25 The circuit operation in the address setting

process in the 2-mat system 64 K-D-RAM will be now be described with reference to Fig. 3A and Fig. 3B.

5 First, when the address buffer control signal ϕ_{AR} of the row system rises to a high level, 7 kinds of pairs of complementary two address signals $(a_0, \overline{a_0}) \sim (a_6, \overline{a_6})$ corresponding to the row address signals $A_0 \sim A_6$ are applied to the row decoders R-DCR₁, R-DCR₂ from the address buffer ADB through a row address line R-ADL.

10 Next, when the word line control signal ϕ_X rises to a high level, the row decoders R-DCR₁, R-DCR₂ are made active, and one of the word lines in each of the memory arrays M-ARY₁, M-ARY₂ is selected and made to be a high level.

15 Next, when the address buffer control signal ϕ_{AC} of the column system rises to a high level, 7 kinds of pairs of complementary column address signals $(a_9, \overline{a_9}) \sim (a_{15}, \overline{a_{15}})$ corresponding to the column address signals $A_9 \sim A_{15}$ are applied to the column decoder C-DCR from the address buffer ADB through the column address line C-ADL.

20 As a result, one of 128 pairs of output signal lines of the column decoder C-DCR is made to be a high level, and the high-level signal is

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applied to the column switch selectors CSW-S₁,
CSW-S₂.

Next, when the column switch control signal ϕ_Y rises to a high level, the ϕ_{Yij} signal
5 generating circuit ϕ_{Yij} -SG is made operative.

On the other hand, the pair of complementary signals (a_7 , $\bar{a}_7$) corresponding to the address
signal A₇ is previously applied to the ϕ_{Yij} signal
generating circuit ϕ_{Yij} -SG when the address buffer
10 control signal ϕ_{AR} becomes a high level, while the
pair of complementary signals (a_8 , $\bar{a}_8$) corresponding
to the address signal A₈ is previously applied to
the ϕ_{Yij} signal generating circuit ϕ_{Yij} -SG when
the address buffer control signal ϕ_{AC} becomes a
15 high level. Consequently, when the column switch
control signal ϕ_Y becomes a high level, almost
simultaneously therewith, the ϕ_{Yij} signal
generating circuit ϕ_{Yij} -SG transmits a signal to
each of the column switch selectors CSW-S₁,

20 CSW-S₂.

Thus, one pair is selected from a total of
512 pairs of transistors in the column switches
C-SW₁, C-SW₂, and one pair of data lines DL in the
memory array is connected to the common data line
25 CDL.

The memory array M-ARY shown in Fig. 4A has a plurality of memory cells M-CEL arranged on a semiconductor substrate 1, while the dummy array D-ARY shown in Fig. 4A has a plurality of dummy cells D-CEL arranged on the semiconductor substrate 1.

The memory array M-ARY shown in Fig. 4A is arranged as follows. A field insulating film 2 having a basic pattern shown in Fig. 5 is formed on the surface of the semiconductor substrate 1 in order to separate the memory cells M-CEL from each other, each memory cell comprising a MISFET Q_M and a capacitor C_S for storage.

Unlike the field insulating film 2 following the basic pattern rule, a field insulating film 2a is arranged underneath a contact hole CH_0 for applying the supply voltage V_{CC} to a first polycrystalline silicon layer 6. Accordingly, it is possible to prevent occurrence of such an accident that the aluminium silicon alloy formed according to the interaction between

an aluminium layer and the polycrystalline silicon layer near the contact hole CH_0 penetrates through the insulating film underneath the contact hole CH_0 to undesirably reach the surface of the semiconductor substrate 1.

The first polycrystalline silicon layer 6 employed as one of electrodes of the storage capacitor C_S in each memory cell M-CEL is formed having a basic pattern shown in Fig. 6 on the field insulating film 2 and a gate insulating film 3.

Moreover, the word lines $WL_{1-1} \sim WL_{1-6}$ formed from a second polycrystalline silicon layer 8 extend over the first polycrystalline silicon layer 6 in the vertical direction as viewed in Fig. 4A.

In addition, a power supply line V_{CC-L} for supplying the supply voltage V_{CC} to the polycrystalline silicon layer 6 as one electrode of the storage capacitor C_S extends in the horizontal direction as viewed in Fig. 4A.

On the other hand, the dummy data lines DDL_{1-1} , $\overline{DDL_{1-1}}$ and the data lines DL_{1-1} , $\overline{DL_{1-1}}$ formed from the aluminium layer 10 extend in substantially parallel with the power supply line

V_{CC-L} as shown in Fig. 4A. The dummy data line DDL_{1-1} is connected to the drain region of the MISFET Q_m in the memory cell M-CEL through a contact hole CH_1 , while the dummy data line $\overline{DDL}_{1-1}$ is connected to the drain region of the MISFET Q_M in another memory cell M-CEL through a contact hole CH_2 . Moreover, each of the data lines DL_{1-1} , $\overline{DL}_{1-1}$ extends in the horizontal direction as viewed in Fig. 4A similarly to the dummy data lines DDL_{1-1} , $\overline{DDL}_{1-1}$ and is connected to the drain region of the MISFET Q_M in a memory cell through a contact hole at a given portion.

The dummy cell D-CEL shown in Fig. 4A is arranged as follows. The field insulating film 2 is formed on one part of the surface of the semiconductor substrate 1, while the gate insulating film 3 is formed on the other part of the surface of the semiconductor substrate 1.

On the field insulating film 2 and the gate insulating film 3, first polycrystalline silicon layers $15a$, $15b$ extend separately from each other in the vertical direction as viewed in Fig. 4A. The width of each of the first polycrystalline silicon layers $15a$, $15b$ is extremely important for

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determining the value of the capacitance of the capacitor C_{ds} in each dummy cell D-CEL. An N^+ type semiconductor region 14 is located between the first polycrystalline silicon layers 15a and 15b and employed as an earth line common to the dummy cells D-CEL.

Moreover, the dummy word line DWL_{1-1} formed from a second polycrystalline silicon layer extends over the first polycrystalline silicon layer 15a. The dummy word line DWL_{1-1} constitutes the gate electrode of a MISFET Q_{D1} of each dummy cell D-CEL. On the other hand, a control signal line ϕ_{dc-L1} formed from the second polycrystalline silicon layer for applying the discharging control signal ϕ_{dc} shown in Fig. 2B is separated from the dummy word line DWL_{1-1} while extending in parallel therewith. The control signal line ϕ_{dc-L1} constitutes the gate electrode of a MISFET Q_{D2} in each dummy cell D-CEL.

Similarly, a dummy word line DWL_{1-2} and a control signal line ϕ_{dc-L2} extend in parallel with the dummy word line DWL_{1-1} and the control signal line ϕ_{dc-L1} .

Moreover, dummy data lines DDL_{1-1} , $\overline{DDL_{1-1}}$ and data lines DL_{1-1} , $\overline{DL_{1-1}}$ extend from the memory

array M-ARY as shown in Fig. 4A. The dummy data line $\overline{DDL}_{1-1}$ is connected to the drain region of the MISFET Q_{D1} of the dummy cell D-CEL through a contact hole CH_3 and, similarly, the data line 5 DL_{1-1} is connected to the drain region of the MISFET Q_{D1} in another dummy cell D-CEL through a contact hole CH_4 .

In Fig. 4B, the circuit includes an active restoring section AR, and a data line 10 precharging circuit section PC.

The active restoring section AR has two active restoring circuits AR_1 shown in Fig. 2B. In other words, one active restoring circuit is constituted on the side of an arrow A shown in 15 Fig. 4B, and the other active restoring circuit is constituted on the side of an arrow B. In the active restoring section AR, active restoring control signal lines ϕ_{rg-L} , ϕ_{rs-L} and a power supply line V_{CC-L} common to both the active 20 restoring circuits are arranged as shown in Fig. 4B.

On the other hand, the precharging circuit section PC has two data line precharging circuits arranged corresponding to the two active restoring circuits. In the precharging circuit section PC, a potential line V_{DP-L} , a precharging control signal line ϕ_{PC-L} and dummy data lines DDL_{1-1} , $\overline{DDL_{1-1}}$ as well as data lines DL_{1-1} , $\overline{DL_{1-1}}$ extending to the memory array M-ARY shown in Fig. 4A are arranged as shown in Fig. 4B.

10 The MISFETs $Q_{S1} \sim Q_{S7}$ and the capacitors C_{B11} , C_{B12} in Fig. 2B are arranged as shown in Fig. 4B.

Fig. 7 shows sectional views of the IC structure taken along lines X_2-X_2 , X_3-X_3 shown in 15 the layout pattern respectively.

The basic layout in the example shown in Fig. 4C is the same as shown in Fig. 4A. In the example shown in Fig. 2D and Fig. 2E, however, the data line DL_{1-1} is arranged in the second line since 20 the dummy data line DDL_{1-1} is constituted by a single dummy data line.

Fig. 4D shows a layout pattern of a part of a peripheral circuit, e.g. the dummy sense amplifier DSA'_1 and the sense amplifier SA_1 shown in Fig. 2E. In this example, since the dummy data line is constituted by a single line similarly to the dummy data line DDL_{1-1} , the active restoring section AR and the precharging circuit section PC of the dummy sense amplifier DSA'_1 are reduced, so that the area occupied thereby is smaller as compared with the layout shown in Fig. 4B or the sense amplifier SA_1 shown in the same figure. Except for this, the layout is basically similar to the layout shown in Fig. 4B.

The composite parasitic capacitances between data lines of all the data lines can be made equal to each other, i.e. $2C_{dd}$, because the dummy data lines are provided outside the outermost data lines DL_{1-1} , $\overline{DL_{1-n}}$ respectively. Accordingly, the coupling noises from a word line and a dummy word line and the coupling noises resulting from the fluctuation in the substrate

bias voltage - V_{BB} are equally generated in the lines constituting a pair data line (DL_{1-1} , $\overline{DL_{1-1}}$), so that they can be canceled out by means of a differential type sense amplifier (SA_1).

5 Thus, since the minute voltage difference fed to the sense amplifier (SA_1) is not affected by the coupling noises, it is possible to prevent malfunction of the sense amplifier (SA_1) and enlarge the input level margin.

10 Moreover, in case of enlarging the memory capacity to, e.g., 1 M bits, the application of the present invention prevents appearance of the above-described adverse effects even if the distance between adjacent data lines is made as
15 small as possible and the capacitance value of the parasitic capacitance C_{dd} between data lines is enlarged. Accordingly, the technical idea of the present invention is indispensable for a memory array of high density, i.e., for enlarging the
20 memory capacity.

 The arrangement of the memory array may be modified in a variety of forms besides the above-described 2-mat system, such as the 8-mat

system wherein a memory cell of about 64 K bits is divided into 8 memory arrays $M-ARY_{1\sim 8}$ each having a memory capacity of 128 rows $\times$ 54 columns = 8192 bits (8 K bits).

5 Moreover, the parasitic capacitance C_0 of the dummy data line may be replaced by capacitance means equivalent to the above-described memory cells, dummy cell and dummy sense amplifier.

10 The invention can be applied to such a dynamic RAM as having redundancy memory cells. The redundancy memory cells are connected to, e.g., each line of an additional pair data line. The pair data line is further connected with dummy cells and a sense amplifier. Consequently, the

15 redundancy memory cells, the additional pair data line, the dummy cells and the sense amplifier are arranged similarly to, e.g., the pair data line DL_{1-1} , $\overline{DL_{1-1}}$ shown in Fig. 2A and the memory cells, the dummy cells and the sense amplifier SA_1

20 which are connected therewith. The additional pair data line and the like are arranged at an end part of a memory array, for example. The additional pair data line is connected to common data lines (CDL_1 , $\overline{CDL_1}$) through redundancy column

25 switch MISFETs arranged similarly to the column

switch MISFETs Q_{11} , shown in Fig. 2A. A redundancy address decoder is provided for the switching control of the redundancy column switch MISFETs. Thereby, if there is a pair data line connected with a defective memory cell or there is a defective pair data line, the pair data line is replaced with the additional pair data line. In other words, when an address signal represents the defective pair data line, the additional pair data line is accessed.

When the additional pair data line is arranged at an end part of the memory array, there is possibility that unbalanced coupling noises are applied to the lines constituting the additional pair data line respectively. Dummy data lines and dummy sense amplifiers arranged similarly to the above-described examples can be arranged in order to balance the coupling noises with each other.

Moreover, in case of providing a plurality of additional pair data lines, i.e., a plurality of pair data lines for redressing defects, it is possible take such an arrangement that one of the additional pair data lines other than the additional pair data lines arranged at the

outermost ends of the memory array respectively is preferentially selected to replace a defective pair data line. In this case, each of the pair data lines arranged at the outermost ends of the memory array
5 respectively has the function similar to that of the dummy data lines in the above-described examples if it does not replace the defective pair data line by the address changing operation for redressing defects.

10 Attention is drawn to Application No. 85.05714 (Serial No. 2155239) which has been divided out of the present Application.



CLAIMS.

1. A dynamic RAM integrated circuit device having a folded bit line arrangement including:

(a) a memory array having a plurality of pair data lines formed on a semiconductor substrate, a plurality of memory cells connected with the corresponding one of said plurality of pair data lines and a plurality of word lines each connected with the corresponding ones of said plurality of memory cells; and

(b) an additional compensating data line formed on said semiconductor substrate so as to extend close to as well as in parallel with a pair data line in said plurality of pair data lines arranged in an end of said memory array, in order to decrease the difference between the stray capacitances connected to the lines constituting said pair data line arranged at an end of said memory array respectively.

2. A dynamic RAM integrated circuit device, according to claim 1, wherein said additional data line is formed from the same wiring layer as each of said plurality of pair data lines.

3. A dynamic RAM integrated circuit device according to claim 1, wherein each of said plurality of word lines crosses each of said plurality of pair data lines and said additional data line.



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4. A dynamic RAM integrated circuit device according to claim 1, wherein said additional data line is connected with one terminals of the corresponding ones of said plurality of memory cells having the other terminals connected with the corresponding ones of said plurality of word lines.
5. A dynamic RAM integrated circuit device according to claim 1 wherein the distance between said additional data line and the data line arranged at an end part of said memory array is made substantially equal to that between the data lines constituting one of said plurality of pair data lines.
6. A dynamic RAM integrated circuit device according to claim 1 wherein said additional data line is connected with circuit elements substantially equivalent to those connected to each data line of said plurality of pair data lines, in order to allow the parasitic capacitance connected to said additional data line to be substantially equal to that connected to each data line of said plurality of pair data lines.
7. A dynamic RAM integrated circuit device according to claim 6 wherein said circuit elements connected to said additional data line include circuit elements equivalent to those constituting a sense



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amplifier connected to each of said plurality of pair data lines and a transistor equivalent to that for forming a column switch for selecting one data line from said plurality of pair data lines.

5 8. A dynamic RAM integrated circuit device according to any one of the preceding claims 1 to 4, wherein said additional data line is a pair additional data line formed on said semiconductor substrate so as to extend adjacently to each other as well
10 as in parallel with each other.

9. A dynamic RAM integrated circuit device according to claim 8 wherein the distance between the additional data lines constituting said pair additional data line is made substantially equal
15 to that between the data lines constituting each of said plurality of pair data lines and the distance between the data line arranged at an end part of said memory array and one of the additional data lines constituting said pair additional data line
20 arranged adjacently thereto is made substantially equal to that between the adjacent ones of said plurality of pair data lines.

10. A dynamic RAM integrated circuit device according to claim 9 wherein each of the additional
25 data lines constituting said pair additional data



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line is connected with circuit elements substantially equivalent to those connected to each data line of said plurality of pair data lines, in order to allow the parasitic capacitance connected to each of the
5 additional data lines constituting said pair additional data line to be substantially equal to that connected to each data line of said plurality of pair data lines.

11. A dynamic RAM integrated circuit device
10 constructed substantially as herein described with reference to and as illustrated in Figures 2 to 7 of the accompanying drawings.
