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(54) **Title**: SELECTIVE GERMANIUM P-CONTACT METALIZATION THROUGH TRENCH

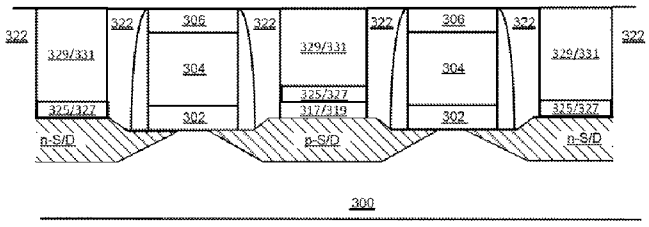


FIG. 5F

(57) **Abstract**: Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on, for example, silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in Sight of this disclosure, including both planar and non-planar transistor structures {e.g., FinFETs), as well as strained and unstrained channel structures. Graded buffering can be used to reduce misfit dislocation. The techniques are particularly well-suited for implementing p-type de vices, but can be used for n-type de vices if so desired.

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