

INTEGRATED CIRCUIT DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application claims the benefit of and priority to Korean Patent Application No. 10-2019-0107645, filed on August 30, 2019, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

TECHNICAL FIELD

[0002] The inventive concepts relate to integrated circuit devices, and more particularly, to integrated circuit devices including a nonvolatile memory device having a cell over periphery (COP) structure.

BACKGROUND

[0003] In accordance with the multi-functionalization of information communication apparatuses, integrated circuit devices including memory devices have become mass storage and highly integrated, and thus sizes of memory cells have gradually reduced and operation circuits and interconnection structures included in the memory devices for the operation and electrical connection of the memory devices are becoming more complicated. Accordingly, there is a need for an integrated circuit device including a memory device having a structure with excellent electrical characteristics while improving the degree of integration.

SUMMARY

[0004] The inventive concepts provide an integrated circuit device having a structure capable of improving the reliability of an interconnection structure with improved integration and reduced chip size.

[0005] According to some aspects of the inventive concepts, there is provided an integrated circuit device including: a memory including a memory stack unit, a memory cell interconnection including a plurality of upper conductive patterns configured to be electrically connectable to the memory stack unit, and a memory cell insulation surrounding the memory stack and the memory cell interconnection unit; a peripheral circuit including a peripheral circuit board, a peripheral circuit region on the peripheral circuit board, and a peripheral circuit interconnection including a plurality of lower conductive patterns between the peripheral circuit region and the memory and bonded to the memory cell

interconnection unit; a plurality of conductive bonding structures on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in a vertical direction, the plurality of conductive bonding structures being a bonded resultant of a plurality of first upper conductive patterns selected from among the plurality of upper conductive patterns and a respective plurality of first lower conductive patterns selected from among the plurality of lower conductive patterns; and a through electrode penetrating one of the memory cell insulation and the peripheral circuit board and extended to a second lower conductive pattern selected from among the plurality of lower conductive patterns in the vertical direction, in a second region, the second region overlapping the memory cell insulation in the vertical direction.

[0006] According to an aspect of the inventive concept, there is provided an integrated circuit device including: a memory including a memory stack including a plurality of bit lines extending in a first horizontal direction, a memory cell interconnection including a plurality of upper conductive patterns configured to be electrically connectable to the plurality of bit lines, and a memory cell insulation surrounding the memory stack and the memory cell interconnection unit; a peripheral circuit including a peripheral circuit board, a peripheral circuit region on the peripheral circuit board, and a peripheral circuit interconnection including a plurality of lower conductive patterns between the peripheral circuit region and the memory and bonded to the memory cell interconnection unit; a conductive bonding on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in a vertical direction, the conductive bonding being a bonded resultant of a first upper conductive pattern selected from among the plurality of upper conductive patterns and a first lower conductive pattern selected from among the plurality of lower conductive patterns; and a plurality of through electrodes extended in the vertical direction through one of the memory cell insulation and the peripheral circuit board, in a second region spaced apart from the first region in a horizontal direction, wherein the plurality of through electrodes include a plurality of first through electrodes arranged in a line along the first horizontal direction in the second region.

[0007] According to an aspect of the inventive concept, there is provided an integrated circuit device including: a memory including a semiconductor layer, a memory stack on the semiconductor layer, a memory cell interconnection including a plurality of upper

conductive patterns overlapping the memory stack in a vertical direction and configured to be electrically connectable to the memory stack unit, and a memory cell insulation surrounding the semiconductor layer, the memory stack and the memory cell interconnection unit; a peripheral circuit including a peripheral circuit board, a peripheral circuit region on the peripheral circuit board, and a peripheral circuit interconnection between the peripheral circuit region and the memory and bonded to the memory cell interconnection unit; a plurality of conductive bonding structures including Cu and on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in the vertical direction; a plurality of lower conductive patterns including at least one metal selected from among Al, W, and Cu and in the peripheral circuit interconnection in a second region, the second region overlapping the memory cell insulation in the vertical direction; and a through electrode penetrating one of the memory cell insulation and the peripheral circuit board in the second region and contacting one lower conductive pattern among the plurality of lower conductive patterns.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments of the inventive concepts will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] FIG. 1 is a block diagram of an integrated circuit device according to example embodiments of the inventive concepts;

[0010] FIG. 2 is a perspective view illustrating a schematic structure of an integrated circuit device according to example embodiments of the inventive concepts;

[0011] FIG. 3 is a perspective view illustrating a schematic structure of an integrated circuit device according to example embodiments of the inventive concepts;

[0012] FIG. 4A is a plan view illustrating an example structure of some components of a memory cell array that may be included in an integrated circuit device according to example embodiments of the inventive concepts, and FIG. 4B is a cross-sectional view showing some components of cross sections taken along lines A1-A1' and A2-A2' of FIG. 4A;

[0013] FIGS. 5A and 5B are exploded plan views respectively illustrating some components of an integrated circuit device according to example embodiments of the inventive concepts;

[0014] FIGS. 6 to 13 are cross-sectional views illustrating an integrated circuit devices according to example embodiments of the inventive concepts;

[0015] FIGS. 14A and 14B are exploded plan views respectively illustrating some components of an integrated circuit device according to example embodiments of the inventive concepts;

[0016] FIGS. 15 to 18 are cross-sectional views illustrating an integrated circuit devices according to example embodiments of the inventive concepts;

[0017] FIGS. 19A to 19D are cross-sectional views illustrating a method of manufacturing an integrated circuit device in the order of process, according to example embodiments of the inventive concepts; and

[0018] FIGS. 20A to 20C are cross-sectional views illustrating a method of manufacturing an integrated circuit device in the order of process, according to example embodiments of the inventive concepts.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0019] Hereinafter, example embodiments of the inventive concepts will be described in detail with reference to the accompanying drawings. The same reference numerals are used for the same elements in the drawings, and redundant description thereof will be omitted.

[0020] FIG. 1 is a block diagram of an integrated circuit device 10 according to example embodiments of the inventive concepts.

[0021] Referring to FIG. 1, the integrated circuit device 10 may include a memory cell array 20 and a peripheral circuit 30. The memory cell array 20 may include a plurality of memory cell blocks BLK1, BLK2, ..., and BLKn. Each of the plurality of memory cell blocks BLK1, BLK2, ..., and BLKn may include a plurality of memory cells. The memory cell blocks BLK1, BLK2,..., and BLKn may be connected to the peripheral circuit 30 through a bit line BL, a word line WL, a string select line SSL, and a ground select line GSL.

[0022] The peripheral circuit 30 may include a row decoder 32, a page buffer 34, a data input/output circuit 36, and a control logic 38. Although not shown in FIG. 1, the peripheral circuit 30 may further include an input/output interface, a column logic, a voltage generator, a pre-decoder, a temperature sensor, a command decoder, an address decoder, and the like.

[0023] The peripheral circuit 30 (as well as other elements and/or sub-elements, such as the row decoder 32, page buffer 34, data input/output circuit 36, and control logic 38) may

include processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof. For example, the processing circuitry more specifically may include, but is not limited to, a central processing unit (CPU) , an arithmetic logic unit (ALU), a digital signal processor, a microcomputer, a field programmable gate array (FPGA), a System-on-Chip (SoC), a programmable logic unit, a microprocessor, application-specific integrated circuit (ASIC), etc.

[0024] The memory cell array 20 may be connected to the page buffer 34 through the bit line BL and may be connected to the row decoder 32 through the word line WL, the string select line SSL, and the ground select line GSL. In the memory cell array 20, the plurality of memory cells included in the plurality of memory cell blocks BLK1, BLK2, ..., and BLKn may be flash memory cells, respectively. The memory cell array 20 may include a three dimensional memory cell array. The three dimensional memory cell array may include a plurality of NAND strings, and each of the NAND strings may include memory cells respectively connected to a plurality of word lines WL vertically stacked on a substrate. In example embodiments, the memory cell array 20 may include a memory stack MS described below with reference to FIGS. 4A and 4B.

[0025] The peripheral circuit 30 may receive an address ADDR, a command CMD, and a control signal CTRL from the outside of the integrated circuit device 10, and may transmit and receive data DATA to and from an apparatus outside the integrated circuit device 10.

[0026] The row decoder 32 may select at least one of the plurality of memory cell blocks BLK1, BLK2,..., and BLKn in response to an address ADDR from the outside and may select the word line WL, the string select line SSL, and the ground select line GSL of the selected memory cell block. The row decoder 32 may transmit a voltage for performing a memory operation to the word line WL of the selected memory cell block.

[0027] The page buffer 34 may be connected to the memory cell array 20 through the bit line BL. The page buffer 34 may operate as a write driver in a program operation and thus apply a voltage corresponding to the data DATA to be stored in the memory cell array 20 to the bit line BL and may operate as a sense amplifier in a read operation and thus sense the data DATA stored in the memory cell array 20. The page buffer 34 may operate according to a control signal PCTL to be provided from the control logic 38.

[0028] The data input/output circuit 36 may be connected to the page buffer 34 through data lines DLs. The data input/output circuit 36 may receive the data DATA from a memory

controller (not shown) in the program operation and may provide program data DATA to the page buffer 34 based on a column address C_ADDR to be provided from the control logic 38. The data input/output circuit 36 may provide read data DATA stored in the page buffer 34 to the memory controller, based on the column address C_ADDR to be provided from the control logic 38 in the read operation.

[0029] The data input/output circuit 36 may transmit an input address or command to the control logic 38 or the row decoder 32. The peripheral circuit 30 of the integrated circuit device 10 may further include an electrostatic discharge (ESD) circuit and a pull-up/pull-down driver.

[0030] The control logic 38 may receive the command CMD and the control signal CTRL from the memory controller. The control logic 38 may provide a row address R_ADDR to the row decoder 32 and may provide the column address C_ADDR to the data input/output circuit 36. The control logic 38 may generate various internal control signals to be used in the integrated circuit device 10 in response to the control signal CTRL. For example, the control logic 38 may adjust voltage levels to be provided to the word line WL and the bit line BL when performing a memory operation such as a program operation or an erase operation.

[0031] FIG. 2 is a perspective view illustrating a schematic structure of an integrated circuit device 100 according to example embodiments of the inventive concepts. The integrated circuit device 100 may be a specific implementation of some of the example embodiments of the integrated circuit device 10 illustrated in FIG. 1.

[0032] Referring to FIG. 2, the integrated circuit device 100 may include a memory structure MST and a peripheral circuit structure PST overlapping each other in a vertical direction (a Z direction).

[0033] The memory structure MST may include a memory stack unit MSP including a memory cell array 20 (see FIG. 1), a memory cell interconnection unit C60 configured to be electrically connected to the memory stack unit MSP, and a memory cell insulation unit C70 surrounding the memory stack unit MSP and the memory cell interconnection unit C60. The memory cell insulation unit C70 may be disposed to surround at least two sides of the memory stack unit MSP at a position vertically overlapping with the peripheral circuit structure PST. FIG. 2 illustrates that the memory cell insulation unit C70 may have a ring shape surrounding four sides of the memory stack unit MSP such that the memory cell insulation unit C70 covers both sides in an X direction and both sides in a Y direction of the

memory stack unit MSP, but the inventive concepts are not limited to the illustration in FIG. 2. The memory cell insulation unit C70 may be arranged to surround at least one of both sides of the X direction and at least one of both sides of the Y direction of the memory stack unit MSP.

[0034] The peripheral circuit structure PST may include a peripheral circuit board SUB, a peripheral circuit region P30 and a peripheral circuit interconnection part P80 sequentially formed on the peripheral circuit board SUB. The peripheral circuit region P30 may include the peripheral circuit 30 described with reference to FIG. 1. The peripheral circuit interconnection unit P80 may be configured to be electrically connected to the peripheral circuit 30 included in the peripheral circuit board SUB and the peripheral circuit region P30. The peripheral circuit region P30 may be spaced apart from the memory stack unit MSP in the vertical direction (the Z direction) with the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 therebetween.

[0035] The integrated circuit device 100 may have a cell over periphery (COP) structure in which the memory structure MST may be disposed on the peripheral circuit structure PST, thereby reducing a horizontal area of the integrated circuit device 100 and improving the degree of integration.

[0036] Each of the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 may include a plurality of conductive patterns and a plurality of contact plugs for interconnecting two conductive patterns adjacent in the vertical direction among the plurality of conductive patterns (not illustrated). The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 may be in contact with each other by bonding. The plurality of conductive patterns of each of the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 may include a plurality of conductive bonding patterns for mutually bonding the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 (not illustrated). A plurality of conductive bonding structures, which are a result obtained by bonding the conductive bonding pattern included in the memory cell interconnection unit C60 and the conductive bonding pattern included in the peripheral circuit interconnection unit P80, may be arranged along a boundary between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80. The conductive bonding structure may not be disposed at a boundary between the memory cell insulation unit C70 and the peripheral circuit interconnection unit P80.

[0037] The integrated circuit device 100 may include a plurality of through electrodes THV penetrating the memory cell insulation unit C70 in the vertical direction. Each of the plurality of through electrodes THV may include a first portion THVA penetrating the memory cell insulation unit C70 and a second portion THVB penetrating a portion of the peripheral circuit interconnection unit P80. Each of the plurality of through electrodes THV may be connected to at least one conductive pattern selected from among a plurality of conductive patterns included in the peripheral circuit interconnection unit P80 and may be connected to the peripheral circuit 30 (see FIG. 1) in the peripheral circuit region P30 through the at least one conductive pattern.

[0038] There may not be a conductive bonding structure, which is a result obtained by bonding the conductive bonding pattern included in the memory cell interconnection unit C60 to the conductive bonding pattern included in the peripheral circuit interconnection unit P80, in an electrical connection path between the plurality of through electrodes THV and the peripheral circuit 30 (see FIG. 1) in the peripheral circuit region P30. Therefore, it may be possible to prevent or reduce the increase in resistance due to the conductive bonding structure in the electrical connection path between the plurality of through electrodes THV and the peripheral circuit 30 (see FIG. 1) in the peripheral circuit region P30.

[0039] FIG. 3 is a perspective view illustrating a schematic structure of an integrated circuit device 200 according to example embodiments of the inventive concepts. The integrated circuit device 200 may be another specific implementation of some of the example embodiments of the integrated circuit device 10 illustrated in FIG. 1.

[0040] Referring to FIG. 3, the integrated circuit device 200 may have substantially the same configuration as the integrated circuit device 100 illustrated in FIG. 2. However, the integrated circuit device 200 may include a plurality of through electrodes TSV instead of the plurality of through electrodes THV illustrated in FIG. 2. The plurality of through electrodes TSV may not penetrate the memory structure MST, but may penetrate only the peripheral circuit structure PST. The plurality of through electrodes TSV may be disposed at positions overlapping the memory cell insulation C70 in the peripheral circuit structure PST. Each of the plurality of through electrodes TSV may include a first portion TSVA penetrating the peripheral circuit board SUB, a second portion TSVB penetrating the peripheral circuit region P30, and a third portion TSVC penetrating a portion of the peripheral circuit interconnection unit P80. In example embodiments, each of the plurality of through electrodes TSV may be connected to at least one conductive pattern selected

from among the plurality of conductive patterns included in the peripheral circuit interconnection unit P80. Each of the plurality of through electrodes TSV may be connected to the peripheral circuit 30 (see FIG. 1) in the peripheral circuit region P30 through the at least one conductive pattern.

[0041] There may not be a conductive bonding structure which is a result obtained by bonding the conductive bonding pattern included in the memory cell interconnection unit C60 to the conductive bonding pattern included in the peripheral circuit interconnection unit P80, in an electrical connection path between the plurality of through electrodes TSV and the peripheral circuit 30 (see FIG. 1) in the peripheral circuit region P30. Therefore, it may be possible to fundamentally block and/or reduce the increase in resistance due to the conductive bonding structure in the electrical connection path between the plurality of through electrodes TSV and the peripheral circuit 30 (see FIG. 1) in the peripheral circuit region P30.

[0042] In some example embodiments, an integrated circuit device may include both the through electrodes THV and TSV such that peripheral circuit interconnection unit P80 includes at least one conductive pattern selected from among the plurality of conductive patterns included in the peripheral circuit interconnection unit P80 connected to a through electrode THV, and at least one other conductive pattern selected from among the plurality of conductive patterns included in the peripheral circuit interconnection unit P80 connected to a through electrode TSV.

[0043] FIG. 4A is a plan view illustrating an example structure of some components of the memory cell array 20 illustrated in FIG. 1, and FIG. 4B is a cross-sectional view illustrating some configurations of a cross-section taken along line A1-A1' and a cross-section taken along line A2-A2' of FIG. 4A.

[0044] Referring to FIGS. 4A and 4B, the memory cell array 20 may include a semiconductor layer 102 including a memory cell region MEC and a connection region CON. The semiconductor layer 102 may have a main surface 102M extending in the horizontal direction along an X-Y plane of FIG. 4B. The semiconductor layer 102 may include a single crystal semiconductor or a polycrystalline semiconductor. The semiconductor layer 102 may include Si, Ge, or SiGe. The connection region CON may be disposed adjacent to an edge side of the memory cell region MEC. FIGS. 4A and 4B illustrate that the connection region CON is only disposed on one side of the memory cell

region MEC, but the connection region CON may be disposed on one or both sides of the memory cell region MEC in a first horizontal direction (the X direction).

[0045] The memory stack MS extending over the memory cell region MEC and the connection region CON may be formed on the semiconductor layer 102. The memory stack MS may include the plurality of word lines WL disposed in the memory cell region MEC, and a plurality of pad regions 112 disposed in the connection region CON and integrally connected to the plurality of word lines WL. The plurality of word lines WL may extend in the horizontal direction parallel to the main surface 102M of the semiconductor layer 102 and may overlap each other in the vertical direction (the Z direction). The plurality of pad regions 112 may be configured to form a stepped connection part 110 in the connection region CON.

[0046] The plurality of word lines WL may include the ground select line GSL and the string select line SSL. A stacked number of the plurality of word lines WL overlapping each other in the vertical direction (the Z direction) in the memory cell region MEC may be at least 48, 64, or 96, but the stacked number of the plurality of word lines WL is not limited to the above examples.

[0047] A plurality of word line cut regions WLC may extend in the first horizontal direction (the X direction) parallel to the main surface 102M of the semiconductor layer 102. The plurality of word line cut regions WLC may define a width of each of the plurality of word lines WL in a second horizontal direction (the Y direction).

[0048] A plurality of common source regions (not shown) may be formed to extend in the X direction in the semiconductor layer 102. In some example embodiments, the plurality of common source regions may include an impurity region heavily doped with n-type impurities. The plurality of common source regions may function as a source region for supplying current to vertical-type memory cells. A plurality of common source patterns CSP may extend in the X direction on the plurality of common source regions. The plurality of common source patterns CSP may be formed to fill a portion of the word line cut region WLC. The common source pattern CSP may be surrounded by an insulating spacer 120 in the word line cut region WLC. The insulating spacer 120 may include an oxide film, a nitride film, or a combination thereof.

[0049] Two string select lines SSL neighboring in the Y direction may be spaced apart from each other with a string select line cut region SSLC therebetween. The string select

line cut region SSLC may be filled with an insulating film 122. The insulating film 122 may include an oxide film, a nitride film, and/or a combination thereof.

[0050] The plurality of word lines WL and the plurality of pad regions 112 may respectively include metal, metal silicide, a semiconductor doped with impurities, and/or combinations thereof. For example, each of the plurality of word lines WL may include metal such as W, Ni, Co, Ta, and/or the like, metal silicide such as tungsten silicide, nickel silicide, cobalt silicide, tantalum silicide, and/or the like, polysilicon doped with impurities, and/or combinations thereof.

[0051] A plurality of insulating films 124 may be between the semiconductor layer 102 and the ground select line GSL and between the plurality of word lines WL. The insulating film 124 closest to the semiconductor layer 102 among the plurality of insulating films 124 may have a thickness less than that of the other insulating films 124. The insulating film 124 furthest from the semiconductor layer 102 among the plurality of insulating films 124 may cover a top surface of the string select line SSL. The plurality of insulating films 124 may include silicon oxide, silicon nitride, and/or SiON.

[0052] In the memory cell region MEC, a plurality of channel structures 130 may extend in the vertical direction (the Z direction) through the plurality of word lines WL and the plurality of insulating films 124. The plurality of channel structures 130 may be arranged to be spaced apart from each other at predetermined, or desired, intervals in the X and Y directions. The plurality of channel structures 130 may include a gate dielectric film 132, a channel region 134, a buried insulating film 136, and a drain region 138, respectively. The channel region 134 may include doped polysilicon and/or undoped polysilicon. The channel region 134 may have a cylindrical shape, although other shapes may be used. An internal space of the channel region 134 may be filled with the buried insulating film 136. The buried insulating film 136 may include an insulating material. For example, the buried insulating film 136 may include silicon oxide, silicon nitride, SiON, and/or combinations thereof. The drain region 138 may include polysilicon doped with impurities, metal, conductive metal nitride, or combinations thereof. Examples of the metal that may constitute the drain region 138 may include W, Ni, Co, Ta, and/or the like. The plurality of drain regions 138 may be insulated from each other by an insulating film 137. The insulating film 137 may include an oxide film, a nitride film, and/or a combination thereof.

[0053] In the memory cell region MEC, a plurality of bit lines BL may be disposed on the plurality of word lines WL and the plurality of channel structures 130. The plurality of bit

lines BL may be disposed in parallel to each other and may extend in the Y direction. A plurality of bit line contact pads 142 may be between the plurality of channel structures 130 and the plurality of bit lines BL. The drain region 138 may be connected to one corresponding bit line BL among the plurality of bit lines BL through the bit line contact pad 142. The plurality of bit line contact pads 142 may be insulated from each other by an insulating film 143. The plurality of bit lines BL may be insulated from each other by an insulating film 145. The plurality of bit line contact pads 142 and the plurality of bit lines BL may include metal, metal nitride, or a combination thereof. For example, the plurality of bit line contact pads 142 and the plurality of bit lines BL may have the same material or different materials, and include W, Ti, Ta, Cu, Al, Ti, TiN, TaN, WN, and/or combinations thereof. The insulating film 143 and the insulating film 145 may have the same material or different materials, and include an oxide film, a nitride film, and/or a combination thereof.

[0054] An insulating film 114 covering the stepped connection part 110 may be between the semiconductor layer 102 and the insulating film 137 in the connection region CON. The insulating film 114 may cover the plurality of pad regions 112. In the connection region CON, a plurality of contact plugs 116 may be connected to the stepped connection part 110. The plurality of contact plugs 116 may extend from the plurality of pad regions 112 through the insulating films 114, 137, and 143 in the vertical direction (the Z direction). A plurality of interconnection layers MA may be formed on the plurality of contact plugs 116. The plurality of interconnection layers MA may be connected to the plurality of contact plugs 116. The plurality of interconnection layers MA may be configured to be electrically connectable to the word lines WL through the plurality of contact plugs 116, respectively. The plurality of interconnection layers MA may be formed at the same level as the plurality of bit lines BL. Herein, the term "level" may mean a distance in the vertical direction (Z direction or -Z direction) from the main surface 102M of the semiconductor layer 102. In the connection region CON, the plurality of interconnection layers MA may be insulated from each other by the insulating film 145. The plurality of contact plugs 116 and the plurality of interconnection layers MA may each include W, Ti, Ta, Cu, Al, Ti, TiN, TaN, WN, and/or combinations thereof.

[0055] FIG. 5A is an exploded plan view illustrating some components of an integrated circuit device 300A according to still other example embodiments of the inventive concepts. The integrated circuit device 300A may have substantially the same configuration as the integrated circuit device 100 illustrated in FIG. 2. The integrated circuit device 300A may

include the plurality of through electrodes THV. However, the plurality of through electrodes THV may be arranged to surround four sides of the memory stack unit MSP included in the memory structure MST. A plurality of through electrodes THV1, which is a portion of the plurality of through electrodes THV, may be arranged in a line in an extension direction (the Y direction) of the plurality of bit lines BL included in the memory stack unit MSP. A plurality of through electrodes THV2, which is another portion of the plurality of through electrodes THV, may be arranged in a line in a width direction (the X direction) of the plurality of bit lines BL included in the memory stack unit MSP.

[0056] FIG. 5B is an exploded plan view illustrating some components of an integrated circuit device 300B according to still other example embodiments of the inventive concepts. The integrated circuit device 300B may have substantially the same configuration as the integrated circuit device 300A illustrated in FIG. 5A. However, in the integrated circuit device 300B, the plurality of through electrodes THV may be arranged to surround three sides of the memory stack unit MSP included in the memory structure MST.

[0057] FIGS. 5A and 5B illustrate configurations in which at least three sides of the memory stack unit MSP of the memory structure MST are arranged to be surrounded by the plurality of through electrodes THV, but the inventive concepts are not limited to the illustrations in FIGS. 5A and 5B. For example, the plurality of through electrodes THV may be disposed to surround one side or two sides of the memory stack unit MSP.

[0058] FIG. 6 is a cross-sectional view illustrating an integrated circuit device 400A according to example embodiments of the inventive concepts.

[0059] Referring to FIG. 6, the integrated circuit device 400A may include a memory structure M4A and a peripheral circuit structure P4A, which are bonded to each other.

[0060] The memory structure M4A may include the memory stack unit MSP, the memory cell interconnection unit C60, and the memory cell insulation unit C70 surrounding the memory stack unit MSP and the memory cell interconnection unit C60.

[0061] The memory stack unit MSP may include the memory stack MS. The detailed configuration of the memory stack MS is the same as those described with reference to FIGS. 4A and 4B. In FIG. 6, some components of the memory stack MS are omitted for the simplicity of the drawings. The memory cell interconnection unit C60 may include a plurality of upper conductive patterns M152 and B162 configured to be electrically connected to the memory stack MS of the memory stack unit MSP. A plurality of contact plugs C154 may be between the plurality of bit lines BL and the upper conductive pattern

M152, and between the plurality of interconnection layers MA and the upper conductive pattern M152, and a plurality of contact plugs C164 may be between the upper conductive pattern M152 and the upper conductive pattern B162. The memory cell insulation unit C70 may include an oxide film, a nitride film, a polymer film, and/or combinations thereof. The memory cell insulation unit C70 may be integrally connected to an insulating film 114 covering the memory stack MS.

[0062] The peripheral circuit structure P4A may include the peripheral circuit board SUB, the peripheral circuit region P30 and the peripheral circuit interconnection unit P80 sequentially formed on the peripheral circuit board SUB.

[0063] The peripheral circuit board SUB may include a first region A1 overlapping the memory stack unit MSP in the vertical direction (the Z direction) and a second region A2 overlapping the memory cell insulation unit C70 in the vertical direction (the Z direction). The peripheral circuit board SUB may have a main surface SM extending in the horizontal direction along the X-Y plane. In example embodiments, the peripheral circuit board SUB may include Si, Ge, or SiGe. In other example embodiments, the peripheral circuit board SUB may include a polysilicon film, a silicon-on-insulator (SOI) structure, or a germanium-on-insulator (GeOI) structure.

[0064] The peripheral circuit 30 described with reference to FIG. 1 may be formed in the peripheral circuit region P30. The peripheral circuit region P30 may include a plurality of transistors TR formed on an active region of the peripheral circuit board SUB. Each of the transistors TR may include a gate PG and source/drain regions (not shown) formed in the active region of the peripheral circuit board SUB at both sides of the gate PG. A gate insulating film 204 may be between the peripheral circuit board SUB and the gate PG, and both sidewalls of the gate PG may be covered with insulating spacers 210. A plurality of contact plugs 220 may be connected to the plurality of transistors TR. The peripheral circuit region P30 may further include unit devices such as a resistor and a capacitor.

[0065] The peripheral circuit interconnection unit P80 may be between the peripheral circuit region P30 and the memory structure M4A. The peripheral circuit interconnection unit P80 may have a multilayer interconnection structure including a plurality of lower conductive patterns M252, M262, and B272 and a plurality of contact plugs C254, C264, and C274. The number of layers of the multilayer interconnection structure is not limited to the illustration in FIG. 6, and may have the multilayer interconnection structure having various number of layers as necessary. At least some of the plurality of lower conductive

patterns M252, M262, and B272 and the plurality of contact plugs C254, C264, and C274 may be electrically connected to the plurality of transistors TR in the peripheral circuit region P30.

[0066] The plurality of contact plugs 220, the plurality of lower conductive patterns M252, M262, and B272, and the plurality of contact plugs C254, C264, and C274 may include metal, conductive metal nitride, metal silicide, and/or combinations thereof, respectively. In example embodiments, the plurality of contact plugs 220, the plurality of lower conductive patterns M252, M262, and B272, and the plurality of contact plugs C254, C264, and C274 may include W, Al, Cu, Mo, Ti, Co, Ta, Ni, tungsten silicide, titanium silicide, cobalt silicide, tantalum silicide, nickel silicide, and/or combinations thereof. For example, the plurality of contact plugs 220, the plurality of lower conductive patterns M252, M262, and B272, and the plurality of contact plugs C254, C264, and C274 may respectively include a metal pattern including W, Al, or Cu and a conductive barrier film surrounding the metal pattern. The conductive barrier film may include Ti, TiN, Ta, TaN, and/or combinations thereof.

[0067] Conductive regions included in the peripheral circuit region P30 and the peripheral circuit interconnection unit P80 may be covered with an interlayer insulating film 290. The interlayer insulating film 290 may include silicon oxide, silicon nitride, SiON, and/or SiOCN.

[0068] The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 may be bonded to each other. In the first region A1, a plurality of conductive bonding structures BS may be disposed along a boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80, which are bonded to each other. Each of the plurality of conductive bonding structures BS may include a bonding result of the upper conductive pattern B162 included in the memory cell interconnection unit C60 and the lower conductive pattern B272 included in the peripheral circuit interconnection unit P80. The upper conductive pattern B162 and the lower conductive pattern B272 constituting each of the plurality of conductive bonding structures BS may have a structure in which they are integrally coupled to each other without the boundary between them.

[0069] A back surface 102B of the semiconductor layer 102 and a back surface C70B of the memory cell insulation unit C70 may be covered with an insulating film 430. The insulating film 430 may include a silicon oxide film, a silicon nitride film, and/or a polymer

film. A conductive pad 440 may be formed on the insulating film 430. The conductive pad 440 may be spaced apart from the memory structure M4A with the insulating film 430 therebetween. The conductive pad 440 may extend in the horizontal direction along the X-Y plane outside the memory structure M4A. The conductive pad 440 may not include a portion overlapping the memory stack MS in the vertical direction (the Z direction).

[0070] In example embodiments, the conductive pad 440 may include a stacked structure of a first conductive film and a second conductive film. The first conductive film may include Ti, Cu, Ni, Au, NiV, NiP, TiNi, TiW, TaN, Al, Pd, CrCu, and/or combinations thereof. For example, the first conductive film may include a Cr/Cu/Au stacked structure, a Cr/CrCu/Cu stacked structure, a TiWCu compound, a TiWCu/Cu stacked structure, a Ni/Cu stacked structure, a NiV/Cu stacked structure, a Ti/Ni stacked structure, a Ti/NiP stacked structure, a TiWNiV compound, an Al/Ni/Au stacked structure, an Al/NiP/Au stacked structure, a stacked structure of Ti/TiNi/CuNi compound, a Ti/Ni/Pd stacked structure, a Ni/Pd/Au stacked structure, or a NiP/Pd/Au stacked structure. The second conductive film may include Ni, Cu, Al, and/or combinations thereof.

[0071] A through electrode THV4 may be disposed in the second region A2, in which the through electrode THV4 may penetrate the insulating film 430 and the memory cell insulation unit C70, and may extend to the peripheral circuit interconnection unit P80 in the vertical direction (the Z direction). The through electrode THV4 may extend to a lower conductive pattern M262 through a portion of the interlayer insulating film 290 included in the peripheral circuit interconnection unit P80. One end of the through electrode THV4 may be in contact with the lower conductive pattern M262, and the other end of the through electrode THV4 may be in contact with the conductive pad 440. The through electrode THV4 may include at least one metal selected from among W, Au, Ag, Cu, Al, TiAlN, WN, Ir, Pt, Pd, Ru, Zr, Rh, Ni, Co, Cr, Sn, and/or Zn. In example embodiments, the through electrode THV4 may include a metal film including W and a conductive barrier film surrounding the metal film. The conductive barrier film may include Ti, TiN, Ta, TaN, and/or combinations thereof.

[0072] Although one through electrode THV4 is illustrated in FIG. 6, the integrated circuit device 400A may include a plurality of through electrodes THV4 in the second region A2, in which the through electrode THV4 may penetrate the insulating layer 430 and the memory cell insulation unit C70 and may extend to the peripheral circuit interconnection unit P80 in the vertical direction (the Z direction). As described with respect to the plurality

of through electrodes THV with reference to FIG. 5A or 5B, the plurality of through electrodes THV4 may include the plurality of through electrodes THV1 arranged in a line in the extension direction (the Y direction) of the plurality of bit lines BL included in the memory stack unit MSP and the plurality of through electrodes THV2 arranged in a line in the width direction (the X direction) of the plurality of bit lines BL.

[0073] In the peripheral circuit interconnection unit P80, the lower conductive pattern M262 contacting one end of the through electrode THV4 may be formed at a different level than the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS. Herein, the term "level" means a distance in the vertical direction (Z direction or -Z direction) from the main surface SM of the peripheral circuit board SUB. The shortest distance from the main surface SM of the peripheral circuit board SUB to the lower conductive pattern B272 which constitutes the conductive bonding structure BS, may be greater than the shortest distance from the main surface SM to the lower conductive pattern M262, which is in contact with one end of the through electrode THV4. The lower conductive pattern B272 constituting the conductive bonding structure BS may be disposed along the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80, and the lower conductive pattern M262 in contact with one end of the through electrode THV4 may be spaced apart from the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 in a direction approaching the peripheral circuit board SUB.

[0074] The lower conductive pattern M262 contacting one end of the through electrode THV4 and the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS may include different metals. In example embodiments, the lower conductive pattern M262 contacting one end of the through electrode THV4 may include Al, and the lower conductive pattern B272 constituting the conductive bonding structure BS may include Cu.

[0075] The lower conductive pattern M262 contacting one end of the through electrode THV4 and the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS may have different cross-sectional shapes in the vertical direction (the Z direction). In example embodiments, the lower conductive pattern M262 contacting one end of the through electrode THV4 may have a cross-sectional shape in which a width in the horizontal direction along the X-Y plane decreases as the lower conductive pattern M262 becomes closer toward the conductive structure M4A, and the lower conductive

pattern B272 constituting the bonding structure BS may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane increases as the lower conductive pattern B272 becomes closer toward the memory structure M4A.

[0076] The conductive bonding structure BS may not exist in an electrical connection path between the through electrode THV4 and the peripheral circuits in the peripheral circuit region P30. Thus, the increase in resistance due to the conductive bonding structure BS in the electrical connection path between the through electrode THV4 and the peripheral circuits in the peripheral circuit region P30 may be reduced or prevented. In particular, when the through electrode THV4 is connected to a circuit used for inputting/outputting data, addresses, or commands, such as the data input/output circuit 36 described with reference to FIG. 1, an ESD circuit, a pull-up/pull-down driver, or a circuit sensitive to resistance, the reliability of the integrated circuit device 400A may be improved by reducing the resistance in the electrical connection path via the through electrode THV4.

[0077] FIG. 7 is a cross-sectional view illustrating an integrated circuit device 400B according to example embodiments of the inventive concepts.

[0078] Referring to FIG. 7, the integrated circuit device 400B may have substantially the same configuration as the integrated circuit device 400A described with reference to FIG. 6. However, the integrated circuit device 400B may include a conductive pad 450 formed on the insulating film 430. The conductive pad 450 may have substantially the same configuration as the conductive pad 440 described with reference to FIG. 6. However, the conductive pad 450 may include a portion overlapping the memory stack MS in the vertical direction (the Z direction). Therefore, an area in which the conductive pads 450 may extend outwardly beyond the memory structure M4A in the horizontal direction may be reduced, thereby reducing the increase of a planar size of a chip due to the conductive pads 450. Therefore, it may contribute to reducing the planar size of the chip including the integrated circuit device 400B.

[0079] FIG. 8 is a cross-sectional view illustrating an integrated circuit device 400C according to example embodiments of the inventive concepts.

[0080] Referring to FIG. 8, the integrated circuit device 400C may have substantially the same configuration as the integrated circuit device 400A described with reference to FIG. 6. However, the peripheral circuit structure P4C of the integrated circuit device 400C may include a peripheral circuit interconnection unit P84. The peripheral circuit interconnection unit P84 may have a multilayer interconnection structure including a plurality of lower

conductive patterns M252, M462, and B272 and a plurality of contact plugs C254, C264, and C274.

[0081] The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80 may be bonded to each other. In the first region A1, the plurality of conductive bonding structures BS may be disposed along the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P80, which are bonded to each other.

[0082] In the second region A2, the through electrode THV4 may extend to the peripheral circuit interconnection unit P84 in the vertical direction (the Z direction), through the insulating layer 430 and the memory cell insulation unit C70. The through electrode THV4 may extend to the lower conductive pattern M462 included in the peripheral circuit interconnection unit P84. One end of the through electrode THV4 may be in contact with the lower conductive pattern M462.

[0083] The lower conductive pattern M462 contacting one end of the through electrode THV4 and the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS may be formed at different levels. The shortest distance from the main surface SM of the peripheral circuit board SUB to the lower conductive pattern B272 which constitutes the conductive bonding structure BS, may be greater than the shortest distance from the main surface SM to the lower conductive pattern M462 which is in contact with one end of the through electrode THV4.

[0084] The lower conductive pattern M462 contacting one end of the through electrode THV4 and the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS may include the same metal. In example embodiments, the lower conductive pattern M462 contacting one end of the through electrode THV4 and the lower conductive pattern B272 constituting the conductive bonding structure BS may include Cu, respectively.

[0085] The lower conductive pattern M462 contacting one end of the through electrode THV4 and the lower conductive pattern B272 constituting the conductive bonding structure BS may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane increases as they become closer toward the memory structure M4A, respectively.

[0086] FIG. 9 is a cross-sectional view illustrating an integrated circuit device 400D according to example embodiments of the inventive concepts.

[0087] Referring to FIG. 9, the integrated circuit device 400D may have substantially the same configuration as the integrated circuit device 400C described with reference to FIG. 8. However, the integrated circuit device 400D may include the conductive pad 450 formed on the insulating film 430. The conductive pad 450 may include a portion overlapping the memory stack MS in the vertical direction (the Z direction).

[0088] FIG. 10 is a cross-sectional view illustrating an integrated circuit device 500A according to example embodiments of the inventive concepts.

[0089] Referring to FIG. 10, the integrated circuit device 500A may have substantially the same configuration as the integrated circuit device 400A described with reference to FIG. 6. However, the peripheral circuit structure P5A of the integrated circuit device 500A may include a peripheral circuit interconnection unit P85A. The peripheral circuit interconnection unit P85A may have a multilayer interconnection structure including a plurality of lower conductive patterns M252, M262, B272 and B574 and a plurality of contact plugs C254, C264, and C274.

[0090] The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P85A may be bonded to each other. In the first region A1, the plurality of conductive bonding structures BS may be disposed along the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P85A, which are bonded to each other.

[0091] In the second region A2, a through electrode THV5 may extend to the peripheral circuit interconnection unit P85A in the vertical direction (the Z direction), through the insulating layer 430 and the memory cell insulation unit C70. The through electrode THV5 may extend to the lower conductive pattern B574 included in the peripheral circuit interconnection unit P85A. One end of the through electrode THV5 may be in contact with the lower conductive pattern B574, and the other end of the through electrode THV5 may be in contact with the conductive pad 440. More detailed configuration with respect to the through electrode THV5 may be substantially the same as that described with respect to the through electrode THV4 with reference to FIG. 6.

[0092] The lower conductive pattern B574 and the lower conductive pattern B272 may be formed at the same level. The shortest distance from the main surface SM of the peripheral circuit board SUB to the lower conductive pattern B272 may be approximately the same as or similar to the shortest distance from the main surface SM to the lower conductive pattern B574. The lower conductive pattern B574 and the lower conductive pattern B272 may

include the same metal. In example embodiments, the lower conductive pattern B574 and the lower conductive pattern B272 may respectively include Cu. The lower conductive pattern B574 and the lower conductive pattern B272 may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane increases as they become closer toward the memory structure M4A, respectively.

[0093] The conductive bonding structure BS may not exist in an electrical connection path between the through electrode THV5 and peripheral circuits in the peripheral circuit region P30. Thus, the increase in resistance due to the conductive bonding structure BS in the electrical connection path between the through electrode THV5 and the peripheral circuits in the peripheral circuit region P30 may be reduced or prevented.

[0094] FIG. 11 is a cross-sectional view illustrating an integrated circuit device 500B according to example embodiments of the inventive concepts.

[0095] Referring to FIG. 11, the integrated circuit device 500B may have substantially the same configuration as the integrated circuit device 500A described with reference to FIG. 10. However, the integrated circuit device 500B may include the conductive pad 450 formed on the insulating film 430. The conductive pad 450 may include a portion overlapping the memory stack MS in the vertical direction (the Z direction).

[0096] FIG. 12 is a cross-sectional view illustrating an integrated circuit device 500C according to example embodiments of the inventive concepts.

[0097] Referring to FIG. 12, the integrated circuit device 500C may have substantially the same configuration as the integrated circuit device 400A described with reference to FIG. 6. However, the peripheral circuit structure P5C of the integrated circuit device 500C may include a peripheral circuit interconnection unit P85C. The peripheral circuit interconnection unit P85C may have a multilayer interconnection structure including a plurality of lower conductive patterns M252, M262, B272 and M574 and a plurality of contact plugs C254, C264, and C274.

[0098] The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P85C may be bonded to each other. In the first region A1, the plurality of conductive bonding structures BS may be disposed along the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P85C, which are bonded to each other.

[0099] In the second region A2, the through electrode THV5 may extend to the peripheral circuit interconnection unit P85C in the vertical direction (the Z direction), through the

insulating layer 430 and the memory cell insulation unit C70. The through electrode THV5 may extend to the lower conductive pattern M574 included in the peripheral circuit interconnection unit P85C. One end of the through electrode THV5 may be in contact with the lower conductive pattern M574.

[00100] The lower conductive pattern M574 and the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS may be formed at the same level. The shortest distance from the main surface SM of the peripheral circuit board SUB to the lower conductive pattern B272 may be approximately the same as or similar to the shortest distance from the main surface SM to the lower conductive pattern M574.

[00101] The lower conductive pattern M574 and the lower conductive pattern B272 may include the same metal. In example embodiments, the lower conductive pattern M574 and the lower conductive pattern B272 may include Cu, respectively. The lower conductive pattern M574 and the lower conductive pattern B272 may have different cross-sectional shapes in the vertical direction (the Z direction). In example embodiments, the lower conductive pattern M574 may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane decreases as it becomes closer to the memory structure M4A, and the lower conductive pattern B272 may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane increases as it becomes closer to the memory structure M4A.

[00102] FIG. 13 is a cross-sectional view illustrating an integrated circuit device 500D according to example embodiments of the inventive concepts.

[00103] Referring to FIG. 13, the integrated circuit device 500D may have substantially the same configuration as the integrated circuit device 500C described with reference to FIG. 12. However, the integrated circuit device 500D may include the conductive pad 450 formed on the insulating film 430. The conductive pad 450 may include a portion overlapping the memory stack MS in the vertical direction (the Z direction).

[00104] The integrated circuit devices 400A, 400B, 400C, 400D, 500A, 500B, 500C, and 500D illustrated in FIGS. 6 to 13 may be a portion of the integrated circuit device 300A illustrated in FIG. 5A or the integrated circuit device 300B illustrated in FIG. 5B, respectively.

[00105] FIG. 14A is an exploded plan view illustrating some components of an integrated circuit device 600A according to example embodiments of the inventive concepts. The integrated circuit device 600A may have substantially the same configuration as the

integrated circuit device 200 illustrated in FIG. 3. The integrated circuit device 600A may include a plurality of through electrodes TSV penetrating only the peripheral circuit structure PST without penetrating the memory structure MST. The plurality of through electrodes TSV may extend in the vertical direction (the Z direction) to completely penetrate the peripheral circuit board SUB and the peripheral circuit region P30 of the peripheral circuit structure PST and partially penetrate the peripheral circuit interconnection unit P80. However, the plurality of through electrodes TSV may be disposed to surround four sides of the peripheral circuit structure PST. A plurality of through electrodes TSV1, which is a portion of the plurality of through electrodes TSV, may be arranged in a line in the extension direction (the Y direction) of the plurality of bit lines BL included in the memory stack unit MSP. A plurality of through electrodes TSV2, which is another portion of the plurality of through electrodes TSV, may be arranged in a line in the width direction (the X direction) of the plurality of bit lines BL included in the memory stack unit MSP. More detailed configurations of the plurality of through electrodes TSV may be substantially the same as those described with reference to FIG. 3.

[00106] FIG. 14B is an exploded plan view illustrating some components of an integrated circuit device 600B according to example embodiments of the inventive concepts. The integrated circuit device 600B may have substantially the same configuration as the integrated circuit device 600A illustrated in FIG. 14A. However, in the integrated circuit device 600B, the plurality of through electrodes TSV may be disposed to surround three sides of the peripheral circuit structure PST.

[00107] FIGS. 14A and 14B illustrate a configuration in which a plurality of through electrodes TSV are disposed to surround at least three sides of the peripheral circuit structure PST, but the inventive concepts are not limited to example embodiments illustrated in FIGS. 14A and 14B. For example, the plurality of through electrodes TSV may be arranged to surround one side or two sides of the peripheral circuit structure PST.

[00108] FIG. 15 is a cross-sectional view illustrating an integrated circuit device 700A according to example embodiments of the inventive concepts.

[00109] Referring to FIG. 15, the integrated circuit device 700A may have substantially the same configuration as the integrated circuit device 400A described with reference to FIG. 6. However, the integrated circuit device 700A may include an insulating film 730 covering a back surface SB of the peripheral circuit board SUB. A conductive pad 740 may

be formed on the insulating film 730. The conductive pad 740 may be spaced apart from the peripheral circuit board SUB with the insulating layer 730 therebetween.

[00110] In the integrated circuit device 700A, the peripheral circuit interconnection unit P87A of the peripheral circuit structure P7A may include a multilayer interconnection structure including the plurality of lower conductive patterns M252, M262, and B272 and the plurality of contact plugs C254, C264, C274. A through electrode TSV7 may be arranged in the second region A2, in which the through electrode TSV7 extends to the peripheral circuit interconnection unit P87A through the insulating film 730, the peripheral circuit board SUB, and the peripheral circuit area P30 in the vertical direction (the Z direction). The through electrode THV7 may extend to the lower conductive pattern M262 included in the peripheral circuit interconnection unit P87A. One end of the through electrode THV7 may be in contact with the lower conductive pattern M262, and the other end of the through electrode THV7 may be in contact with the conductive pad 740.

[00111] More detailed configurations with respect to the insulating film 730, the conductive pad 740, and the through electrode TSV7 may be generally the same as those described with respect to the insulating film 430, the conductive pad 440, and the through electrode THV4 with reference to FIG. 6.

[00112] Although one through electrode TSV7 is illustrated in the second region A2 in FIG. 15, the integrated circuit device 700A may include a plurality of through electrodes TSV7 in the second region A2, which extend to the peripheral circuit interconnection unit P87A through the insulating film 730, the peripheral circuit board SUB, and the peripheral circuit region P30 in the vertical direction (the Z direction). As described with respect to the plurality of through electrodes THV with reference to FIGS. 14A or 14B, the plurality of through electrodes THV7 may include the plurality of through electrodes THV1 arranged in a line in the extension direction (the Y direction) of the plurality of bit lines BL and the plurality of through electrodes THV2 arranged in a line in the width direction (the X direction) of the plurality of bit lines BL.

[00113] The lower conductive pattern M262 contacting one end of the through electrode TSV7 and the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS may be formed at different levels, and may include different metals. In addition, the lower conductive pattern M262 may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane decreases as the lower conductive pattern M262 becomes closer toward the memory structure M4A, and the lower conductive

pattern B272 may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane increases as the lower conductive pattern B272 becomes closer toward the memory structure M4A.

[00114] The conductive bonding structure BS may not exist in an electrical connection path between the through electrode THV7 and the peripheral circuits in the peripheral circuit region P30. Thus, the increase in resistance due to the conductive bonding structure BS in the electrical connection path between the through electrode THV7 and the peripheral circuits in the peripheral circuit region P30 may be reduced or prevented.

[00115] In addition, since the through electrode TSV7 may be configured to penetrate only the peripheral circuit structure P7A without penetrating the memory structure M4A, even if the stacked number of word lines WL are increased in order to improve the degree of integration in the memory stack MS and the number of contacts connected to the word lines WL and the number of interconnections are increased, a vertical length of the through electrode TSV7 may be kept constant regardless of the increase in height in the vertical direction of the memory stack MS. Accordingly, even if the stacked number of word lines WL are increased to increase the vertical height of the memory stack MS, a resistance value may be kept constant in an electrical connection path connected to the outside from a circuit used to input/output data, an address, or a command, or a circuit sensitive to resistance.

[00116] FIG. 16 is a cross-sectional view illustrating an integrated circuit device 700B according to example embodiments of the inventive concepts.

[00117] Referring to FIG. 16, the integrated circuit device 700B may have substantially the same configuration as the integrated circuit device 700A described with reference to FIG. 15. In the integrated circuit device 700B, the peripheral circuit interconnection unit P87B of the peripheral circuit structure P7B may include a multilayer interconnection structure including the plurality of lower conductive patterns M252, M762, and B272 and the plurality of contact plugs C254, C264, C274.

[00118] The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P87B may be bonded to each other. In the first region A1, the plurality of conductive bonding structures BS may be disposed along the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P87B, which are bonded to each other. One end of the through electrode TSV7 may contact the lower conductive pattern M762 in the second region A2.

[00119] The lower conductive pattern M762 contacting one end of the through electrode THV7 and the lower conductive pattern B272 constituting the plurality of conductive bonding structures BS may be formed at different levels. The lower conductive pattern M762 and the lower conductive pattern B272 may include the same metal. The lower conductive pattern M762 and the lower conductive pattern B272 may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane increases as they become closer to the memory structure M4A, respectively.

[00120] FIG. 17 is a cross-sectional view illustrating an integrated circuit device 800A according to example embodiments of the inventive concepts.

[00121] Referring to FIG. 17, the integrated circuit device 800A may have substantially the same configuration as the integrated circuit device 700A described with reference to FIG. 15. However, the peripheral circuit interconnection unit P88A of the peripheral circuit structure P8A in the integrated circuit device 800A may include a multilayer interconnection structure including a plurality of lower conductive patterns M252, M262, M264, B272, and B874 and a plurality of contact plugs C254, C264, and C274.

[00122] The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P88A may be bonded to each other. In the first region A1, the plurality of conductive bonding structures BS may be disposed along the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P88A, which are bonded to each other.

[00123] In the second region A2, a through electrode TSV8 may extend in the vertical direction (the Z direction) to the peripheral circuit interconnection unit P88A through the insulating film 730, the peripheral circuit board SUB, and the peripheral circuit region P30. One end of the through electrode THV8 may be in contact with the lower conductive pattern B874. More detailed configuration with respect to the through electrode THV8 may be substantially the same as that described with respect to the through electrode THV4 with reference to FIG. 6.

[00124] The lower conductive pattern B874 and the lower conductive pattern B272 may be formed at the same level. The lower conductive pattern B874 and the lower conductive pattern B272 may include the same metal. The lower conductive pattern B874 and the lower conductive pattern B272 may have the cross-sectional shape in which the width in the horizontal direction along the X-Y plane increases as they become closer to the memory structure M4A, respectively.

[00125] The conductive bonding structure BS may not exist in an electrical connection path between the through electrode THV8 and the peripheral circuits in the peripheral circuit region P30. Thus, an increase in resistance due to the conductive bonding structure BS in the electrical connection path between the through electrode THV8 and the peripheral circuits in the peripheral circuit region P30 may be reduced or prevented.

[00126] In addition, since the through electrode TSV8 may be configured to penetrate only the peripheral circuit structure P8A without penetrating the memory structure M4A, even if the stacked number of word lines WL are increased in order to improve the degree of integration in the memory stack MS and the number of contacts connected to the word lines WL and the number of interconnections are increased, a vertical length of the through electrode TSV8 may be kept constant regardless of the increase in height in the vertical direction of the memory stack MS. Accordingly, even if the stacked number of word lines WL are increased to increase the vertical height of the memory stack MS, a resistance value may be kept constant in an electrical connection path connected to the outside from a circuit used to input/output data, an address, or a command, or a circuit sensitive to resistance.

[00127] FIG. 18 is a cross-sectional view illustrating an integrated circuit device 800B according to example embodiments of the inventive concepts.

[00128] Referring to FIG. 18, the integrated circuit device 800B may have substantially the same configuration as the integrated circuit device 800A described with reference to FIG. 17. However, the peripheral circuit interconnection unit P88B of the peripheral circuit structure P8B in the integrated circuit device 800B may include a multilayer interconnection structure including a plurality of lower conductive patterns M252, M262, B272, and M574 and a plurality of contact plugs C254, C264, and C274.

[00129] The memory cell interconnection unit C60 and the peripheral circuit interconnection unit P88B may be bonded to each other. In the first region A1, the plurality of conductive bonding structures BS may be disposed along the boundary 410 between the memory cell interconnection unit C60 and the peripheral circuit interconnection unit P88B, which are bonded to each other.

[00130] One end of the through electrode TSV8 may contact the lower conductive pattern M574 in the second region A2. A detailed description of the lower conductive pattern M574 may be as described with reference to FIG. 12.

[00131] The integrated circuit devices 700A, 700B, 800A, and 800B described with reference to FIGS. 15 to 18 may respectively constitute a portion of the integrated circuit

device 600A illustrated in FIG. 14A or the integrated circuit device 600B illustrated in FIG. 14B.

[00132] FIGS. 19A to 19D are cross-sectional views illustrating a manufacturing method of an integrated circuit device according to example embodiments of the inventive concepts. A method of manufacturing the integrated circuit device 400A illustrated in FIG. 6 will be described with reference to FIGS. 19A to 19D.

[00133] Referring to FIG. 19A, the memory structure M4A including the memory stack unit MSP, the memory cell interconnection unit C60, and a memory cell insulation unit C70 may be formed on a substrate 910.

[00134] The substrate 910 may include silicon. In example embodiments, the semiconductor layer 102 may include polysilicon formed by a deposition process on the substrate 910. In other example embodiments, the semiconductor layer 102 may include a silicon film integrally formed with the substrate 910.

[00135] Referring to FIG. 19B, after forming the peripheral circuit structure P4A in which the peripheral circuit region P30 and the peripheral circuit interconnection unit P80 are stacked on the peripheral circuit board SUB, the peripheral circuit board SUB and the substrate 910 may be aligned such that the circuit interconnection unit P80 face the memory cell interconnection unit C60 and the memory cell insulation unit C70 of the memory structure M4A to each other.

[00136] Referring to FIG. 19C, the plurality of conductive bonding structures BS may be formed by performing the bonding process between the memory cell interconnection unit C60 and the memory cell insulation unit C70, and the peripheral circuit interconnection unit P80.

[00137] In some example embodiments, the memory cell interconnection unit C60 and the memory cell insulation unit C70, and the peripheral circuit interconnection unit P80 may be brought into contact with each other in a state of facing each other, and then subjected to heat treatment under pressure. The heat treatment may be performed at a temperature of about 180 °C to about 300 °C. The conductive bonding structure BS may be formed by being integrally coupled without a boundary between the upper conductive pattern B162 and the lower conductive pattern B272 which are in contact with each other, while metals constituting each of the upper conductive pattern B162 and the lower conductive pattern B272 that are in contact with each other reflow by heat treatment during the bonding process.

[00138] Referring to FIG. 19D, the substrate 910 may be removed from the resultant of FIG. 19C by grinding to expose the semiconductor layer 102 and the memory cell insulation unit C70, and then the insulating film 430 may be formed to cover a back surface 102B of the semiconductor layer 102 and a back surface C70B of the memory cell insulation unit C70. Thereafter, in the second region A2, the through hole TVH may be formed to penetrate the insulating layer 430, the memory cell insulation unit C70, and a portion of the interlayer insulating film 290 and to expose the lower conductive pattern M262.

[00139] Thereafter, the through electrode THV4 filling the through hole TVH may be formed, and then the conductive pad 440 may be formed on the insulating film 430 to manufacture the integrated circuit device 400A illustrated in FIG. 6.

[00140] FIGS. 20A to 20C are cross-sectional views illustrating a method of manufacturing an integrated circuit device in the order of process, according to other example embodiments of the inventive concepts. The method of manufacturing the integrated circuit device 700A illustrated in FIG. 15 will be described with reference to FIGS. 20A to 20C.

[00141] Referring to FIG. 20A, after forming the memory structure M4A on the substrate 910 by the same method as that described with reference to FIG. 19A, the peripheral circuit structure P7A stacked with the peripheral circuit region P30 and the peripheral circuit interconnection unit P87A may be formed on the peripheral circuit board SUB in a similar manner as that described with reference to FIG. 19B, and then the peripheral circuit board SUB and the substrate 910 may be aligned such that the peripheral circuit interconnection unit P87A of the peripheral circuit structure P7A face the interconnection unit C60 and the memory cell insulation unit C70 to each other.

[00142] Referring to FIG. 20B, the bonding process between the memory cell interconnection unit C60 and the memory cell insulation unit C70, and the peripheral circuit interconnection unit P87A may be performed by a method similar to that described with reference to FIG. 19C.

[00143] Referring to FIG. 20C, thereafter, the substrate 910 may be removed from the resultant of FIG. 20B by grinding, the insulating film 730 may be formed to cover the back surface SB of the peripheral circuit board SUB, and the through hole TSH may be formed to penetrate the insulating film 730, the peripheral circuit board SUB, and the peripheral circuit region P30 and to expose the lower conductive pattern M262 included in the peripheral circuit interconnection unit P87A in the second region A2.

[00144] Thereafter, the through electrode TSV7 filling the through hole TSH may be formed, and then the conductive pad 740 may be formed on the insulating film 730 to manufacture the integrated circuit device 700A illustrated in FIG. 15.

[00145] Even though methods of manufacturing the integrated circuit device 400A illustrated in FIG. 6 and the integrated circuit device 700A illustrated in FIG. 15 has been described with reference to FIGS. 19A to 19D and 20A to 20C, those skilled in the art will appreciate that the integrated circuit devices illustrated in FIGS. 2, 3, 5A, 5B, 7 to 13, 14A, 14B, and 16 to 18, and various integrated circuit devices having a structure similar thereto may be manufactured by applying various modifications and changes within the scope of inventive concept, from those described with reference to FIGS. 19A to 19D and 20A to 20C.

[00146] While the inventive concept has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:
 - a memory comprising
 - a memory stack,
 - a memory cell interconnection comprising a plurality of upper conductive patterns configured to be electrically connectable to the memory stack, and
 - a memory cell insulation surrounding the memory stack and the memory cell interconnection;
 - a peripheral circuit comprising
 - a peripheral circuit board,
 - a peripheral circuit region on the peripheral circuit board, and
 - a peripheral circuit interconnection comprising a plurality of lower conductive patterns between the peripheral circuit region and the memory and bonded to the memory cell interconnection;
 - a plurality of conductive bonding structures on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in a vertical direction, the plurality of conductive bonding structures being a bonded resultant of a plurality of first upper conductive patterns selected from among the plurality of upper conductive patterns and a respective plurality of first lower conductive patterns selected from among the plurality of lower conductive patterns; and
 - a through electrode penetrating one of the memory cell insulation and the peripheral circuit board and extended to a second lower conductive pattern selected from among the plurality of lower conductive patterns in the vertical direction, in a second region, the second region overlapping the memory cell insulation in the vertical direction.
2. The integrated circuit device of claim 1, wherein
 - the through electrode penetrates the memory cell insulation and extends to the second lower conductive pattern.
3. The integrated circuit device of claim 1, wherein

the through electrode penetrates the peripheral circuit board and the peripheral circuit region and extends to the second lower conductive pattern.

4. The integrated circuit device of any one of claims 1 to 3, wherein the first lower conductive pattern and the second lower conductive pattern are at different levels.

5. The integrated circuit device of any one of claims 1 to 3, wherein the first lower conductive pattern and the second lower conductive pattern are at the same level.

6. The integrated circuit device of any one of claims 1 to 5, wherein the first lower conductive pattern and the second lower conductive pattern comprise different metals.

7. The integrated circuit device of any one of claims 1 to 5, wherein the first lower conductive pattern and the second lower conductive pattern comprise the same metal.

8. The integrated circuit device of any one of claims 1 to 7, wherein each of the first lower conductive pattern and the second lower conductive pattern has a shape in which a width in a horizontal direction increases as the first lower conductive pattern and the second lower conductive pattern respectively becomes closer toward the memory structure.

9. The integrated circuit device of any one of claims 1 to 7, wherein the first lower conductive pattern has a shape in which a width in a horizontal direction increases as the first lower conductive pattern becomes closer toward the memory structure, and

the second lower conductive pattern has a shape in which a width in the horizontal direction decreases as the second lower conductive pattern becomes closer toward the memory structure.

10. The integrated circuit device of any one of claims 1 to 9, further comprising
a conductive pad in contact with the through electrode and extending in a horizontal direction outside of the memory structure,
wherein the conductive pad comprises a portion overlapping the memory stack in the vertical direction.

11. The integrated circuit device of any one of claims 1 to 9, further comprising
a conductive pad in contact with the through electrode and extending in a horizontal direction outside of the peripheral circuit structure, wherein the conductive pad is spaced apart from the peripheral circuit region with the peripheral circuit board therebetween.

12. An integrated circuit device comprising:
a memory comprising
a memory stack comprising
a plurality of bit lines extending in a first horizontal direction,
a memory cell interconnection comprising a plurality of upper conductive patterns configured to be electrically connectable to the plurality of bit lines, and
a memory cell insulation surrounding the memory stack and the memory cell interconnection;
a peripheral circuit comprising
a peripheral circuit board,
a peripheral circuit region on the peripheral circuit board, and
a peripheral circuit interconnection comprising a plurality of lower conductive patterns between the peripheral circuit region and the memory and bonded to the memory cell interconnection;
a conductive bonding on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in a vertical direction, the conductive bonding being a bonded resultant of a first upper conductive pattern selected from among the plurality of upper conductive patterns and a first lower conductive pattern selected from among the plurality of lower conductive patterns; and

a plurality of through electrodes extended in the vertical direction through one of the memory cell insulation and the peripheral circuit board, in a second region spaced apart from the first region in a horizontal direction,

wherein the plurality of through electrodes comprise a plurality of first through electrodes arranged in a line along the first horizontal direction in the second region.

13. The integrated circuit device of claim 12, wherein
the plurality of through electrodes further comprise a plurality of second through electrodes arranged in a line along a second horizontal direction perpendicular to the first horizontal direction in the second region.

14. The integrated circuit device of claim 12 or claim 13, wherein
the plurality of through electrodes comprise one through electrode in contact with a second lower conductive pattern selected from among the plurality of lower conductive patterns, and
the one through electrode extends to the second lower conductive pattern through the memory cell insulation.

15. The integrated circuit device of claim 12 or claim 13, wherein
the plurality of through electrodes comprise one through electrode in contact with a second lower conductive pattern selected from among the plurality of lower conductive patterns, and
the one through electrode extends to the second lower conductive pattern through the peripheral circuit board and the peripheral circuit region.

16. The integrated circuit device of claim 15, wherein
a first shortest distance from the peripheral circuit board to the first lower conductive pattern is greater than a second shortest distance from the peripheral circuit board to the second lower conductive pattern.

17. The integrated circuit device of claim 15, wherein

a first shortest distance from the peripheral circuit board to the first lower conductive pattern is the same as a second shortest distance from the peripheral circuit board to the second lower conductive pattern.

18. The integrated circuit device of any one of claims 15 to 17, wherein the first lower conductive pattern and the second lower conductive pattern comprise different metals.

19. An integrated circuit device comprising:
a memory comprising
a semiconductor layer,
a memory stack on the semiconductor layer,
a memory cell interconnection comprising a plurality of upper conductive patterns overlapping the memory stack in a vertical direction and configured to be electrically connectable to the memory stack, and
a memory cell insulation surrounding the semiconductor layer, the memory stack, and the memory cell interconnection;
a peripheral circuit comprising
a peripheral circuit board,
a peripheral circuit region on the peripheral circuit board, and
a peripheral circuit interconnection between the peripheral circuit region and the memory and bonded to the memory cell interconnection;
a plurality of conductive bonding structures comprising Cu and on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in the vertical direction;
a plurality of lower conductive patterns comprising at least one metal selected from among Al, W, and Cu and in the peripheral circuit interconnection in a second region, the second region overlapping the memory cell insulation in the vertical direction; and
a through electrode penetrating one of the memory cell insulation and the peripheral circuit board in the second region and contacting one lower conductive pattern among the plurality of lower conductive patterns.

20. The integrated circuit device of claim 19, wherein

the plurality of lower conductive patterns comprise a first lower conductive pattern constituting the plurality of conductive bonding structures and a second lower conductive pattern in contact with the through electrode,

the first lower conductive pattern has a shape in which a width in a horizontal direction increases as the first lower conductive pattern becomes closer toward the memory structure, and

the second lower conductive pattern has a shape in which a width in the horizontal direction decreases as the second lower conductive pattern becomes closer toward the memory structure.