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SEMICONDUCTOR DEVICES

This invention relates to semiconductor devices and in particular bipolar transistors and to integrated circuits including both bipolar and field effect, in particular CMOS (Complementary Metal Oxide Silicon), transistors.

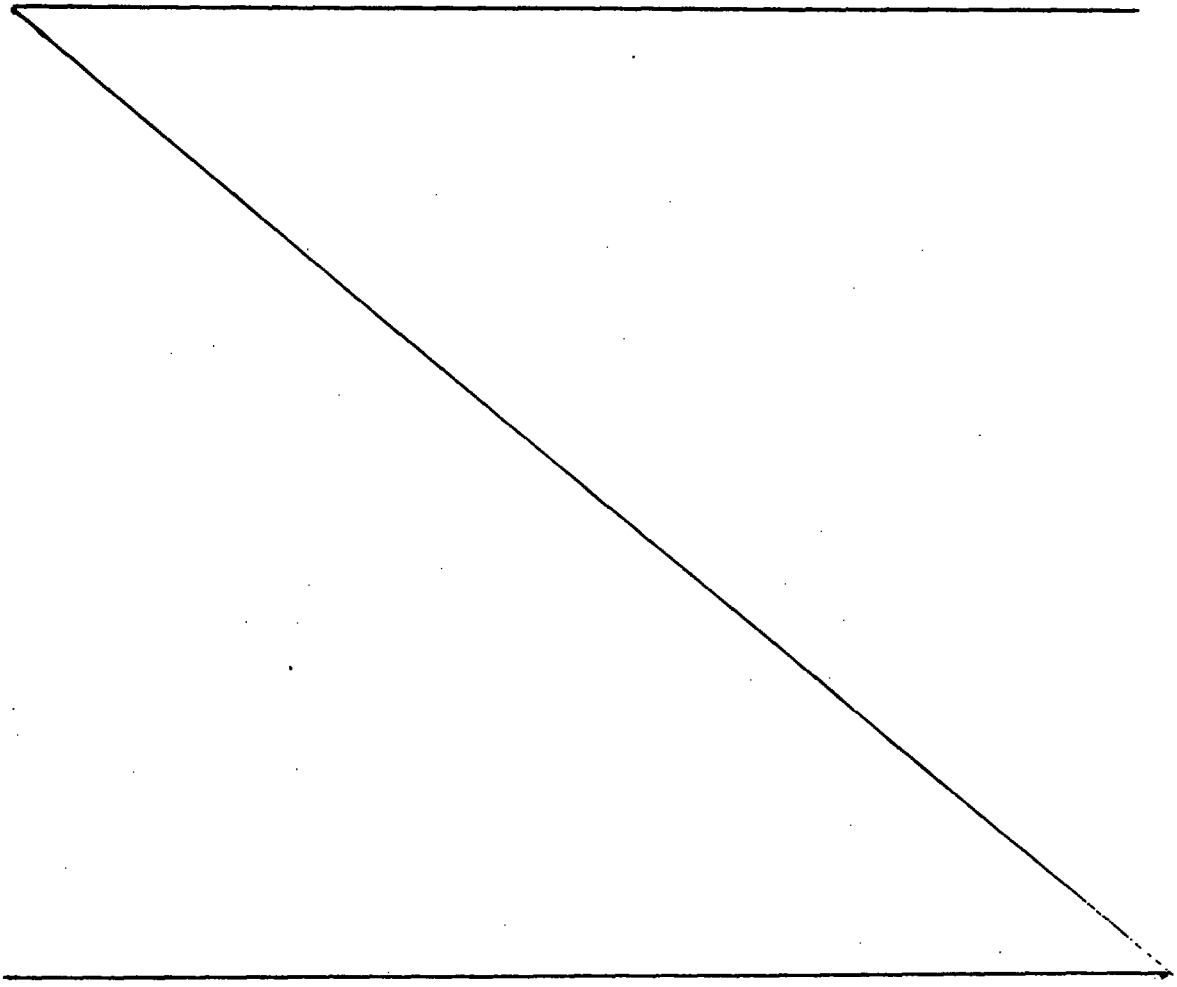
Field effect circuits are used mainly in digital applications, whereas for analogue applications, such as in radio signal processing, bipolar circuits are more suitable. There is a need in certain applications, e.g. telephony, for the processing of both digital and analogue signals and this generally requires the provision of two circuit chips each with its associated peripheral circuitry. Many attempts have been made to combine bipolar and MOS technologies on the same chip but to date none has been entirely successful. A commonly used approach is to add a CMOS capability to a SBC (Standard Buried Collector) bipolar technology. This results in a device with high bipolar performance but poor CMOS capability. If bipolar devices are added to good CMOS technology the resulting triply diffused structures have high parasitic resistances and hence poor bipolar performance.

According to one aspect of the present invention there is provided an integrated circuit including an MOS transistor with a polycrystalline silicon gate and a

bipolar transistor with a polycrystalline silicon emitter, which polycrystalline silicon gate and emitter have the same doping levels and were manufactured by simultaneous etching from a common single polycrystalline layer.

According to another aspect of the present invention there is provided a method of manufacturing an integrated circuit including bipolar and MOS transistors including the step of forming both an MOS transistor gate and a bipolar transistor emitter by etching simultaneously from a common single layer of polycrystalline silicon, the gate and the emitter having the same doping levels.

Embodiments of the invention will now be described with reference to the accompanying drawings, in



which:

Fig. 1 illustrates in cross-section a bipolar/CMOS structure according to one embodiment of the present invention;

Fig. 2 illustrates the bipolar transistor of Fig. 1 formed in a p-well rather than an n-well as illustrated in Fig. 1, and

Figs. 3 to 7 illustrate in cross-section various stages in the manufacture of a bipolar/CMOS structure with n wells.

The bipolar/CMOS structure illustrated in Fig. 1 comprises a bipolar transistor 1, an n-channel MOS transistor 2 and a p-channel MOS transistor 3. The transistor 2 is formed directly in a p-type substrate 4, whereas the transistors 1 and 3 are formed in n-wells 5 and 6, respectively, provided in the substrate 4. The n-channel transistor 2 is formed by conventional CMOS processing and includes n^+ source and drain regions 7 and 8 respectively, external electrical contacts 9 and 10, provided for example by metallisation, to the source and drain regions 7 and 8, a polysilicon gate 11 together with gate oxide 12, a p^+ contact 13 to the substrate 4, an external electrical contact 14 to the p^+ contact 13, provided for example by metallisation, and isolating oxide 15. The gate 11 is also externally electrically connected by means not shown. The p-channel transistor 3 is also formed by conventional CMOS processing in the n-well 6 and includes p^+ source and drain regions 17 and 18, respectively, external electrical contacts 19 and 20, provided for example by metallisation, to the source and drain regions 17 and 18, a polysilicon gate 21 together with gate oxide 22, an n^+ contact 23 to be n-well 6, an external electrical contact 24 to the n^+ contact 23, provided for example by metallisation, and isolating oxide 15.

As will be appreciated from Fig. 1 the bipolar transistor 1 is very similar in cross-section to the p-channel transistor 3 and can in fact be made in integrated form with the CMOS devices by the addition of only two extra masks to number employed for the standard CMOS process. The bipolar transistor 1 employs the n-well 5 as its collector and has an n^+ collector contact 25 thereto and an external electrical contact 26, provided for example by metallisation. The base of transistor 1 is comprised by two p^+ contact regions 27 and 27a joined by a p bridging region 28 with two external electrical contacts 26a and 26b as illustrated, and the emitter is comprised by an n^+ polysilicon region 29, which contacts the p region 28, there also being an external electrical contact (not shown) to the emitter.

The bipolar transistor 1 includes elements equalent to those of p-channel transistor 3 and manufactured concurrently therewith although the same bipolar structure may be manufactured independently thereof. The two extra masks required for the production of the polysilicon emitter transistor 1 are for defining the implant required to produce the base region 28 and for opening the "gate" oxide 30 to bring the polysilicon into contact with the base region 28. In Figs. 1 and 2 the gate oxide is indicated separately from the remaining isolating oxide 15 although it is formed concurrently with part of the isolating oxide 15 as will be more apparent from the description of Figs. 3 to 7.

Thus the bipolar device is fitted directly into n-well CMOS technology, the n-well being used as the collector. For use in a p-well technology an additional n implant, for example phosphorus or arsenic, is needed. This step can be implemented part of the way through the p-well drive in. Due to different thicknesses of oxides in the well and field areas a non-masked implant can be

used for the n-well, although a masked implant can alternatively be used. This produces an n-well 5 within the p-well 5' (stacked wells), which again is used as the collector region of the bipolar device, as illustrated in Fig. 2.

The basic processing stages employed to fabricate the structure of Fig. 1 will now be outlined with reference to Figs. 3 to 7. Using a first mask and photoresist (not shown) n-type wells 36 and 37 are defined in a p-type substrate 32, for example by ion implantation of phosphorous and subsequent driving-in in a conventional manner. Using a second mask (not shown) a layer of silicon nitride 31, or silicon nitride on silicon dioxide, deposited on the surface of the p-type silicon substrate 32 is patterned to distinguish between device areas and areas in which field oxide is to be grown. Areas of nitride 31 are left on the surface of the substrate 32 at positions corresponding to the device areas, as indicated in Fig. 3. Field dopant (not shown) may be implanted into the surface of substrate 32 by use of suitable masking through the windows opened in the nitride layer 31, by for example ion implantation of boron and/or phosphorous. The substrate is then oxidised in order to form field oxide 33 in the windows. The areas of nitride 31 are etched away and the substrate further oxidised in order to obtain thin oxide areas 34 between the thick field oxide areas 33 (Fig. 4). A third mask (not shown) is employed to define a window 40 in a photoresist layer 41 (Fig. 5), through which window p-type dopant, for example boron, is ion implanted to produce a base region 42 for the bipolar transistor. This third mask is one of the additional two masks referred to above. Using a fourth mask (not shown) and an appropriate photoresist layer a window 43 is opened in the thin oxide area covering base region 42. The

alignment is not critical as will be apparent from the following. If an interfacial oxide is required for the polysilicon transistor a suitable treatment can be used now. This fourth mask is the other additional mask. The photoresist is removed and a layer of undoped polycrystalline silicon deposited and ion implanted with As or P. It is then patterned to produce a polycrystalline emitter 44 and gates 45 and 46 (Fig. 6). Then with the polysilicon 44 and 45 together with certain areas of the thin oxide area protected by appropriate patterned photoresist 41a, p^+ dopant for example boron is implanted to provide base contact regions 47 for the bipolar device, the substrate contact 48 for the n-channel MOS transistor and the source and drain regions 49 and 50 for the p-channel MOS transistor. Using a further mask a layer of photoresist 51 is appropriately patterned to define windows whereby an n^+ dopant, for example arsenic, is ion implanted to provide collector contact 52 for the bipolar device, source and drain regions 53 and 54 for the n-channel MOS transistor and the well contact 55 for the p-channel MOS transistor (Fig. 7). The photoresist 51 is removed and the wafer is oxidised and a layer of P.S.G. (phosphosilicate glass) deposited to produce an "oxide" layer of the thickness of layer 15 of Fig. 1. Using another mask windows are opened in the oxide for the provision of the requisite electrical contacts to the underlying regions, the thus processed substrate is then, for example, metallised and the metal patterned as appropriate using yet another mask to produce a structure equivalent to Fig. 1. Further masking and processing may be employed as is conventional for threshold tailoring of the n-channel and p-channel MOS transistors.

By using the high efficiency polysilicon emitter structure the doping levels of the base and collector

regions of the bipolar transistor can be optimised to produce low base and collector series resistance whilst still achieving a high current gain. This latitude is not available in conventional bipolar transistors.

Whilst the source and drain regions of the CMOS transistors are produced in a fully aligned manner by virtue of the polysilicon gates, the emitter of the bipolar device is only semi self-aligned with the base comprised by regions 42 and 47, although the performance is not affected thereby.

Bipolar transistors with the structure illustrated in Fig. 1 and requiring only two additional masks to a conventional CMOS process have been manufactured and found to have very high performance. Thus this approach to the integration of bipolar and CMOS technologies provides devices capable of high performance analogue and digital functioning, the bipolar and CMOS transistors being formed simultaneously on the same chip.

The doped polycrystalline silicon may be manufactured by a process as described in our co-pending GB Application No. 8604278 (Serial No. 217844) (P.D. Scovell-R.L. Baker 11-3).

Attention is directed to GB Application No. 8612801 (Serial No. 2174244) which was divided from the present Application.

CLAIMS:-

1. An integrated circuit including an MOS transistor with a polycrystalline silicon gate and a bipolar transistor with a polycrystalline silicon emitter, which polycrystalline silicon gate and emitter have the same doping levels and were manufactured by simultaneous etching from a common single polycrystalline layer.

2. An integrated circuit as claimed in claim 1, including a plurality of said MOS transistors, wherein the MOS transistors are CMOS transistors with wells of one conductivity type formed in a substrate of the other conductivity type, wherein the bipolar transistor is constructed in a respective well of the one conductivity type which comprises the collector of the bipolar transistor, wherein base contacts of the bipolar transistor comprise first regions of said respective well converted to the other conductivity type, and formed simultaneously with source and drain regions of an MOS transistor of the CMOS transistors which is formed in a respective well of the one conductivity type, which first regions are connected by a bridging base region, and wherein the polycrystalline silicon emitter is in contact with the bridging base region via a window in an oxide layer underlying the polycrystalline silicon emitter.

3. An integrated circuit as claimed in claim 1, including a plurality of said MOS transistors, wherein the MOS transistors are CMOS transistors with wells of one conductivity type formed in a substrate of the other conductivity type, and wherein the bipolar transistor is constructed in a well of the other conductivity type disposed within a well of the one conductivity type, which well of the other conductivity type comprises the collector of the bipolar transistor, wherein base contacts of the bipolar transistor comprise second regions of said well of the other conductivity type

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converted to the one conductivity type, and formed simultaneously with source and drain regions of an MOS transistor of the CMOS transistors which is formed directly in the substrate, which second regions are connected by a bridging base region, and wherein the polycrystalline silicon emitter is in contact with the bridging base region via a window in an oxide layer underlying the polycrystalline silicon emitter.

4. An integrated circuit substantially as herein described with reference to Fig. 1 or Fig. 2 of the accompanying drawings.

5. A method of manufacturing an integrated circuit including bipolar and MOS transistors including the step of forming both an MOS transistor gate and a bipolar transistor emitter by etching simultaneously from a common single layer of polycrystalline silicon, the gate and the emitter having the same doping levels.

6. A method of manufacturing an integrated circuit as claimed in claim 5 wherein the MOS transistors are CMOS transistors and including the use of two masks in addition to those required to form the CMOS transistors, one said mask defining a window for the implantation of a base region of the bipolar transistor and the other said mask defining a window in an oxide layer covering the base region whereby the polycrystalline silicon emitter contacts the base region.

7. A method of manufacturing an integrated circuit as claimed in claim 5 wherein the MOS transistors are CMOS transistors with wells of one conductivity type formed in a substrate of the other conductivity type, wherein the bipolar transistor is constructed in a respective well of the one conductivity type, which comprises the collector of the bipolar transistor, simultaneously with the construction of the CMOS transistors and by the same processing steps as required for the MOS transistors of the CMOS transistors which are formed in the wells of one conductivity type except

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for the addition of a first processing stage to produce a bridging base region between two regions, equivalent to the source and drain regions of the MOS transistors in the wells of one conductivity type, whereby to form the base of the bipolar transistor, and a second processing stage to produce a window in an oxide layer underlying the polycrystalline layer at the bipolar transistor whereby the polycrystalline emitter contacts the base of the bipolar transistor.

8. A method of manufacturing an integrated circuit as claimed in claim 5 wherein the MOS transistors are CMOS transistors with wells of one conductivity type formed in a substrate of the other conductivity type, wherein the bipolar transistor is constructed in a well of the other conductivity type, which comprises the collector of the bipolar transistor, disposed in a well of the other conductivity type, the bipolar transistor being constructed simultaneously with the construction of the CMOS transistors and by the same processing steps as required for the MOS transistors of the CMOS transistors which are formed directly in the substrate except for the addition of a first processing stage to produce a bridging base region between two regions, equivalent to the source and drain regions of the MOS transistors in the substrate, whereby to form the base of the bipolar transistor, and a second processing stage to produce a window in an oxide layer under the polycrystalline layer at the bipolar transistor whereby the polycrystalline emitter contacts the base of the bipolar transistor.

9. A method of manufacturing an integrated circuit as claimed in claim 5 wherein the MOS transistors are CMOS transistors with wells of one conductivity type formed in a substrate of the opposite conductivity type, wherein the bipolar transistor is formed in a respective well of the one conductivity type simultaneously with the CMOS transistors and by the same processing steps,

the bipolar transistor fabrication involving the addition of two masking processes and one implantation process which serve to complete the construction of the bipolar transistor's base region and to obtain contact between the polycrystalline silicon emitter and the base region.

10. A method of manufacturing an integrated circuit substantially as herein described with reference to the accompanying drawings.

11. An integrated circuit made by a method as claimed in any one of claims 5 to 10.

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