Claims

1. A method of plasma processing, comprising:

receiving a substrate in a reaction chamber, wherein the reaction chamber comprises a grid structure dividing the interior of the reaction chamber into an upper sub-chamber proximate a plasma generator and a lower sub-chamber proximate a substrate holder;

flowing a plasma generating gas into the upper sub-chamber;

generating a first plasma in the upper sub-chamber from the plasma generating gas, the first plasma having a first electron density, and generating a second plasma in the lower sub-chamber, wherein the second plasma is an ion-ion plasma that has a second electron density at least about 10 times lower than the first electron density; and

processing the substrate with the second plasma to perform a step in a source drain recess etch comprising:

(a) performing a first etching process to etch the substrate in a vertical direction to form vertically etched features;

(b) performing a second etching process to etch the substrate in a horizontal direction within the vertically etched features;

(c) performing an oxidation process to form an oxidized layer within the vertically etched features; and

(d) repeating (a)-(c) at least once to form source drain recesses in the vertically etched features,

wherein the first etching process, second etching process and oxidation process are all performed in the reaction chamber having the grid structure such that the second plasma in each process is an ion-ion plasma.

2. The method of claim 1, wherein the first plasma has a first electron temperature of about 2 eV or more, and wherein the second plasma has a second effective electron temperature of about 1 eV or less.

3. The method of claim 1, wherein the second electron density is about $5\times10^{9}\ cm^{-3}$ or less.

4. The method of claim 1, wherein the ratio of negative ions:positive ions in the second plasma is between about 0.5-1.

5. The method of claim 1, wherein the vertically etched features have a reentrant shape after (c).

6. The method of claim 1, wherein the first etching process in (a) is performed with a first plasma generating gas, wherein the second etching process in (b) is performed with a second plasma generating gas, wherein a composition of the first plasma generating gas is different from a composition of the second plasma generating gas, and wherein the oxidation process in (c) is performed with a third plasma generating gas comprising oxygen.

7. The method of claim 6, wherein the first plasma generating gas comprises Cl_2, and wherein the second plasma generating gas comprises NF_3 and Cl_2.

8. A method of plasma processing, comprising:

receiving a substrate in a reaction chamber, wherein the reaction chamber comprises a grid structure dividing the interior of the reaction chamber into an upper sub-chamber proximate a plasma generator and a lower sub-chamber proximate a substrate holder;

flowing a plasma generating gas into the upper sub-chamber;

generating a first plasma in the upper sub-chamber from the plasma generating gas, the first plasma having a first electron density, and generating a second plasma in the lower sub-chamber, wherein the second plasma is an ion-ion plasma that has a second electron density at least about 10 times lower than the first electron density, and wherein the first plasma is an inductively coupled plasma; and

processing the substrate with the second plasma to perform a shallow trench isolation etch,

wherein the substrate is biased to between about 300-1200 V during the etch.

9. The method of claim 8, wherein the etching process involves simultaneously etching at least a first feature shape and a second feature shape, the first feature shape having an aspect

ratio of about 10 or higher and the second feature shape having an aspect ratio of about 1 or lower,

wherein after etching, an etch depth of the first feature is at least about 95% the etch depth of the second feature.

10. The method of claim 9, wherein after etching, the first feature has an etching profile of at least about 88°, and the second feature has an etching profile of at least about 85°.

11. The method of claim 8, wherein the first plasma has a first electron temperature of about 2 eV or more, and wherein the second plasma has a second effective electron temperature of about 1 eV or less.

12. The method of claim 8, wherein the second electron density is about 5×10^{9} cm^{-3} or less.

13. The method of claim 8, wherein the ratio of negative ions:positive ions in the second plasma is between about 0.5-1.

14. The method of claim 8, further comprising pulsing the bias applied to the substrate.

15. The method of claim 8, wherein the bias applied to the substrate is a DC bias.

16. A method of etching polysilicon on a partially fabricated integrated circuit to define a FinFET gate region, comprising:

(a) receiving a substrate having a layer of polysilicon thereon in a reaction chamber, wherein the reaction chamber comprises a grid structure dividing the interior of the reaction chamber into an upper sub-chamber proximate a plasma generator and a lower sub-chamber proximate a substrate holder;

(b) flowing a plasma generating gas into the upper sub-chamber;

(c) generating a first plasma in the upper sub-chamber from the plasma generating gas, and generating a second plasma in the lower sub-chamber, wherein the second plasma is an ion-ion plasma;

(d) etching the polysilicon layer provided on the substrate to thereby define a FinFET gate region, and

(e) repeating (a)-(d), wherein during a first iteration of (a)-(d), the plasma generating gas is a first plasma generating gas having a first composition, wherein during a second iteration of (a)-(d), the plasma generating gas is a second plasma generating gas having a second composition, and wherein the first composition is different than the second composition.

17. The method of claim 16, wherein etching the polysilicon layer in (d) forms cavities in locations that will be proximate a FinFET gate in a completed integrated circuit.

18. The method of claim 17, wherein a pressure in the reaction chamber during the etching is between about 5-20 mTorr.

19. The method of claim 17, wherein there is substantially no etching profile loading between on-fin regions and off-fin regions.

20. The method of claim 19, wherein sidewalls of the etched regions do not become recessed during etching.

21. The method of claim 17, wherein a mask layer positioned above the polysilicon layer reduces in thickness by less than about 10% during the etching in (d).

22. The method of claim 16, wherein etching the polysilicon layer in (d) forms cavities in locations where a FinFET gate will be positioned in a completed integrated circuit.

23. The method of claim 22, wherein the first plasma generating gas comprises HBr, and the second plasma generating gas comprises Cl_2, and wherein the first and second plasma generating gases are substantially free of oxygen-containing reactants.

24. The method of claim 23, wherein a pressure in the reaction chamber is between about 20-80 mTorr during the first iteration, and wherein the pressure in the reaction chamber is between about 4-80 mTorr during the second iteration.

25. The method of claim 16, wherein an effective electron temperature in the second plasma is about 1 eV or less, and is less than an effective electron temperature in the first plasma.

26. The method of claim 25, wherein an electron density in the second plasma is about 5×10^{9} cm^{-3} or less, and is less than an electron density in the first plasma.

27. The method of claim 16, wherein the grid structure comprises two or more grids, at least one of which is movable relative to the others.

28. The method of claim 16, wherein the first plasma is a continuous wave plasma.

29. The method of claim 16, wherein there is substantially no etching profile loading between etched features positioned on the substrate at locations having different feature densities.

30. The method of claim 15, wherein a pressure in the reaction chamber is between about 20-80 mTorr during the first iteration of (a)-(d), and wherein the pressure in the reaction chamber is between about 4-80 mTorr during the second iteration of (a)-(d).