

SEMICONDUCTOR STRUCTURE FOR DIGITAL AND RADIOFREQUENCY APPLICATIONS

5 TECHNICAL FIELD OF THE INVENTION

The present invention relates to a semiconductor-on-insulator structure for digital and radiofrequency applications. The invention also relates to a process for fabricating such a structure via transfer of a layer from a first substrate, called the "donor substrate", to a second substrate, called the "receiver substrate".

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PRIOR ART

Semiconductor-on-insulator structures are multilayer structures comprising a substrate, which is generally made of silicon, an electrically insulating layer arranged on top of the substrate, which is generally a layer of oxide such as a layer of silicon oxide, and, arranged on top of the insulating layer, a semiconductor layer in which the source, the channel and drain of the transistors are produced and which is generally a layer of silicon.

Semiconductor-on-insulator (SeOI) structures are referred to as "silicon-on-insulator" (SOI) structures when the semiconductor is silicon.

Among existing SOI structures, fully-depleted silicon-on-insulator (FD-SOI) structures are commonly used for digital applications. FD-SOI structures are characterized by the presence of a thin oxide layer, arranged on a silicon substrate, and of a very thin semiconductor layer called the SOI layer arranged on the oxide layer.

The oxide layer is located between the substrate and the SOI layer. The oxide layer is then said to be "buried", and is called the "BOX" for Buried OXide.

25 The SOI layer allows the conduction channel to be formed in the FD-SOI structure.

Because of the small thickness and of the uniformity of the BOX layer and of the SOI layer, it is not necessary to dope the conduction channel, and hence the structure is able to operate in a fully depleted mode.

FD-SOI structures have improved electrostatic characteristics with respect to structures without BOX layers. The BOX layer decreases the parasitic electrical capacitance between the source and drain, and also allows leakage of electrons from the conduction channel to the substrate to be considerably decreased by combining the flow of electrons to the conduction channel, thus decreasing current losses and improving the performance of the structure.

35 FD-SOI structures can be compatible with radiofrequency (RF) applications, but however suffer from the appearance of electrical losses in said substrate.

To compensate for these electrical losses and improve RF performance, it is known to use a substrate, in particular an SOI substrate, having a high electrical resistivity, this

type of substrate commonly being referred to as an “HR substrate” for high-resistivity substrate. The latter is advantageously combined with a charge-trapping layer, i.e. a trap-rich layer. However, this type of substrate is incompatible with use of transistors the threshold voltage of which may be controlled via a back-side gate (back bias voltage).

5 Specifically, the presence of this layer containing trapped charges hinders back biasing (application of a potential difference to the back side) and may furthermore lead to an accelerated diffusion of dopants, thus preventing the production of high-quality PN junctions, because of problems with junction leakage.

10 Apart from FD-SOI structures comprising one BOX layer, FD-SOI structures comprising two BOX layers, which are called “double BOX” structures, have been produced.

The double-BOX technology is advantageous in the case where the FD-SOI structure comprises double-gate transistors the gate electrodes of which are formed both above and below the conduction channel. Thus, the SOI layer of the back gate, which is called the back-gate SOI layer, is electrically separated from the SOI layer of the front gate, which is called the front-gate SOI layer, by a first BOX layer, and is also electrically separated from
15 the basic substrate by a second BOX layer.

Document US 2010/0176482 describes an example of such an FD-SOI structure comprising two BOX layers, for a CMOS technology.

20 According to this document, CMOS structures with a high-k gate dielectric and with a gate length of as small as 30 nm are fabricated using an optimised process allowing a good isolation between the devices and the back gate to be obtained.

The existing double-BOX technology is used for digital applications, and not both for radiofrequency and digital applications.

25 **BRIEF DESCRIPTION OF THE INVENTION**

One aim of the invention is to provide a semiconductor-on-insulator structure allowing the aforementioned drawbacks to be overcome. The invention aims to provide such a structure allowing digital applications and radiofrequency applications to be combined.

To this end, the invention provides a semiconductor-on insulator structure comprising:

- 30 - a stack, called the back stack, of the following layers from a back side to a front side of the structure:
- a semiconductor carrier substrate the electrical resistivity of which is comprised between 500 Ω .cm and 30 k Ω .cm,
 - a first electrically insulating layer,
 - 35 • a first semiconductor layer,
- at least one trench isolation that extends through the back stack at least down to the first electrically insulating layer, and that electrically isolates two adjacent regions of the multilayer structure,

the multilayer structure mainly being characterized in that it furthermore comprises:

- at least one FD-SOI first region comprising a stack, called the front stack, arranged on the back stack, said front stack comprising:
 - a second electrically insulating layer arranged on the first semiconductor layer,
 - a second semiconductor layer called the active layer, arranged on the second electrically insulating layer,
 wherein the first electrically insulating layer has a thickness larger than that of the second electrically insulating layer, and the first semiconductor layer has a thickness larger than that of the active layer, said FD-SOI first region furthermore comprising at least one digital component in the active layer,
- at least one RF-SOI second region electrically isolated from the FD-SOI region by a trench isolation, comprising at least one radiofrequency component plumb with the first electrically insulating layer.

According to other aspects, the proposed structure has the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the back stack furthermore comprises a charge-trapping layer arranged between the carrier substrate and the first electrically insulating layer;
- the charge-trapping layer is made of polysilicon or of porous silicon;
- the radiofrequency component is arranged in the first semiconductor layer;
- the RF-SOI second region comprises the front stack arranged on the back stack, and wherein the radiofrequency component is arranged in the active layer;
- the first semiconductor layer is made of crystalline material;
- the first semiconductor layer is made of amorphous material;
- the second semiconductor layer is made of crystalline material;
- the first electrically insulating layer is a layer of silicon oxide;
- the second electrically insulating layer is a layer of silicon oxide;
- the first electrically insulating layer has a thickness comprised between 50 nm and 1500 nm;
- the second electrically insulating layer has a thickness comprised between 10 nm and 100 nm;
- the first semiconductor layer has a thickness comprised between 10 nm and 200 nm;
- the active layer has a thickness comprised between 3 nm and 30 nm.

The invention also relates to a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- providing a first donor substrate,
- forming a weakened zone in said first donor substrate, so as to delineate a first semiconductor layer,
- 5 - transferring said first semiconductor layer to a semiconductor carrier substrate, a first electrically insulating layer being at the interface between the donor substrate and the carrier substrate so as to form a back stack comprising the carrier substrate, the first electrically insulating layer and the transferred first semiconductor layer,
- providing a second donor substrate,
- 10 - forming a weakened zone in said second donor substrate, so as to delineate a second semiconductor layer, called the active layer,
- transferring said semiconductor layer to the back stack, a second electrically insulating layer being at the interface between the second donor substrate and the back stack, so as to form a front stack comprising the second electrically insulating layer and the transferred second semiconductor layer,
- 15 - forming at least one trench isolation that extends through the front stack and through the back stack at least down to the first electrically insulating layer, in order to electrically isolate two adjacent regions, including at least one FD-SOI region and at least one RF-SOI region,
- 20 - producing:
 - at least one digital component in the active layer, in the FD-SOI region, and
 - at least one radiofrequency component plumb with the first electrically insulating layer.

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The invention also relates to a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- forming a back stack by depositing a first semiconductor layer on a carrier substrate covered with a first electrically insulating layer,
- 30 - providing a donor substrate,
- forming a weakened zone in said donor substrate, so as to delineate a second semiconductor layer,
- transferring said second semiconductor layer to the back stack, a second electrically insulating layer being at the interface between the second donor substrate and the back stack, so as to form a front stack on the back stack,
- 35 - forming at least one trench isolation that extends through the front stack and through the back stack at least down to the first electrically insulating layer, in

order to electrically isolate two adjacent regions, including at least one FD-SOI region and at least one RF-SOI region,

- producing:

- at least one digital component in the active layer, in the FD-SOI region, and
- at least one radiofrequency component plumb with the first electrically insulating layer.

According to other aspects, the proposed processes have the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the method comprises, before the radiofrequency component is produced, a step of selectively removing the active layer and the second electrically insulating layer of the RF-SOI region, and wherein the radiofrequency component is then formed in the first semiconductor layer;
- the process furthermore comprises, before the transferring step, forming a charge-trapping layer on the receiver substrate, said charge-trapping layer being arranged between the carrier substrate and the first electrically insulating layer.

The multilayer structure of the invention serves as carrier for the fabrication of transistors, in particular MOSFETs. MOSFETs are semiconductor devices comprising three active electrodes, namely an input electrode called the gate, an output electrode called the drain, and a third electrode called the source. These transistors allow a voltage (or a current) output on the drain to be controlled by virtue of the gate.

In the present text, the term “on”, when it relates to the position of a first layer with respect to a second layer, or the position of a component with respect to a layer, does not necessarily imply that the first layer makes direct contact with the second or that the component makes direct contact with the layer. Unless otherwise specified, this term does not exclude one or more other layers being intermediate between the first layer and second layer, or between the component and the layer.

DESCRIPTION OF THE FIGURES

Other advantages and features of the invention will become apparent upon reading the following description given by way of illustrative and non-limiting example, with reference to the following appended figures:

Figure 1 is a schematic of a first embodiment of a multilayer structure according to the invention, comprising two FD-SOI regions and one RF-SOI region, in which a digital component is produced in the active layer of the FD-SOI regions and a radiofrequency component is produced in the active layer of the RF-SOI region;

Figure 2 is a schematic of a second embodiment of a multilayer structure according to the invention, comprising two FD-SOI regions and one RF-SOI region, in which a digital

component is produced in the active layer of the FD-SOI regions and a radiofrequency component is produced in the first semiconductor layer of the RF-SOI region;

Figure 3A is a schematic illustrating the formation of a weakened zone in a first donor substrate;

5 Figure 3B is a schematic of a back stack obtained after bonding the first semiconductor layer to the receiver substrate;

Figure 3C is a schematic illustrating the formation of a weakened zone in a second donor substrate;

10 Figure 3D is a schematic of a structure obtained after bonding the second semiconductor layer to the back stack;

Figure 3E shows a multilayer structure obtained using the fabricating process according to a first embodiment;

Figure 4A shows a multilayer structure in which a segment of the active layer and of the second electrically insulating layer has been locally removed to form a cavity;

15 Figure 4B shows the structure of Figure 4A, obtained using the fabricating process according to a second embodiment;

Figure 5A shows a structure equipped with trench isolations;

20 Figure 5B shows the structure of Figure 5A, in which a lateral segment of the first semiconductor layer has been locally removed in order to form a cavity, according to a third embodiment of the fabricating process;

Figure 5C shows the structure of Figure 5B, in which the cavity has been filled with a third electrically insulating layer.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

25 A first subject of the invention relates to a semiconductor-on-insulator multilayer structure that is usable both for digital applications and for radiofrequency applications.

Figure 1 illustrates a first embodiment of such a multilayer structure 1 according to the invention.

30 With reference to Figure 1, the multilayer structure 1 comprises a stack, called the back stack, from a back side to a front side of the structure, of a semiconductor carrier substrate 2, a first electrically insulating layer 3, and a first semiconductor layer 4.

35 The semiconductor carrier substrate 2 is a highly resistive substrate, i.e. it has an electrical resistivity comprised between 500 Ω .cm and 30 k Ω .cm, and preferably comprised between 1 k Ω .cm and 10 k Ω .cm. A high resistivity gives the carrier substrate the ability to limit electrical losses and to improve the radiofrequency performance of the structure.

The first electrically insulating layer 3 allows the carrier substrate 2 to be insulated from the first semiconductor layer 4 and from the layers superjacent said first semiconductor layer.

The first electrically insulating layer 3 is preferably a layer of oxide. Since this layer is buried in the structure between the carrier substrate 2 and the first semiconductor layer 4, it may also be called the “first BOX”. It is preferably a layer of silicon oxide.

5 The thickness of the first electrically insulating layer 3 is relatively large, and preferably comprised between 50 nm (nanometres) and 1500 nm. Specifically, too small a thickness, in particular one smaller than 50 nm, would run the risk of breakdown in the first electrically insulating layer.

10 Optionally, the structure 1 also comprises a charge-trapping layer 7, which is preferably made of polysilicon or of porous silicon, arranged between the carrier substrate 2 and the first electrically insulating layer 3. This charge-trapping layer allows the electrical charge that accumulates under the first electrically insulating layer 3 to be trapped.

15 The first semiconductor layer 4 is an intermediate layer arranged between the first electrically insulating layer 3 and a second electrically insulating layer 5, which is described in more detail below in the present text. It preferably has a thickness comprised between 10 nm and 200 nm.

The semiconductor layer 4 is advantageously made of a crystalline material or of an amorphous material, which may optionally be doped in the FD-SOI regions. This material is chosen so that the semiconductor layer in the FD-SOI regions can be biased in order to control the threshold voltage of the transistor (back bias voltage).

20 Preferably, the material of the semiconductor layer 4 is not doped in the RF-SOI regions in order to optimize the electrical resistivity of the back stack and to thus limit electrical losses.

The material of the semiconductor layer 4 is preferably chosen from: single-crystal silicon, polysilicon, and silicon-germanium.

25 The multilayer structure 1 comprises a plurality of regions intended for different applications, including at least one FD-SOI region for digital applications and at least one RF-SOI region for radiofrequency applications.

30 In order to be able to combine an FD-SOI region and an RF-SOI region in one and the same structure, the nature of the constituent layers of the stack located on the first semiconductor layer, called the front stack, is different depending on whether said stack forms part of an FD-SOI region or of an RF-SOI region.

35 According to the first embodiment illustrated in Figure 1, the two FD-SOI regions and the RF-SOI region comprise the same front stack. This front stack comprises a second electrically insulating layer 5 arranged on the first semiconductor layer 4, and a second semiconductor layer 6 called the active layer arranged on the second electrically insulating layer 5.

The structure 1 furthermore comprises trench isolations 8 that extend from the free surface of the active layer 6, through the thickness of the structure. The trenches pass

through the active layer 6 and the second electrically insulating layer 5 of the front stack, and extend through the back stack at least down to the first electrically insulating layer 3. The trenches may extend more deeply into the back stack, so as to pass through the charge-trapping layer 7 when the latter is present, and the carrier substrate 2.

5 Each trench isolation electrically isolates two adjacent regions of the structure 1. A trench thus separates two FD-SOI regions, or two RF-SOI regions, or indeed one FD-SOI region and one RF-SOI region.

In the structure of Figure 1, the second electrically insulating layer 5 extends, over the first semiconductor layer 4, both into the FD-SOI regions and into the RF-SOI region.

10 The second electrically insulating layer 5 allows the active layer 6 to be insulated from the first semiconductor layer 4 and from the layers subjacent the intermediate layer.

The second electrically insulating layer 5 is preferably a layer of oxide. Since this layer is buried in the structure between the first semiconductor layer 4 and the active layer 6, it may also be called the "second BOX". It is preferably a layer of silicon oxide.

15 The active layer 6 has a thickness that is relatively small, and smaller than that of the first electrically insulating layer 3. This small thickness makes it possible to be able to control the threshold voltage of the transistor via suitable biasing of the subjacent first semiconductor layer. A thickness of the second electrically insulating layer 5 preferably comprised between 10 nm and 100 nm is selected to this end.

20 The second semiconductor layer 6 is called the active layer because it is intended for the production both of digital components 9 and of radiofrequency components 10, the components produced depending on the digital and radiofrequency applications desired for the structure.

25 The active layer 6 is preferably made of crystalline material, and more preferably is a layer of single-crystal silicon.

The thickness of the active layer 6 is preferably comprised between 3 nm and 30 nm, and more preferably between 5 nm and 20 nm. It is preferable for the thickness of the active layer to be uniform over all the extent of the material, i.e. for its thickness to vary by 1 nm or less, in order to optimize the operation of the FD-SOI regions, in a fully depleted mode.

30 According to the first embodiment shown in Figure 1, the radiofrequency components are produced on the front stack and in the active layer 6.

Figure 2 illustrates a second embodiment of the multilayer structure 1 according to the invention.

35 This second embodiment differs from the first in that the front stack described above is present solely in the FD-SOI regions, and the radiofrequency components are arranged directly in the first semiconductor layer 4 of the RF-SOI region.

With reference to Figure 2, the RF-SOI region thus comprises neither the second electrically insulating layer 5 arranged on the first semiconductor layer 4, nor the active layer

6 arranged on the second electrically insulating layer 5. Specifically, the first electrically insulating layer 3 already allows, without the presence of the second electrically insulating layer 5, a structure that is resistive enough to limit electrical losses to be obtained.

5 Three embodiments of a process for fabricating a multilayer structure 1 such as described above will now be described.

According to a first embodiment, a first donor substrate 20 is initially provided.

10 With reference to Figure 3A, a weakened zone 21 is formed in this substrate, so as to delineate a first semiconductor layer 4. The weakened zone 21 is formed in the donor substrate at a predefined depth that corresponds substantially to the thickness of the semiconductor layer to be transferred. Preferably, the weakened zone 21 is created by implanting hydrogen and/or helium atoms into the donor substrate 20.

15 The first semiconductor layer 4 is then transferred to a semiconductor carrier substrate 2, which is a receiver substrate, by bonding the donor substrate 20 to the carrier substrate via the first electrically insulating layer 3 then by detaching the donor substrate along the weakened zone 21 (Smart Cut™ process). The first electrically insulating layer may be formed on the donor substrate or on the carrier substrate.

Alternatively, the transfer may be achieved by thinning the donor substrate 21 from the side thereof opposite the side bonded to the carrier substrate 2, until the thickness desired for the first semiconductor layer 4 is obtained.

20 Optionally, before the bonding step, a charge-trapping layer 7 is formed on the carrier substrate 2, between the carrier substrate and the first electrically insulating layer 3.

A back stack, such as described above and shown in Figure 3B, comprising the carrier substrate 2, the charge-trapping layer 7 when present, the first electrically insulating layer 3 and the transferred first semiconductor layer 4, is then obtained.

25 Moreover, a second donor substrate 30 is provided.

With reference to Figure 3C, a weakened zone 31 is formed in this substrate, so as to delineate a second semiconductor layer 6. The weakened zone may be formed in the same way used to delineate the first semiconductor layer.

30 The second semiconductor layer 6 is then transferred to the back stack, which forms a receiver substrate, by bonding the second donor substrate to the back stack via the second electrically insulating layer 5 then by detaching the donor substrate along the weakened zone (Smart Cut™ process). The second electrically insulating layer 5 may be formed on the donor substrate or on the receiver substrate.

35 With reference to Figure 3D, a front stack positioned on the back stack and comprising the second electrically insulating layer 5 and the second semiconductor layer 6, is then obtained.

Alternatively, the transfer may be achieved by thinning the second donor substrate 30 from the side thereof opposite the side bonded to the back stack, until the thickness desired for the second semiconductor layer 6 is obtained.

5 Optionally, before the transferring step, it is possible to carry out a treatment of the free surface of the first semiconductor layer in order to decrease the roughness thereof. This surface treatment improves the bonding of the second electrically insulating layer to the first semiconductor layer.

10 With reference to Figure 3E, the trench isolations 8, which extend through the front stack and through the back stack at least down to the first electrically insulating layer 3, are then formed, in order to electrically isolate two adjacent regions, in particular an FD-SOI region and an RF-SOI region.

15 In the case where it is desired to obtain the structure of Figure 2, before the radiofrequency components 10 are produced and preferably before the digital components 9 are produced, a segment of the active layer 6 and of the second electrically insulating layer 5 of the RF-SOI regions is selectively removed in order to form a cavity 11. This is shown in Figure 4A.

20 The local removal may advantageously be carried out by etching. To this end, a lithography mask is deposited on the active layer 6. The mask is provided with at least one aperture. The active layer 6 is then etched through the aperture of the mask in order to form the cavity 11. Any known etching technique suitable for this purpose is usable, such as for example dry etching with hydrochloric acid.

 The digital components 9 are produced on the second semiconductor layer 6, which is the active layer. This allows an FD-SOI region to be obtained.

25 The radiofrequency components 10 are also produced, on the first semiconductor layer. The radiofrequency components may be produced in the active layer 6 (Figure 1) or in the first semiconductor layer 4 (Figure 2 and Figure 4B). This allows an RF-SOI region to be obtained.

30 The first embodiment that has just been described comprises two steps of delineating and transferring a semiconductor layer. This is most particularly advantageous in the case where the first semiconductor layer is crystalline. The transfer of such a layer from a donor substrate allows its crystal quality to be preserved on the final structure.

35 When an optimization of the crystal quality of the first semiconductor layer is not required, for example when the latter is amorphous, it is possible to form the first semiconductor layer by deposition on the first electrically insulating layer. This process then employs only a single transferring step, i.e. the step of transferring the active layer, and is therefore more economical.

 This method corresponds to a second embodiment that will now be described.

According to a second embodiment, a back stack is formed by depositing a first semiconductor layer 4 on a carrier substrate 2 covered beforehand with a first electrically insulating layer 3. This back stack is illustrated in Figure 3B.

The first semiconductor layer 4 may be formed by epitaxy on the carrier substrate, or
 5 alternatively deposited on said carrier substrate in particular by chemical vapour deposition (CVD).

Optionally, before the deposition of the first semiconductor layer, a charge-trapping layer 7 is formed on the carrier substrate 2, between the carrier substrate and the first electrically insulating layer 3.

10 Moreover, a donor substrate 30 is provided.

With reference to Figure 3C, a weakened zone 31 is formed in this donor substrate, so as to delineate a second semiconductor layer 6. The weakened zone may be formed in the same way used for the first embodiment.

The second semiconductor layer 6 is then transferred to the back stack by bonding
 15 the donor substrate to the back stack via the second electrically insulating layer 5 then by detaching the donor substrate along the weakened zone (Smart Cut™ process).

With reference to Figure 3D, a front stack positioned on the back stack and comprising the second electrically insulating layer 5 and the second semiconductor layer 6, is then obtained.

20 Alternatively, the transfer may be achieved by thinning the donor substrate 30 from the side thereof opposite the side bonded to the back stack, until the thickness desired for the second semiconductor layer 6 is obtained.

Optionally, before the transferring step, it is possible to carry out a treatment of the free surface of the first semiconductor layer in order to decrease the roughness thereof.
 25 This surface treatment improves the bonding of the second electrically insulating layer to the first semiconductor layer, this being particularly advantageous when, as in the present embodiment, the first semiconductor layer is formed by deposition and not by Smart-Cut™ transfer.

With reference to Figure 3E, the trench isolations 8, which extend through the front
 30 stack and through the back stack at least down to the first electrically insulating layer 3, are then formed, in order to electrically isolate two adjacent regions, in particular an FD-SOI region and an RF-SOI region.

In the case where it is desired to obtain the structure of Figure 2, before the radiofrequency components 10 are produced and preferably before the digital components
 35 9 are produced, a segment of the active layer 6 and of the second electrically insulating layer 5 of the RF-SOI regions is selectively removed in order to form a cavity 11. This is shown in Figure 4A.

The local removal may advantageously be carried out by etching, similarly to the first embodiment.

The digital components 9 are produced on the second semiconductor layer 6, which is the active layer. This allows an FD-SOI region to be obtained.

5 The radiofrequency components 10 are also produced on the first semiconductor layer. The radiofrequency components may be produced in the active layer 6 (Figure 1) or in the first semiconductor layer 4 (Figure 2 and Figure 4B). This allows an RF-SOI region to be obtained.

10 **According to a third embodiment**, the fabricating process comprises the same steps as those of the first embodiment or those of the second embodiment, in order to form the structure of Figure 1 comprising the semiconductor carrier substrate 2, the first electrically insulating layer 3, the first semiconductor layer 4, the second electrically insulating layer 5 and the active layer 6. This structure is shown in Figure 5A.

15 However, contrary to these two embodiments, a segment of the first semiconductor layer 4 is removed locally. This local removal may be carried out before the radiofrequency components 10 and optionally the digital components are produced on the active layer 6, or indeed after the radiofrequency components 10 and optionally the digital components have been produced on the active layer 6, i.e. during the fabrication of the transistor. It may in particular be a question of a MOS transistor, such as a CMOS transistor.

20 According to this third embodiment, with reference to Figure 5A, a trench 8 is dug at a defined distance from the edge of the structure, so that the trench extends from the free surface of the active layer 6, through the second electrically insulating layer 5 and the first semiconductor layer 4, down to the first electrically insulating layer 3. This allows the lateral segment delineated by the trench 8 to be physically isolated from the rest of the structure.

25 With reference to Figure 5B, the first semiconductor layer 4 in the lateral segment is then locally removed in order to form a cavity 12.

30 The cavity 12 is a lateral cavity, located on the edge of the useful zone, and opens onto the exterior of the structure. It is bounded in the thickness of the structure by the first electrically insulating layer 3 and the second electrically insulating layer 5, and laterally by the trench 8.

With reference to Figure 5C, a third electrically insulating layer 13 is then deposited in the cavity 12, in order to fill the cavity.

35 One or more radiofrequency components 10 may then be produced on the active layer 6, plumb with the third electrically insulating layer 7. An RF-SOI region is then obtained on the structure edge. The expression "plumb with", which relates to the position of a component with respect to a layer within a structure, means that the component and the layer face each other in the direction of the thickness of the structure. In other words, any

axis that extends through the thickness of the structure and that intercepts the component, also intercepts the layer plumb with this component.

The advantage of producing the third electrically insulating layer during the process for fabricating the transistor is that it makes it possible to use the etch masks of this process
5 and therefore to benefit from an optimal alignment of the various layers of the structure.

According to a fourth embodiment (not shown), the active layer 6, the second electrically insulating layer 5 and the first semiconductor layer 4 are removed locally, so as to form a cavity.

A trench 8 may be dug beforehand in the structure, so that the trench extends from
10 the free surface of the active layer 6, through the second electrically insulating layer 5 and the first semiconductor layer 4, down to the first electrically insulating layer 3. This allows the segment of interest delineated by the trench 8 to be physically isolated from the rest of the structure.

Next, the cavity is filled with an oxide, then passive radiofrequency components
15 (inductors, capacitors, conduction lines) are produced on the oxide layer formed.

These passive radiofrequency components do not require a semiconductor such as silicon. They are produced in the back stack of the circuit, with metal lines (in a dielectric layer for example). Given that these passive RF components are negatively impacted by electrically conductive materials, they greatly benefit from the high-resistivity substrate and
20 from the charge-trapping layer, and from the removal of the semiconductor layers.

According to a fifth embodiment (not shown) a trench 8 is dug in the structure, so that the trench extends from the free surface of the active layer 6, through the second electrically insulating layer 5 and the first semiconductor layer 4, down to the first electrically insulating layer 3. This allows the segment of interest delineated by the trench 8 to be physically
25 isolated from the rest of the structure.

The active layer 6, the second electrically insulating layer 5 and the first semiconductor layer 4 are removed locally, so as to form a cavity.

Next, passive radiofrequency components are produced in the trench. To this end, it is preferable for the active layer 6 and the second electrically insulating layer 5 to not be too
30 thick. A thickness comprised between 3 nm and 30 nm for the active layer 6 and a thickness comprised between 10 nm and 100 nm for the second electrically insulating layer 5 are suitable for this purpose.

Just like the third embodiment, these embodiments have the advantage of using the etch masks of the process for fabricating the transistor, and therefore of benefiting from an
35 optimal alignment of the various layers of the structure.

CLAIMS

1. Semiconductor-on-insulator multilayer structure (1), comprising:
 - a stack, called the back stack, of the following layers from a back side to a front side of the structure:
 - a semiconductor carrier substrate (2) the electrical resistivity of which is comprised between 500 Ω .cm and 30 k Ω .cm,
 - a first electrically insulating layer (3),
 - a first semiconductor layer (4),
 - at least one trench isolation (8) that extends through the back stack at least down to the first electrically insulating layer (3), and that electrically isolates two adjacent regions of the multilayer structure,
 - the multilayer structure (1) being characterized in that it furthermore comprises:
 - at least one FD-SOI first region comprising a stack, called the front stack, arranged on the back stack, said front stack comprising:
 - a second electrically insulating layer (5) arranged on the first semiconductor layer (4),
 - a second semiconductor layer (6) called the active layer, arranged on the second electrically insulating layer (5),
 - wherein the first electrically insulating layer (3) has a thickness larger than that of the second electrically insulating layer (5), and the first semiconductor layer (4) has a thickness larger than that of the active layer (6), said FD-SOI first region furthermore comprising at least one digital component (9) in the active layer (6),
 - at least one RF-SOI second region electrically isolated from the FD-SOI region by a trench isolation (8), comprising at least one radiofrequency component (10) plumb with the first electrically insulating layer (3).
2. Structure (1) according to Claim 1, wherein the back stack furthermore comprises a charge-trapping layer (7) arranged between the carrier substrate (2) and the first electrically insulating layer (3).
3. Structure (1) according to Claim 2, wherein the charge-trapping layer (7) is made of polysilicon or of porous silicon.
4. Structure (1) according to one of Claims 1 to 3, wherein the radiofrequency component (10) is arranged in the first semiconductor layer (4).

5. Structure (1) according to one of Claims 1 to 3, wherein the RF-SOI second region comprises the front stack arranged on the back stack, and wherein the radiofrequency component (10) is arranged in the active layer (6).
- 5 6. Structure (1) according to one of the preceding claims, wherein the first semiconductor layer (4) is made of crystalline material.
7. Structure (1) according to one of the Claims 1 to 5, wherein the first semiconductor layer (4) is made of amorphous material.
- 10 8. Structure (1) according to one of the preceding claims, wherein the second semiconductor layer (6) is made of crystalline material.
9. Structure (1) according to one of the preceding claims, wherein the first electrically insulating layer (3) is a layer of silicon oxide.
- 15 10. Structure (1) according to one of the preceding claims, wherein the second electrically insulating layer (5) is a layer of silicon oxide.
- 20 11. Structure (1) according to one of the preceding claims, wherein the first electrically insulating layer (3) has a thickness comprised between 50 nm and 1500 nm.
- 25 12. Structure (1) according to one of the preceding claims, wherein the second electrically insulating layer (5) has a thickness comprised between 10 nm and 100 nm.
- 30 13. Structure (1) according to one of the preceding claims, wherein the first semiconductor layer (4) has a thickness comprised between 10 nm and 200 nm.
14. Structure (1) according to one of the preceding claims, wherein the active layer (6) has a thickness comprised between 3 nm and 30 nm.
- 35 15. Process for fabricating a semiconductor-on-insulator multilayer structure (1), comprising the following steps:
 - providing a first donor substrate,
 - forming a weakened zone in said first donor substrate, so as to delineate a first semiconductor layer (4),
 - 40 - transferring said first semiconductor layer (4) to a semiconductor carrier substrate (2), a first electrically insulating layer (3) being at the interface

between the donor substrate and the carrier substrate so as to form a back stack comprising the carrier substrate (2), the first electrically insulating layer (3) and the transferred first semiconductor layer (4),

- providing a second donor substrate,
- 5 - forming a weakened zone in said second donor substrate, so as to delineate a second semiconductor layer (6), called the active layer,
- transferring said semiconductor layer (6) to the back stack, a second electrically insulating layer (5) being at the interface between the second donor substrate and the back stack, so as to form a front stack comprising the
- 10 second electrically insulating layer (5) and the transferred second semiconductor layer (6),
- forming at least one trench isolation (8) that extends through the front stack and through the back stack at least down to the first electrically insulating layer (3), in order to electrically isolate two adjacent regions, including at least one
- 15 FD-SOI region and at least one RF-SOI region,
- producing:
- at least one digital component (9) in the active layer (6), in the FD-SOI region, and
- at least one radiofrequency component (10) plumb with the first electrically
- 20 insulating layer (3).

16. Process for fabricating a semiconductor-on-insulator multilayer structure (1), comprising the following steps:

- forming a back stack by depositing a first semiconductor layer (4) on a carrier
- 25 substrate (2) covered with a first electrically insulating layer (3),
- providing a donor substrate,
- forming a weakened zone in said donor substrate, so as to delineate a second semiconductor layer (6),
- transferring said second semiconductor layer (6) to the back stack, a second
- 30 electrically insulating layer (5) being at the interface between the second donor substrate and the back stack, so as to form a front stack on the back stack,
- forming at least one trench isolation (8) that extends through the front stack and through the back stack at least down to the first electrically insulating layer
- 35 (3), in order to electrically isolate two adjacent regions, including at least one FD-SOI region and at least one RF-SOI region,
- producing:

at least one digital component (9) in the active layer (6), in the FD-SOI region,
and
at least one radiofrequency component (10) on the first semiconductor layer (4).

- 5 17. Process according to Claim 15 or Claim 16, comprising, before the
radiofrequency component (10) is produced, a step of selectively removing the
active layer (6) and the second electrically insulating layer (5) of the RF-SOI
region, and wherein the radiofrequency component (10) is then formed in the
10 first semiconductor layer (4).
18. Process according to one of Claims 15 to 17, furthermore comprising, before
the transferring step, forming a charge-trapping layer (7) on the receiver
substrate, said charge-trapping layer (7) being arranged between the carrier
substrate (2) and the first electrically insulating layer (3).