WHAT IS CLAIMED IS:

1. A switching element comprising:

a lower barrier electrode on a substrate;

a switching pattern on the lower barrier electrode; and

an upper barrier electrode on the switching pattern,

wherein the lower barrier electrode comprises:

a first lower barrier electrode layer; and

a second lower barrier electrode layer interposed between the first lower barrier electrode layer and the switching pattern, the second lower barrier electrode layer having a density different from that of the first lower barrier electrode layer, and

wherein the first lower barrier electrode layer is a carbon film, and the second lower barrier electrode layer is a carbon film.

2. The switching element of claim 1, wherein the density of the second lower barrier electrode layer is higher than the density of the first lower barrier electrode layer.

~~3. The switching element of claim 1 or claim 2, wherein the first lower barrier electrode layer is a carbon film, and the second lower barrier electrode layer is a carbon film.~~

43. The switching element of claim ~~2~~ 1 or claim ~~3~~2, wherein the density of the first lower barrier electrode layer is about 1.7 g/cm^3, and the density of the second lower barrier electrode layer is about 2.3 g/cm^3.

~~5~~4. The switching element of any one of claims 1 to ~~4~~3, wherein resistivity of the second lower barrier electrode layer is less than that of the first lower barrier electrode layer.

~~6~~5. The switching element of any one of claims 1 to ~~5~~4, wherein surface roughness of the second lower barrier electrode layer is less than that of the first lower barrier electrode layer.

~~7~~6. The switching element of any one of claims 1 to ~~6~~5, wherein the upper barrier electrode comprises:

a first upper barrier electrode layer; and

a second upper barrier electrode layer which is disposed on the first upper barrier electrode layer and has a density different from that of the first upper barrier electrode layer.

~~8~~7. The switching element of claim ~~7~~6, further comprising:

an upper electrode on the upper barrier electrode,

wherein the density of the second upper barrier electrode layer is lower than that of the first upper barrier electrode layer.

~~9~~8. The switching element of claim ~~7~~6, wherein the density of the second upper barrier electrode layer is higher than the density of the first upper barrier electrode layer.

~~10~~9. The switching element of any one of claims 1 to ~~9~~8, wherein the switching pattern includes a chalcogenide element.

~~11~~10. A variable resistance memory device comprising:

a first conductive line extending longitudinally in a first direction;

a second conductive line extending longitudinally in a second direction intersecting the first direction when the first conductive line and the second conductive line are viewed in a plan view;

a variable resistance structure interposed between the first and second conductive lines; and

a switching element interposed between the variable resistance structure and the second conductive line,

wherein the switching element comprises:

a lower barrier electrode;

a switching pattern on the lower barrier electrode; and

an upper barrier electrode on the switching pattern, and

wherein the lower barrier electrode comprises:

a first lower barrier electrode layer; and

a second lower barrier electrode layer interposed between the first lower barrier electrode layer and the switching pattern, the second lower barrier electrode layer having a density different from that of the first lower barrier electrode layer, and

wherein the first lower barrier electrode layer is a carbon film, and the second lower barrier electrode layer is a carbon film.

~~12~~11. The variable resistance memory device of claim ~~11~~10, further comprising:

an intermediate electrode interposed between the first lower barrier electrode layer and the variable resistance structure.

~~13~~12. The variable resistance memory device of claim ~~12~~11, wherein a width of the first lower barrier electrode layer is greater than a width of the intermediate electrode.

~~14~~13. The variable resistance memory device of any one of claims ~~11~~ 10 to ~~13~~12, wherein the upper barrier electrode comprises:

a first upper barrier electrode layer; and

a second upper barrier electrode layer which is interposed between the first upper barrier electrode layer and the second conductive line and has a density different from that of the first upper barrier electrode layer.

~~15~~14. The variable resistance memory device of any one of claims ~~11~~ 10 to ~~14~~13, wherein the switching element further comprises an upper electrode interposed between the upper barrier electrode and the second conductive line.

~~16~~15. A method of manufacturing a switching element, the method comprising:

forming a lower barrier layer on a substrate;

forming a switching layer on the lower barrier layer;

forming an upper barrier layer on the switching layer; and

removing portions of the lower barrier layer, the switching layer and the upper barrier layer to form a switching element,

wherein the forming of the lower barrier layer comprises:

forming a first lower barrier layer; and

forming a second lower barrier layer on the first lower barrier layer, wherein the second lower barrier layer has a different density from a density of the first lower barrier layer,

wherein the method further comprises forming a first lower barrier electrode layer and a second lower barrier electrode layer from the first lower barrier layer and the second lower barrier layer, respectively, and

wherein the first lower barrier electrode layer is a carbon film, and the second lower barrier electrode layer is a carbon film.

~~17~~16. The method of claim ~~16~~15, wherein the lower barrier layer is formed by a sputtering method,

wherein the first lower barrier layer is formed using source power, and

wherein the second lower barrier layer is formed using the source power and bias power different from the source power.

~~18~~17. The method of claim ~~16~~ 15 or claim ~~17~~16, wherein the first lower barrier layer is formed at a first temperature, and

wherein the second lower barrier layer is formed at a second temperature lower than the first temperature.

~~19~~18. The method of any one of claims ~~16~~ 15 to ~~18~~17, wherein the forming of the upper barrier layer comprises:

forming a first upper barrier layer; and

forming a second upper barrier layer on the first upper barrier layer, wherein the second upper barrier layer has a different density from a density of the first upper barrier layer.

~~20~~19. The method of claim ~~19~~18, further comprising:

forming an upper electrode layer on the second upper barrier layer.