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DESCRIPTION

SUBSTRATE FOR A TRANSFER MASK, TRANSFER MASK, AND METHOD OF MANUFACTURING THE TRANSFER MASK

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Technical Field

The present invention relates to a substrate for
a transfer mask which is adapted for use in an exposure
process using a charged beam such as electron beam
or ion beam. The present invention relates also to
a transfer mask and to the manufacturing method of
the transfer mask.

Background Art

Recently, electron beam lithography, ion beam
lithography, etc., where an electron beam or ion beam
is employed as an exposure light source, have come to
be seen as useful in a technique for manufacturing
elements having an ultrafine pattern of the next
generation. In the exposure process utilizing these
manufacturing techniques, it is required to employ
a transfer mask. In the manufacture of this transfer
mask, a substrate formed of an SOI (Silicon On
Insulator) substrate is employed because of the
easiness in fine working.

This SOI substrate for forming a transfer pattern
is constituted by a lower monocrystalline silicon wafer
as a substrate, a silicon oxide film formed on the
lower monocrystalline silicon wafer and functioning

as an etching stopper, and an upper monocrystalline silicon wafer formed on the silicon oxide film, the transfer pattern being formed on the upper monocrystalline silicon wafer.

5 The thickness of silicon oxide film constituting part of the SOI substrate to be employed as a substrate for a transfer mask is generally within the range of about 1 μm to 2 μm . However, there is a problem in the employment of the SOI substrate comprising a
10 silicon oxide film having such a magnitude of thickness that cracks tend to be formed in the upper monocrystalline silicon wafer due to stress imposed thereon by the silicon oxide film, thereby destroying the transfer pattern and hence deteriorating the
15 manufacturing efficiency of the transfer mask.

 Therefore, an object of the present invention is to provide a substrate for a transfer mask, which comprises a couple of silicon layers laminated with a silicon oxide film being interposed therebetween,
20 and which makes it possible to stably manufacture a defect-free transfer mask, i.e. a transfer mask wherein a transfer pattern formed on the upper silicon layer is prevented from being destroyed due to stress from the silicon oxide film on the occasion of
25 manufacturing a transfer mask by making use of the substrate.

 Another object of the present invention is to

provide a transfer mask which comprises a transfer pattern formed on the upper silicon layer of the aforementioned substrate for a transfer mask, and which makes it possible to prevent the transfer pattern
5 formed on the upper silicon layer from being destroyed due to stress from the silicon oxide film on the occasion of manufacturing the transfer mask, thereby providing a defect-free transfer mask.

A further object of the present invention is to
10 provide a method of manufacturing the aforementioned transfer mask, which makes it possible to prevent the transfer pattern formed on the upper silicon layer from being destroyed due to stress from the silicon oxide film, thereby enabling a defect-free transfer mask to
15 be manufactured.

Disclosure of Invention

According to the present invention, there is provided a substrate for a transfer mask, which comprises a first silicon layer formed of
20 monocrystalline silicon; a silicon oxide film formed on the first silicon layer and having a thickness ranging from 0.2 to 0.8 μm ; and a second silicon layer formed on the silicon oxide film.

According to the present invention, there is
25 further provided a transfer mask comprising a first silicon layer formed of monocrystalline silicon; a silicon oxide film formed on the first silicon layer

and having a thickness ranging from 0.2 to 0.8 μm ;
and a second silicon layer formed on the silicon oxide
film and bearing therein a transfer pattern; wherein
openings are formed in the first silicon layer, and
5 the portions of the silicon oxide film which correspond
to the openings are removed.

According to the present invention, there is
further provided a method of manufacturing a transfer
mask, the method comprising: preparing a substrate
10 comprising a first silicon layer formed of
monocrystalline silicon, a silicon oxide film formed on
the first silicon layer and having a thickness ranging
from 0.2 to 0.8 μm , and a second silicon layer formed
on the silicon oxide film; forming a transfer pattern
15 on the second silicon layer; forming openings in the
first silicon layer before or after forming the
transfer pattern; and selectively removing portions of
the silicon oxide film which correspond to the
openings.

20 According to the present invention, there is
further provided a method of manufacturing a transfer
mask, the method comprising: preparing a substrate
comprising a first silicon layer formed of
monocrystalline silicon, a silicon oxide film formed on
25 the first silicon layer and having a thickness ranging
from 0.2 to 0.8 μm , and a second silicon layer formed
on the silicon oxide film; forming openings in the

first silicon layer; selectively removing portions of the silicon oxide film which correspond to the openings; and forming a transfer pattern in the second silicon layer.

5 According to the present invention, there is further provided a method of irradiating a charged particle beam, the method comprising: irradiating a charged particle beam onto the aforementioned transfer mask in such a manner as to shape the charged particle
10 beam in conformity with the configuration of a transfer pattern; and image-forming a pattern of the shaped charged particle beam on a substrate through a lens.

 It is preferable in the present invention that the second silicon layer has a film thickness of 0.1 to
15 50 μm . Further, the second silicon layer should preferably be formed of monocrystalline silicon.

 The substrate for a transfer mask according to the present invention should preferably be formed of an SOI substrate comprising two monocrystalline silicon wafers
20 superposed on one another via a silicon oxide film being interposed therebetween.

Brief Description of Drawings

 FIG. 1 is a cross-sectional view showing a substrate (SOI substrate) for a transfer mask
25 according to one example of the present invention;

 FIG. 2 is a cross-sectional view showing one example of a transfer mask which was manufactured

by making use of a substrate (SOI substrate) for a transfer mask according to one example of the present invention;

FIGS. 3A to 3I are cross-sectional views illustrating stepwise one example of a manufacturing process of a transfer mask by making use of a substrate for a transfer mask according to the present invention;

FIGS. 4A to 4I are cross-sectional views illustrating stepwise another example of a manufacturing process of a transfer mask by making use of a substrate for a transfer mask according to the present invention; and

FIGS. 5A to 5F are cross-sectional views illustrating stepwise another example of a manufacturing process of a transfer mask by making use of a substrate for a transfer mask according to the present invention.

Best Mode for Carrying Out of the Invention

Next, a substrate for a transfer mask as well as a transfer mask according to one embodiment of the present invention will be explained in detail with reference to the drawings.

FIG. 1 is a cross-sectional view showing a substrate (SOI substrate) for a transfer mask according to one example of the present invention. Referring to FIG. 1, the substrate (SOI substrate) for a transfer mask 4 is constituted by a laminated structure

comprising a lower monocrystalline silicon wafer 3
in which openings are to be subsequently formed,
an upper monocrystalline silicon wafer 1 in which
a transfer pattern is to be subsequently formed, and
5 a silicon oxide film 2 interposed between the lower
monocrystalline silicon wafer 3 and the upper
monocrystalline silicon wafer 1. This laminated
structure is featured in that the thickness of the
silicon oxide film 2 is confined to a range of 0.2 μm
10 to 0.8 μm .

If the thickness of the silicon oxide film 2 is
less than 0.2 μm , the etching resistance of the
silicon oxide film 2 may become insufficient, thereby
easily inviting a phenomenon wherein the etching is
15 permitted to proceed passing through the silicon oxide
film 2, because over-etching is usually performed
taking the in-plane distribution of etching depth or
the distribution of etching depth depending on the size
of pattern into consideration on the occasion of
20 performing dry etching of the upper monocrystalline
silicon wafer 1.

When the etching is permitted to proceed passing
through the silicon oxide film 2, a wet etching liquid
is permitted to penetrate through this etched through-
25 hole formed in the silicon oxide film 2 on the occasion
of wet etching to form an opening portion in the lower
monocrystalline silicon wafer 3, thereby raising a

problem that the transfer pattern formed on the upper monocrystalline silicon wafer 1 may be destroyed.

Further, when the etching is permitted to proceed passing through the silicon oxide film 2, an inert gas as a cooling medium is allowed to leak through this etched through-hole formed in the silicon oxide film 2 on the occasion of dry etching to form an opening portion in the lower monocrystalline silicon wafer 3 while directly cooling the substrate by making use of a cooling medium, thereby raising a problem that the discharging for etching is caused to be suspended in a midway of the etching process. This leakage of inert gas is also caused in the case where the etching of the lower monocrystalline silicon wafer 3 is performed prior to the formation of the transfer pattern.

On the other hand, if the thickness of the silicon oxide film 2 is larger than $0.8\ \mu\text{m}$, cracks may be generated in the transfer pattern, thereby destroying the transfer pattern due to the stress from the silicon oxide film 2 on the occasion where the silicon oxide film 2 is permitted to be exposed due to wet etching or dry etching of the lower monocrystalline silicon wafer 3 to form an opening therein.

Namely, when the thickness of the silicon oxide film 2 is confined within the range of $0.2\ \mu\text{m}$ to $0.8\ \mu\text{m}$, the phenomenon of generating cracks in the transfer pattern to destroy the transfer pattern can be

prevented.

Incidentally the way, a monocrystalline or polycrystalline silicon layer deposited on the surface of the silicon oxide film 2 may be substituted for the upper monocrystalline silicon wafer 1.

Further, in the present invention, the thickness of the upper monocrystalline silicon wafer or the upper silicon layer should preferably be within the range of 0.1 μm to 50 μm , more preferably, within the range of 1 μm to 50 μm .

If the transfer mask of the present invention is to be applied to a scattering type transfer mask, the thickness of the upper monocrystalline silicon wafer or the upper silicon layer should preferably be within the range of 0.1 to 3 μm . Whereas, if the transfer mask of the present invention is to be applied to a shielding type transfer mask, the thickness of the upper monocrystalline silicon wafer or the upper silicon layer should preferably be within the range of 5 to 50 μm .

In either case, if the thickness of the upper monocrystalline silicon wafer or the upper silicon layer is too thin, the upper monocrystalline silicon wafer or the upper silicon layer may be fused away as the magnitude of electric current is increased in order to enhance throughput. On the other hand, if the thickness of the upper monocrystalline silicon wafer or

the upper silicon layer is too thick, it may become difficult to form a transfer pattern.

Further, the thickness of the lower monocrystalline silicon wafer according to the present invention should preferably be within the range of about 400 μm to 1 mm. Because, if the thickness of the lower monocrystalline silicon wafer is less than 400 μm , it may be no longer possible to ensure its function as a supporting body for the transfer mask. On the other hand, if the thickness of the lower monocrystalline silicon wafer exceeds 1 mm, it may become difficult to satisfactorily work the substrate, i.e., the lower monocrystalline silicon wafer.

FIG. 2 is a cross-sectional view showing one example of a transfer mask which was manufactured by making use of the aforementioned substrate (SOI substrate) 4 for a transfer mask, representing another embodiment of the present invention. As shown in FIG. 2, the transfer mask 40 according to another embodiment of the present invention is constituted by a lower monocrystalline silicon wafer 13 having an opening 9, a silicon oxide film 12 having an opening, and an upper monocrystalline silicon wafer 11 bearing therein a transfer pattern 6.

The construction shown in FIG. 2 represents one embodiment where a conductive film 20a is formed on the lower monocrystalline silicon wafer 13 having an

opening 9, and at the same time, a conductive film 20b is formed on the upper monocrystalline silicon wafer 11 bearing therein a transfer pattern. However, these conductive films 20a, 20b are not necessarily essential, and may be omitted.

Next, the manufacturing process of the transfer mask according to another embodiment of the present invention will be explained as follows.

First of all, a fine pattern is formed on the surface of the upper monocrystalline silicon wafer 11. This process of forming this fine pattern is performed by a sequence of steps comprising, stepwise, a step of forming a resist pattern on the surface of the upper monocrystalline silicon wafer 11, a step of dry-etching the upper monocrystalline silicon wafer 11 by making use of this resist pattern as a mask, and a step of removing the resist pattern.

The exposure process of forming the resist pattern can be suitably performed by directly scanning an electron beam using a resist for an electron beam, or by means of stepper exposure using a photoresist.

In the case where the etching resistance of the resist is found insufficient on the occasion of dry-etching the upper monocrystalline silicon wafer, it is possible to employ, as an etching mask, an inorganic film such as a silicon oxide film, a silicon nitride film, a silicon carbide film, etc.; a metallic film

made of chromium, tungsten, tantalum, titanium, nickel, aluminum, etc., or an alloy of these metals; or a metallic compound film formed through a reaction between any of these metals or alloys and oxygen, nitrogen, carbon, etc. These etching masks can be formed by means of various kinds of thin film-forming method. For example, it is possible to employ a sputtering method, a CVD method, a vapor deposition method, etc.

As for the dry etching method, there is not any particular limitation with respect to the conditions for the etching. As for the gas to be employed in the dry etching, it is possible to employ a mixed gas mainly comprising a fluorine-containing gas such as SF_6 gas and CF_4 gas.; a mixed gas mainly comprising a chlorine-containing gas such as Cl_2 gas and SiCl_4 gas; or a mixed gas mainly comprising a bromine-containing gas such as HBr gas. As for the dry etching apparatus, it is possible to employ that where RIE, magnetron RIE, ECR, ICP, microwaves, helicon waves, NLD, etc., is employed as a discharge system.

Next, openings are formed in the lower monocrystalline silicon wafer, wherein dry etching, wet etching, ultrasonic working, sand blasting, etc., can be suitably employed.

Incidentally, the step of forming a transfer pattern in the upper monocrystalline silicon wafer may

be performed prior to or subsequent to the step of forming openings in the lower monocrystalline silicon wafer.

5 Next, the silicon oxide film formed on the openings is removed. Specifically, the silicon oxide film can be removed by making use of hydrofluoric acid, which is followed by the formation of conductive film on opposite main surfaces if required, thereby accomplishing a transfer mask.

10 As for the conductive film, it is possible to employ a metal such as gold, platinum, palladium, tantalum, tungsten, molybdenum and osmium; or an alloy containing any of these metals. These metals can be employed singly or together with an underlying layer.

15 As for the method of forming the conductive film, it is possible to employ a sputtering method, a CVD method, a vapor deposition method, a plating method, an electrode position method, an ion plating method, etc.

20 As described above, the formation of openings in the lower monocrystalline silicon wafer can be performed prior to the formation of a transfer pattern in the upper monocrystalline silicon wafer. In this case, part of the silicon oxide film which is exposed through the openings formed in the lower

25 monocrystalline silicon wafer may be selectively removed prior to the formation of a transfer pattern in the upper monocrystalline silicon wafer. On the

occasion of forming a transfer pattern in this process,
there is little possibility that the transfer pattern
is cracked or destroyed due to stress generated in the
silicon oxide film, since the silicon oxide film does
5 not exist at this portion.

However, in order to prevent leakage of the inert
gas to be employed for cooling the substrate on the
occasion of the dry etching step for forming a transfer
pattern on the upper monocrystalline silicon wafer,
10 it may be necessary to take some sort of measures such
as the placement of the lower monocrystalline silicon
wafer on a holder which is excellent in thermal
conductivity.

Examples

15 Next, specific example of the present invention
will be explained with reference to drawings.

(Example 1)

FIGS. 3A to 3I are cross-sectional views
illustrating stepwise one example of a manufacturing
20 process of a transfer mask by making use of a substrate
for a transfer mask according to one embodiment of the
present invention. First of all, as shown in FIG. 3A,
an SOI substrate exhibiting a plane orientation of
(100) was employed as a substrate 4 for a transfer
25 mask (which is referred to also as a transfer mask
substrate). This transfer mask substrate 4 was
constituted by a laminated structure comprising

an upper monocrystalline silicon wafer 1, a lower monocrystalline silicon wafer 3, and a silicon oxide film 2 interposed between these upper monocrystalline silicon wafer 1 and lower monocrystalline silicon wafer 3. The thickness of the upper monocrystalline silicon wafer 1 was 20 μm , the thickness of the silicon oxide film was 0.5 μm , and the thickness of the lower monocrystalline silicon wafer 3 was 500 μm .

Then, a resist for an electron beam (ZEP520, Nihon Zeon Co., Ltd.) was coated to a thickness of 0.5 μm on the surface of the upper monocrystalline silicon wafer 1 of the transfer mask substrate 4, and a pattern was described on the resist by making use of an electron beam drawing machine exhibiting an accelerating voltage of 50 kV. Subsequently, by making use of a developing solution for exclusive use (ZED-N50, Nihon Zeon Co., Ltd.), the development of the resist was performed, thereby forming a resist pattern 5 as shown in FIG. 3B.

Next, by making use of the resist pattern 5 as a mask together with the employment of a mixed gas mainly consisting of fluorine-containing gas, i.e., SF_6 , as an etchant, the dry etching of the upper monocrystalline silicon wafer 1 was performed to a depth extending to the silicon oxide film 2 by means of an ICP (inductively coupled plasma) dry etching apparatus, thereby forming a transfer pattern 6 as shown in FIG. 3C.

Then, the resist pattern 5 was removed, and a silicon nitride film 7 having a thickness of $0.3\ \mu\text{m}$ was formed on the opposite main surfaces and peripheral wall of the transfer mask substrate as shown in FIG. 3D by means of an LPCVD (Low Pressure Chemical Vapor Deposition) apparatus.

Subsequently, the silicon nitride film formed on the surface of the lower monocrystalline silicon wafer was subjected to dry etching by making use of a mixed gas mainly containing CHF_3 gas and by means of an RIE (Reactive Ion Etching) apparatus, thereby forming a protective pattern 8 for wet etching as shown in FIG. 3E.

Then, the substrate bearing thereon the protective pattern 8 was set on a jig so as to protect the transfer pattern formed on the upper monocrystalline silicon wafer, and was immersed in an etching solution consisting of an aqueous solution of KOH which was heated to a temperature of about 90°C . Thus, the etching was performed using the protective pattern 8 as a mask to such an extent that the anisotropic etching of the lower monocrystalline silicon wafer 3 along the plane orientation thereof proceeded down to the silicon oxide film 2 functioning as an etching stopper, thereby forming an opening 9 as shown in FIG. 3F. The reference number 3' in FIG. 3F represents the lower monocrystalline silicon wafer in which the opening 9

was formed.

Next, as shown in FIG. 3G, the protective pattern 8 was etched away by making use of hot phosphoric acid heated to about 170°C. Thereafter, as shown in FIG. 3H, the exposed portion of the silicon oxide film 2 was etched away by making use of hydrofluoric acid. The reference number 2' in FIG. 3G represents the silicon oxide film in which openings were formed.

Finally, a platinum-palladium alloy having a thickness of about 0.1 μm was deposited on the opposite main surfaces of the resultant body by means of a magnetron sputtering apparatus to thereby form conductive films 10a and 10b, thus accomplishing a transfer mask as shown in FIG. 3I.

The transfer mask manufactured in this manner was free from cracks of the upper monocrystalline silicon wafer that might be caused by stress from the silicon oxide film, thereby obtaining a transfer mask which was excellent in quality.

(Example 2)

FIGS. 4A to 4I are cross-sectional views illustrating stepwise another example of a manufacturing process of a transfer mask by making use of a transfer mask substrate according to another embodiment of the present invention. First of all, as shown in FIG. 4A, an SOI substrate exhibiting a plane orientation of (100) was employed as a substrate 4 for

a transfer mask (which is referred to also as a transfer mask substrate). This transfer mask substrate 4 was constituted by a laminate structure having the same constituent components as described in Example 1.

5 The thickness of the upper monocrystalline silicon wafer 1 was 20 μm , the thickness of the silicon oxide film was 0.5 μm , and the thickness of the lower monocrystalline silicon wafer 3 was 500 μm .

As shown in FIG. 4B, a silicon nitride film 7 was
10 formed all over the transfer mask substrate 4 including the opposite main surfaces and peripheral wall thereof by means of the CVD method, and then, the silicon nitride film formed on the surface of the lower monocrystalline silicon wafer 3 was subjected to
15 a patterning treatment, thereby forming a protective pattern 8 for wet etching as shown in FIG. 4C.

Then, the lower monocrystalline silicon wafer 3 having thereon the protective pattern 8 was set on a jig and immersed in an etching solution consisting
20 of an aqueous solution of KOH which was heated to a temperature of about 90°C. Thus, the etching was performed using the protective pattern 8 as a mask to such an extent that the anisotropic etching of the lower monocrystalline silicon wafer 3 along the plane
25 orientation thereof proceeded down to the silicon oxide film 2 functioning as an etching stopper, thereby forming an opening 9 as shown in FIG. 4D.

The reference number 3' in FIG. 4D represents the lower monocrystalline silicon wafer in which the opening 9 was formed.

Next, as shown in FIG. 4E, the protective pattern 8 was etched away by making use of hot phosphoric acid heated to about 170°C. Thereafter, a resist for an electron beam was coated to a thickness of 0.5 μm on the surface of the upper monocrystalline silicon wafer 1, and a pattern was described on the resist by making use of an electron beam drawing machine exhibiting an accelerating voltage of 50 kV. Subsequently, by making use of a developing solution for exclusive use, the development of the resist was performed, thereby forming a resist pattern 5 as shown in FIG. 4F. The resist for an electron beam and the developing solution both employed herein were the same as those employed in Example 1.

Next, by making use of the resist pattern 5 as a mask together with the employment of a mixed gas mainly consisting of fluorine-containing gas, i.e., SF_6 , as an etchant, the dry etching of the upper monocrystalline silicon wafer 1 was performed to a depth extending to the silicon oxide film 2 by means of an ICP (inductively coupled plasma) dry etching apparatus, thereby forming a transfer pattern 6 as shown in FIG. 4G.

Then, the resist pattern 5 was removed as shown in

FIG. 4H, and at the same time, the exposed portion of the silicon oxide film 2 was etched away by making use of buffer hydrofluoric acid. The reference number 2' in FIG. 4H represents the silicon oxide film in which openings were formed.

Finally, as shown in FIG. 4I, tantalum having a thickness of about $0.1\text{ }\mu\text{m}$ was deposited on the opposite main surfaces of the resultant body by means of an electron beam vapor deposition apparatus to thereby form conductive films 10a and 10b, thus accomplishing a transfer mask.

The transfer mask manufactured in this manner was free from cracks of the upper monocrystalline silicon wafer that might be caused by stress from the silicon oxide film, thereby obtaining a transfer mask which was excellent in quality.

(Example 3)

FIGS. 5A to 5F are cross-sectional views illustrating stepwise a further example of a manufacturing process of a transfer mask by making use of a transfer mask substrate according to a further embodiment of the present invention. First of all, as shown in FIG. 5A, an SOI substrate exhibiting a plane orientation of (100) was employed as a substrate for a transfer mask 4. This transfer mask substrate 4 was constituted by a laminate structure having the same constituent components as described in Example 1.

The thickness of the upper monocrystalline silicon wafer 1 was 2 μm , the thickness of the silicon oxide film was 0.7 μm , and the thickness of the lower monocrystalline silicon wafer 3 was 500 μm .

5 Then, as shown in FIG. 5B, a resist pattern 5 was formed on the surface of a lower monocrystalline silicon wafer 3 by means of ordinary photolithography. Subsequently, by making use of this resist pattern 5 as a mask together with the employment of a mixed gas
10 mainly consisting of SF_6 as an etchant, etching of the lower monocrystalline silicon wafer 3 was performed by means of an ICP (inductively coupled plasma) dry etching apparatus to thereby form openings 9 as shown in FIG. 5C.

15 When all of the portion of the lower monocrystalline silicon wafer 3 for forming the openings 9 was completely removed by way of etching, the silicon oxide film 2 having a thickness of 0.7 μm was sufficiently capable of acting as an etching
20 stopper. Further, the cross-section of the lower monocrystalline silicon wafer 3' which was provided with openings as a result of the aforementioned etching was found as having substantially perpendicular sidewalls.

25 Then, as shown in FIG. 5D, the resist pattern 5 was removed by an ashing treatment using oxygen plasma, and the portion of the silicon oxide film 2 which was

exposed through the openings 9 was completely etched away by making use of buffer hydrofluoric acid.

The reference number 2' in FIG. 5D represents the silicon oxide film in which openings were formed.

5 Thereafter, a resist for an electron beam was coated to a thickness of 1.0 μm on the surface of the upper monocrystalline silicon wafer 1, and a pattern was described on the resist by making use of an electron beam drawing machine exhibiting
10 an accelerating voltage of 100 kV. Subsequently, by making use of a developing solution for exclusive use, the development of the resist was performed, thereby forming a resist pattern 5 as shown in FIG. 5E.

 Next, by making use of the resist pattern 5 as a
15 mask together with the employment of a mixed gas mainly consisting of HBr as an etchant, the dry etching of the upper monocrystalline silicon wafer 1 was performed by means of an ICP (inductively coupled plasma) dry etching apparatus, thereby forming a transfer pattern
20 6 enabling the charged particle beam to pass therethrough. Subsequently, the resist pattern 5 was removed by making use of an organic solvent. As a result, as shown in FIG. 5F, a transfer mask having the transfer pattern 6 was accomplished.

25 The transfer mask manufactured in this manner was mounted on a charged particle beam exposure apparatus, and this specimen was subjected to an exposure process

using an electron beam as a charged particle beam.

Namely, the electron beam emitted from an electron gun was irradiated onto the transfer mask mounted on the stage arranged at a predetermined position in such a manner as to shape the charged particle beam in conformity with the configuration of the transfer pattern, the resultant shaped pattern of the charged particle beam being subsequently reduced by means of an electron lens and image-formed on the surface of the specimen having the resist film. As a result, it was found possible to perform an exposure of high precision which was exactly the same as designed.

(Comparative Example 1)

A transfer mask was manufactured under the same conditions as those of Example 1 except that the thickness of the silicon oxide film was set to 0.1 μm . When the upper monocrystalline silicon wafer of the transfer mask thus manufactured was investigated through observation thereof, destruction of the transfer pattern due to the wet etching solution was recognized.

(Comparative Example 2)

A transfer mask was manufactured under the same conditions as those of Example 1 except that the thickness of the silicon oxide film was set to 1 μm . When the upper monocrystalline silicon wafer of the transfer mask thus manufactured was investigated

through observation thereof, cracking of the upper monocrystalline silicon wafer due to stress by the silicon oxide film was recognized, and hence the yield of the transfer mask which was free from cracking was found to be 0%.

As explained above, according to the present invention, since the transfer mask substrate which is constituted by a laminated structure comprising two silicon layers, and a silicon oxide film interposed between this pair of silicon layers is constructed such that the thickness of silicon oxide film was confined within the range of 0.2 μm to 0.8 μm , it is possible to attain the effect that the transfer pattern formed on the upper monocrystalline silicon wafer is caused to fracture due to stress by the silicon oxide film.

Furthermore, the transfer mask manufactured by making use of the aforementioned transfer mask substrate is of such a high quality that the upper monocrystalline silicon wafer can hardly be destroyed.

Moreover, according to the manufacturing method of the transfer mask by making use of the aforementioned transfer mask substrate, it is possible to stably manufacture a defect-free transfer mask.

Additionally, according to the method of irradiating a charged particle beam where the aforementioned transfer mask is employed, it is now possible to perform, at high precision, the patterning

exposure of the resist formed on a substrate.

As a result, patterning such as the patterning of a semiconductor can be performed with high yield.

C L A I M S

1. A substrate for a transfer mask, which comprises a first silicon layer formed of monocrystalline silicon; a silicon oxide film formed on the first silicon layer and having a thickness ranging from 0.2 to 0.8 μm ; and a second silicon layer formed on the silicon oxide film.

2. The substrate for a transfer mask according to claim 1, wherein said second silicon layer has a thickness ranging from 0.1 to 50 μm .

3. The substrate for a transfer mask according to claim 1, wherein said second silicon layer is formed of monocrystalline silicon.

4. A transfer mask comprising a first silicon layer formed of monocrystalline silicon; a silicon oxide film formed on the first silicon layer and having a thickness ranging from 0.2 to 0.8 μm ; and a second silicon layer formed on the silicon oxide film and bearing therein a transfer pattern;

wherein openings are formed in said first silicon layer, and the portions of said silicon oxide film which correspond to said openings are removed.

5. The transfer mask according to claim 4, wherein said second silicon layer has a thickness ranging from 0.1 to 50 μm .

6. The transfer mask according to claim 4, wherein said second silicon layer is formed of

monocrystalline silicon.

7. A method of manufacturing a transfer mask,
the method comprising:

5 preparing a substrate comprising a first silicon
layer formed of monocrystalline silicon, a silicon
oxide film formed on the first silicon layer and having
a thickness ranging from 0.2 to 0.8 μm , and a second
silicon layer formed on the silicon oxide film;

10 forming a transfer pattern on said second silicon
layer;

forming openings in said first silicon layer
before or after forming said transfer pattern; and

selectively removing portions of said silicon
oxide film which correspond to said openings.

15 8. The method according to claim 7, wherein said
second silicon layer has a thickness ranging from 0.1
to 50 μm .

9. The method according to claim 7, wherein said
second silicon layer is formed of monocrystalline
20 silicon.

10. A method of manufacturing a transfer mask,
the method comprising:

25 preparing a substrate comprising a first silicon
layer formed of monocrystalline silicon, a silicon
oxide film formed on the first silicon layer and having
a thickness ranging from 0.2 to 0.8 μm , and a second
silicon layer formed on the silicon oxide film;

forming openings in said first silicon layer;
selectively removing portions of said silicon
oxide film which correspond to said openings; and
forming a transfer pattern in said second silicon
5 layer.

11. The method according to claim 10, wherein said
second silicon layer has a thickness ranging from 0.1
to 50 μm .

12. The method according to claim 10, wherein said
10 second silicon layer is formed of monocrystalline
silicon.

13. A method of irradiating a charged particle
beam, the method comprising:

15 irradiating a charged particle beam onto the
transfer mask as claimed in Claim 4 in such a manner
as to shape said charged particle beam in conformity
with the configuration of a transfer pattern; and
image-forming a pattern of said shaped charged
particle beam on a substrate through a lens.