

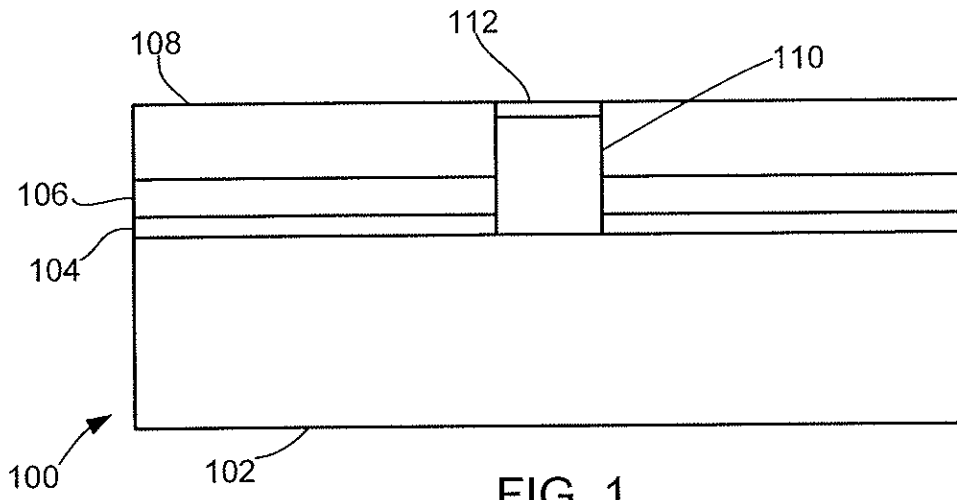


FIG. 1

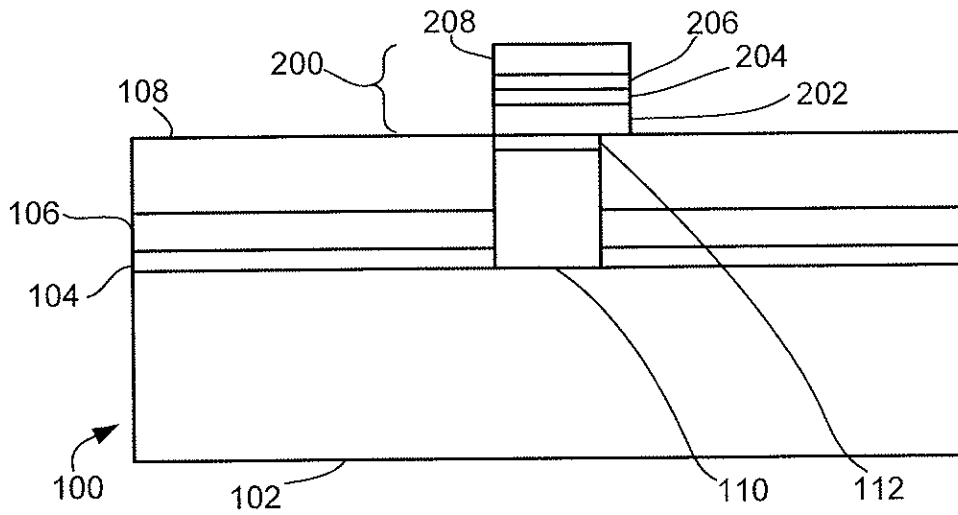


FIG. 2

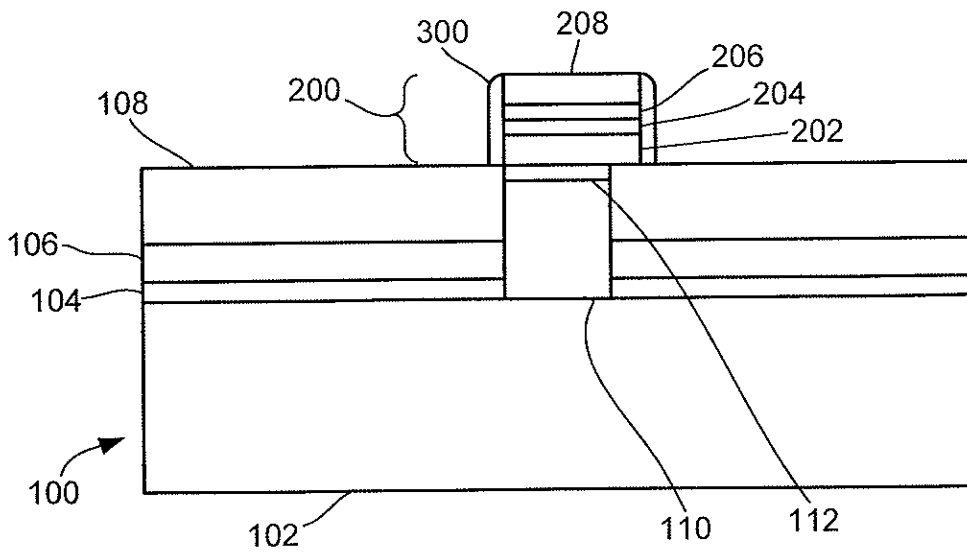


FIG. 3

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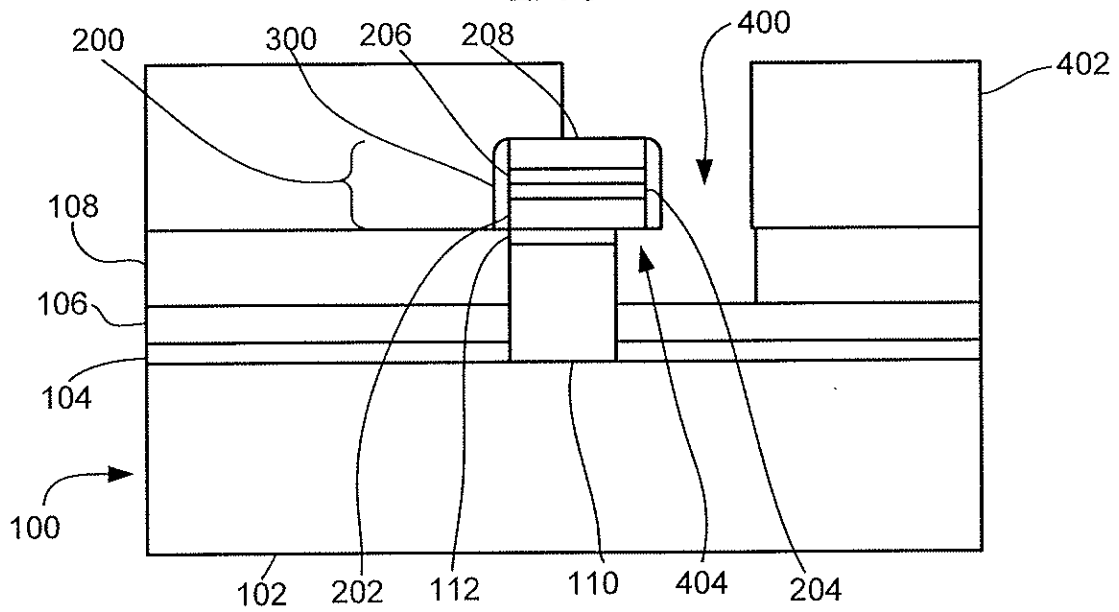


FIG. 4

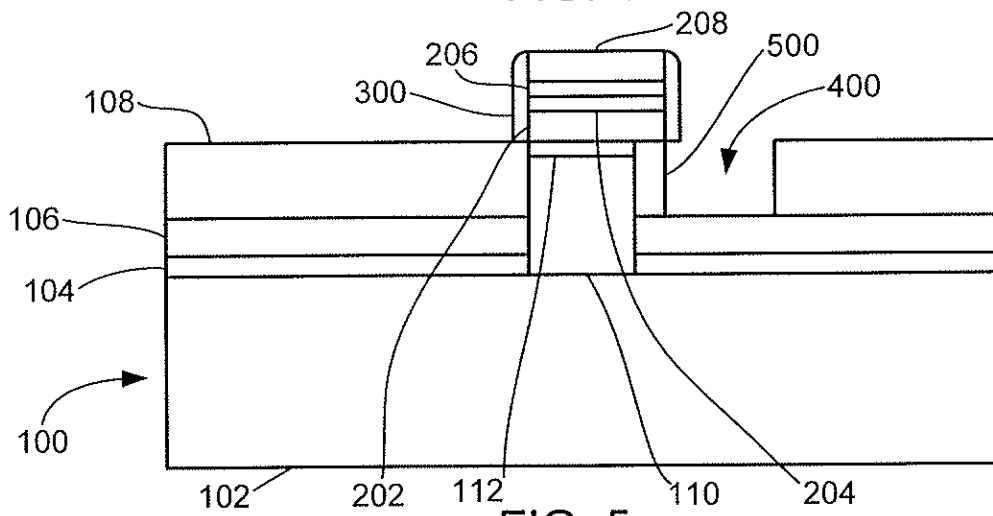


FIG. 5

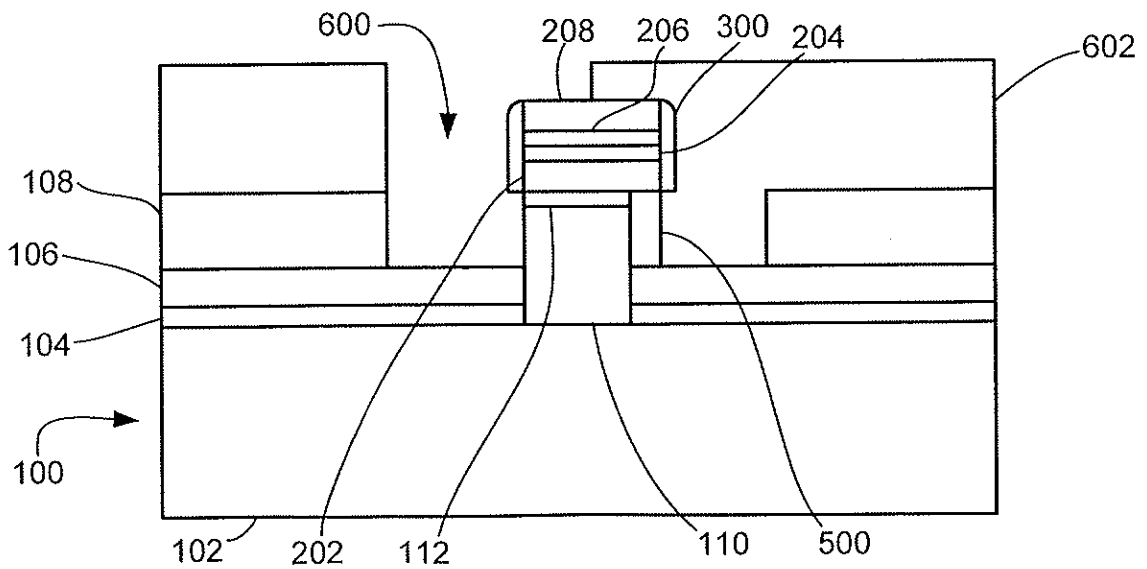


FIG. 6

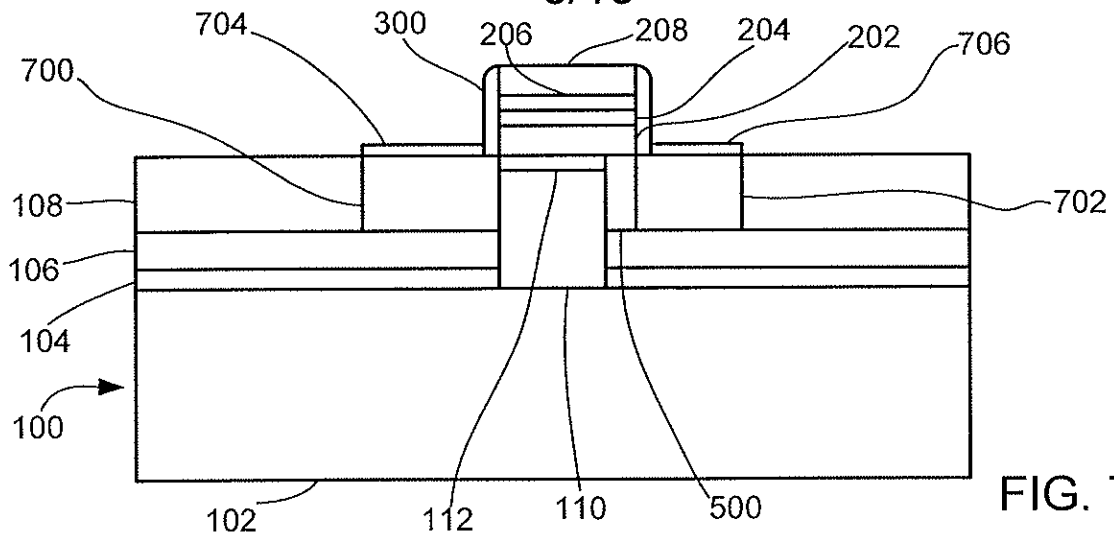


FIG. 7

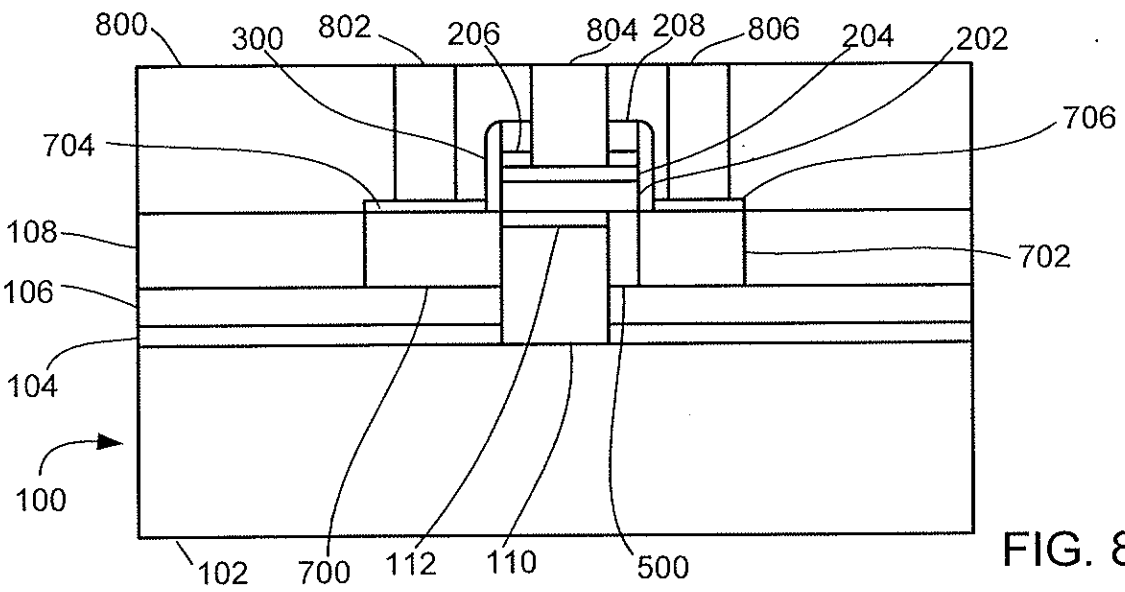


FIG. 8

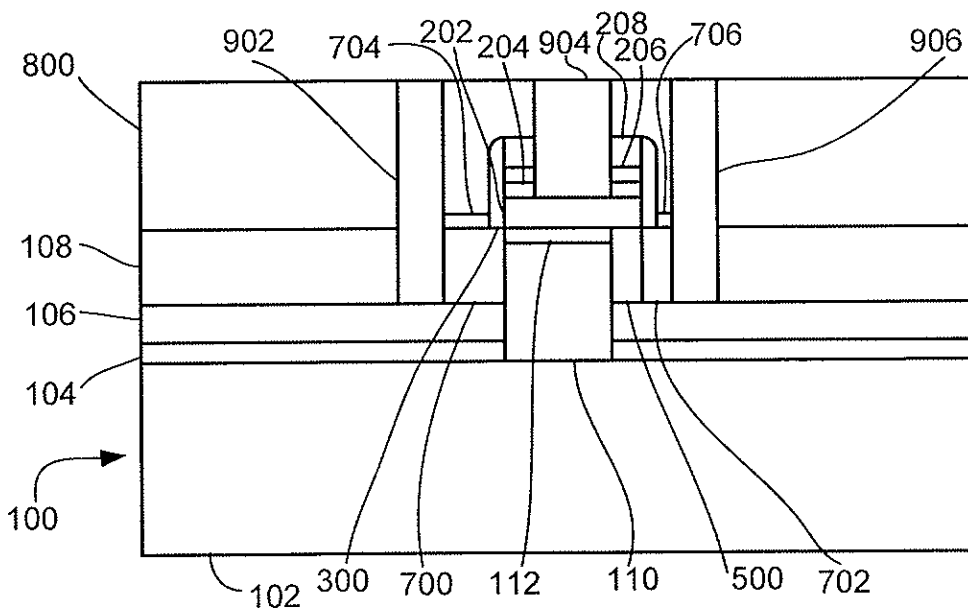


FIG. 9

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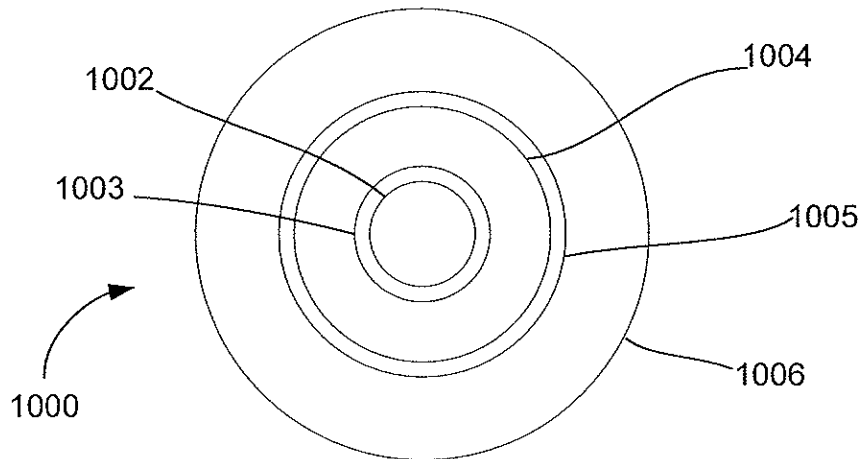


FIG. 10

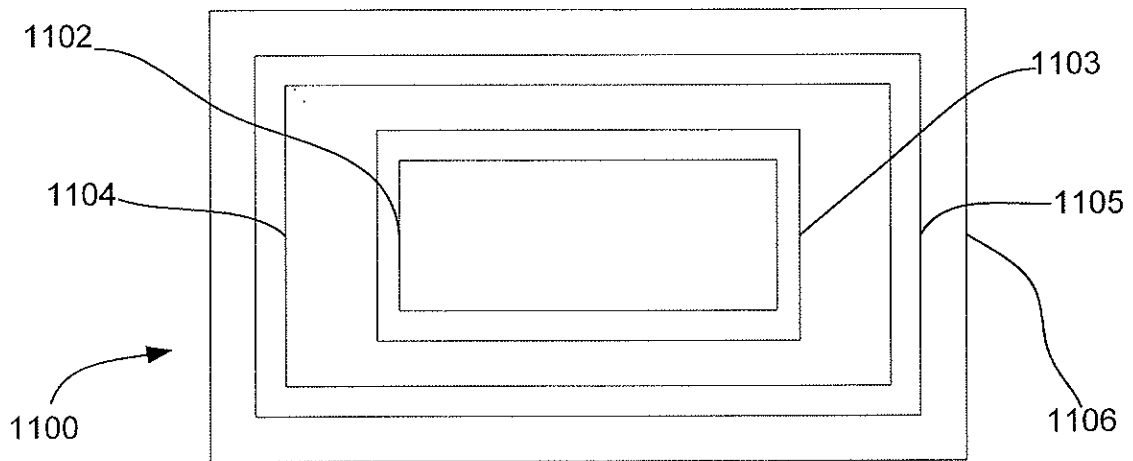


FIG. 11

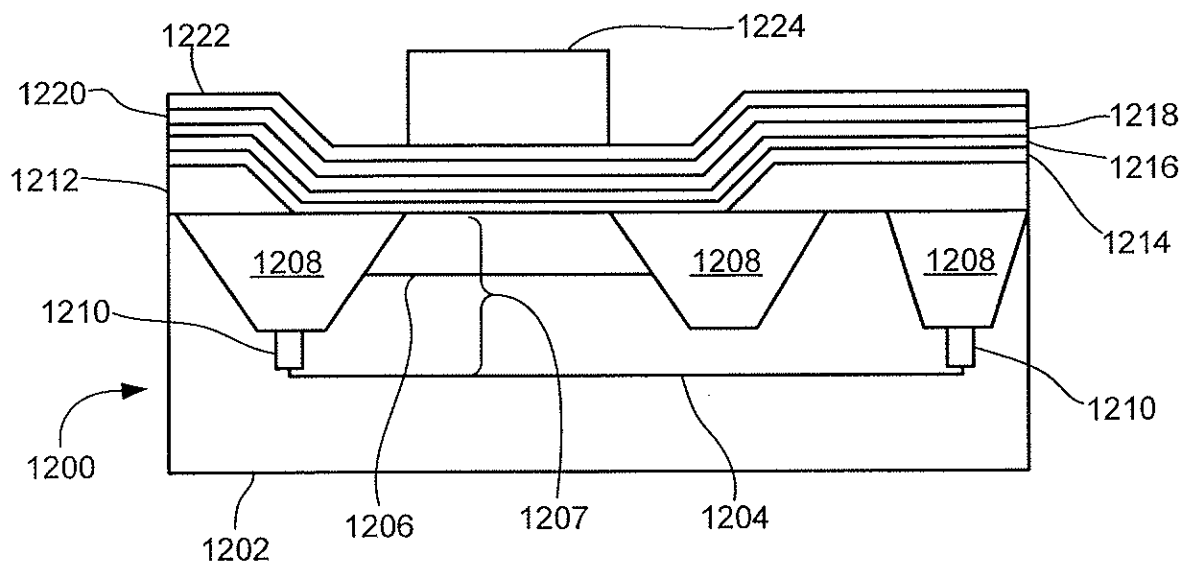


FIG. 12

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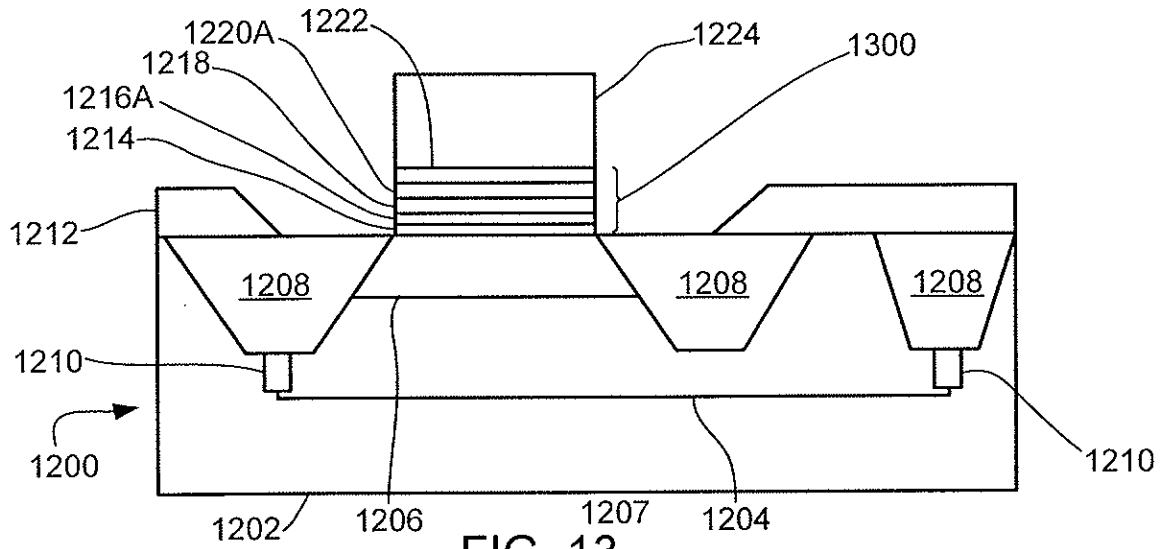


FIG. 13

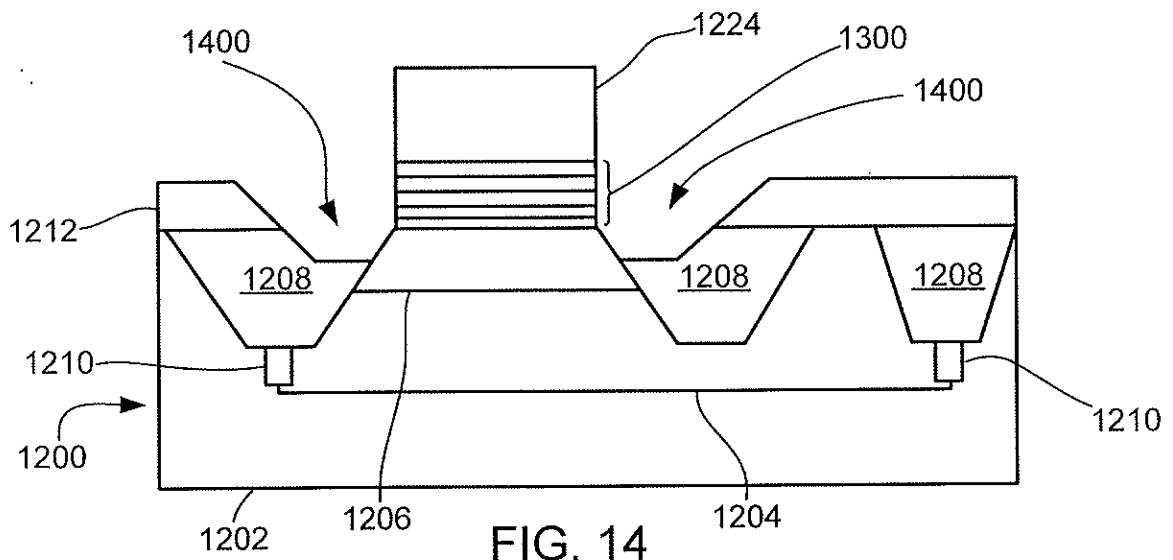


FIG. 14

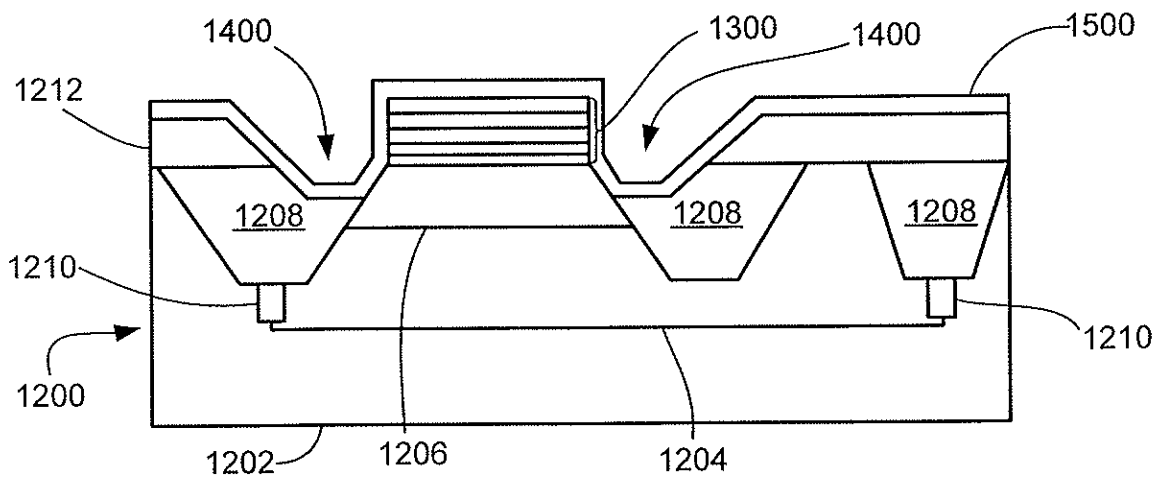
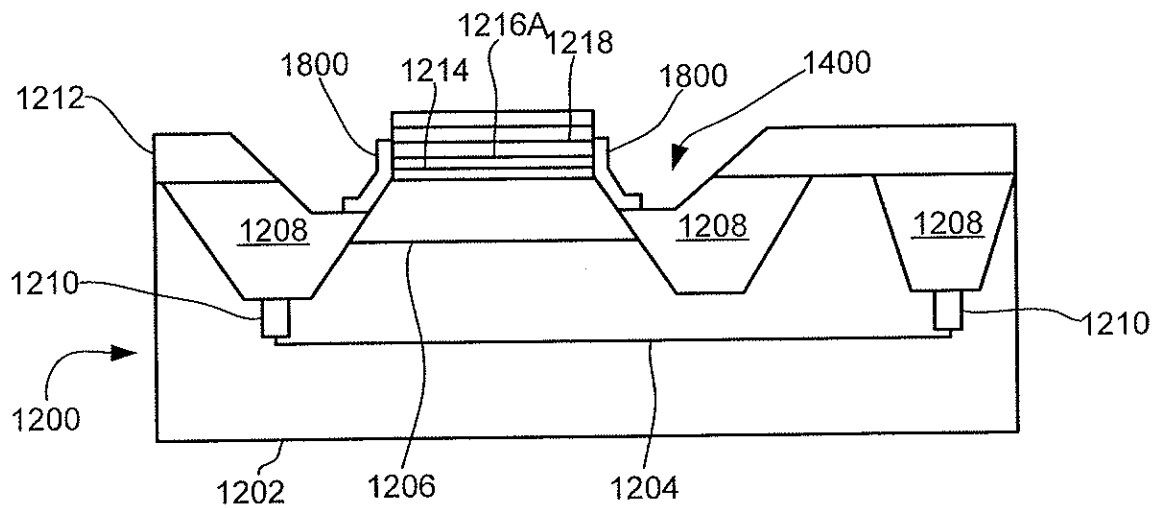
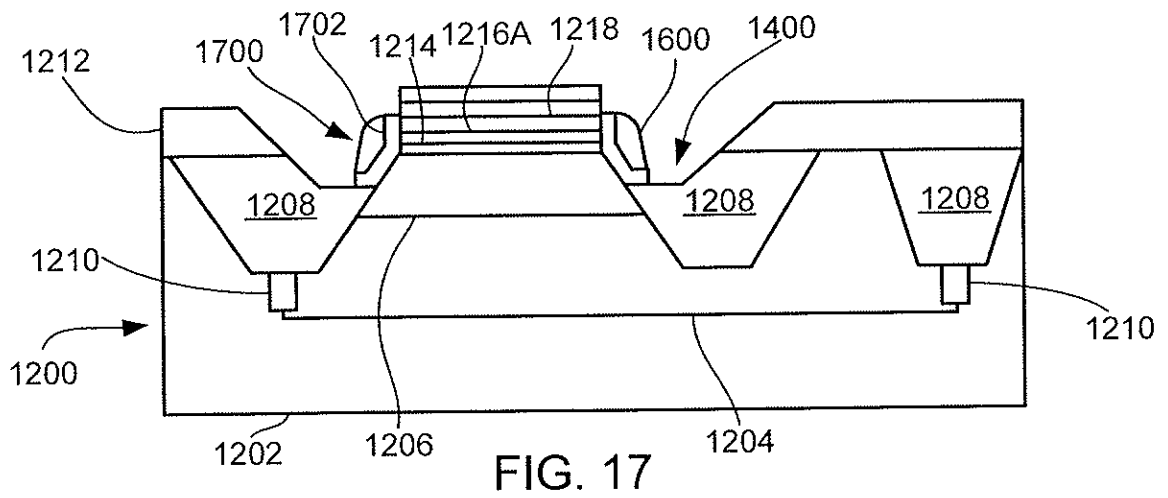
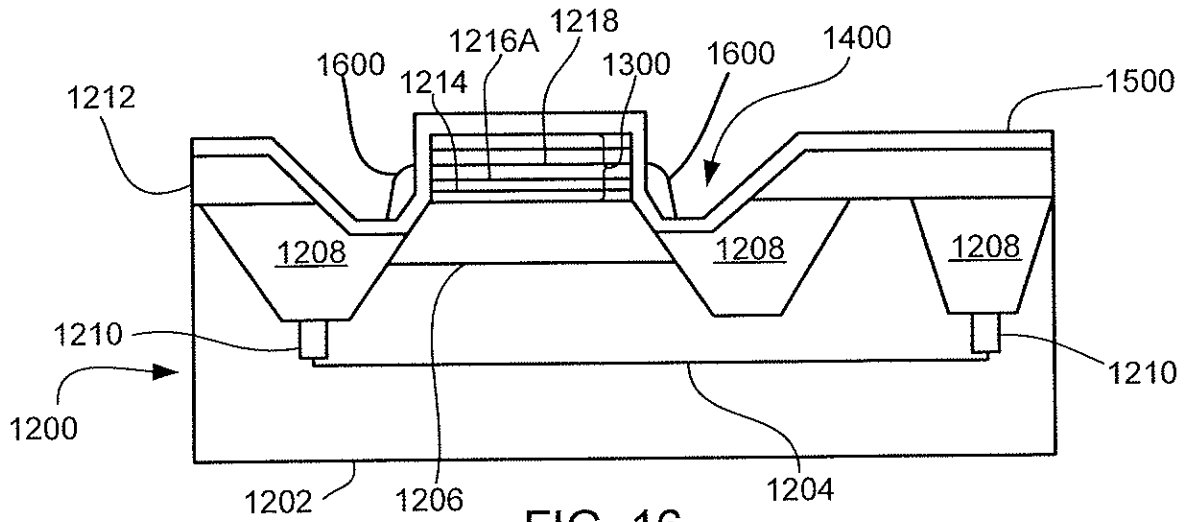


FIG. 15



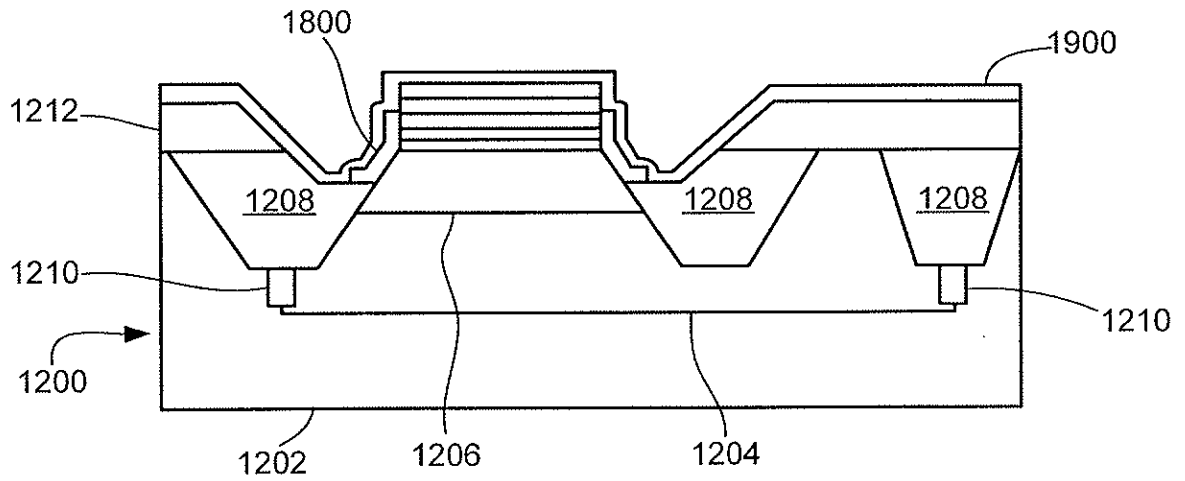


FIG. 19

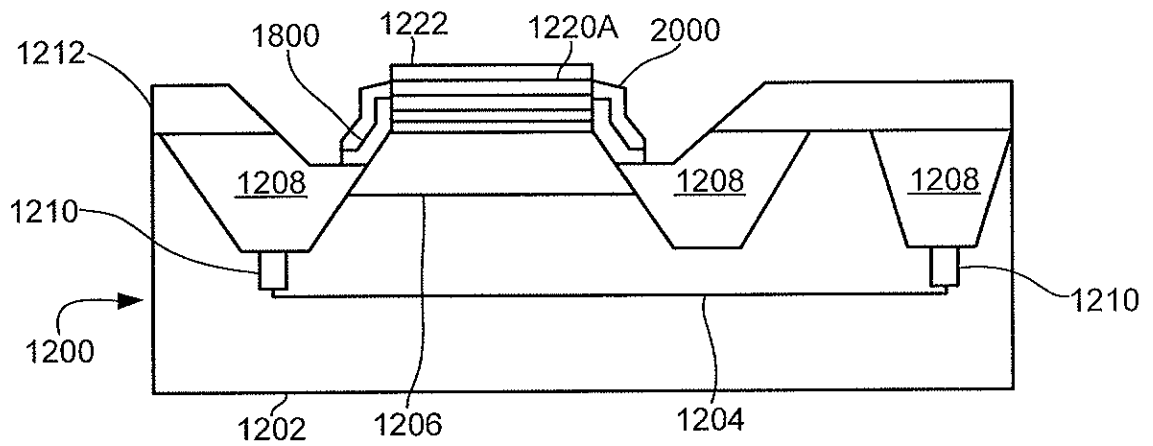
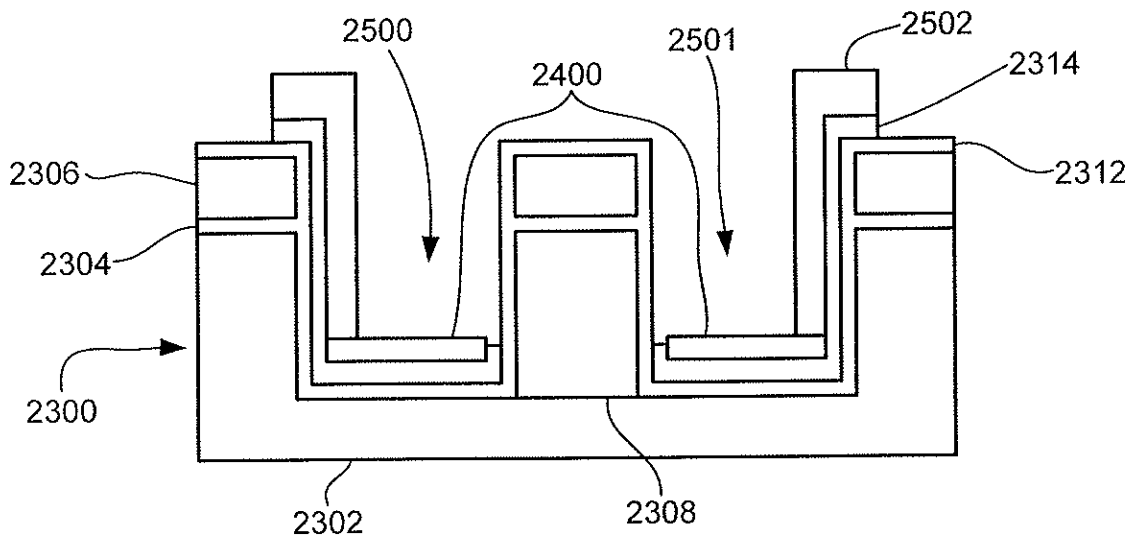
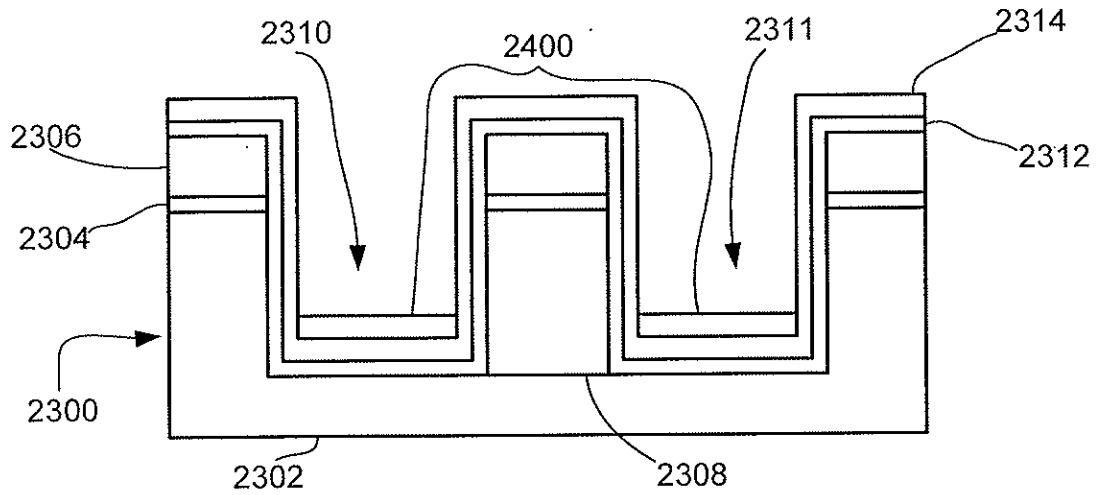
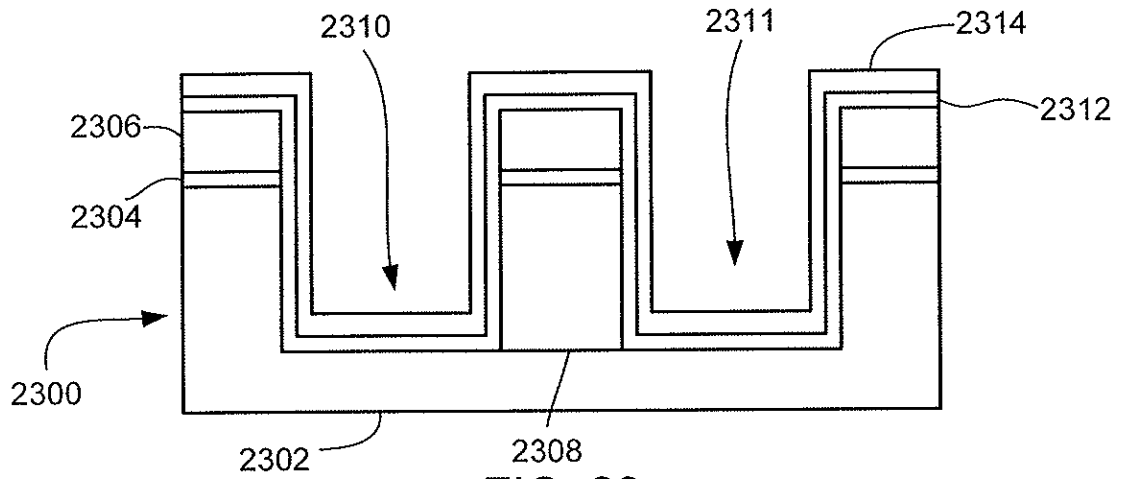


FIG. 20

A cross-sectional view of a semiconductor device. The device consists of a multi-layered substrate. The top layer is labeled 2100. Below it is a layer labeled 1222. Under layer 1222 is a layer labeled 1220A. Below 1220A is a layer labeled 1218. The bottom-most layer is labeled 1214. Two raised regions, labeled 2102, are positioned on top of the substrate. The left raised region is wider than the right one. The layers 1222, 1220A, and 1218 are continuous across the width of the device, including under the raised regions.

FIG. 22B



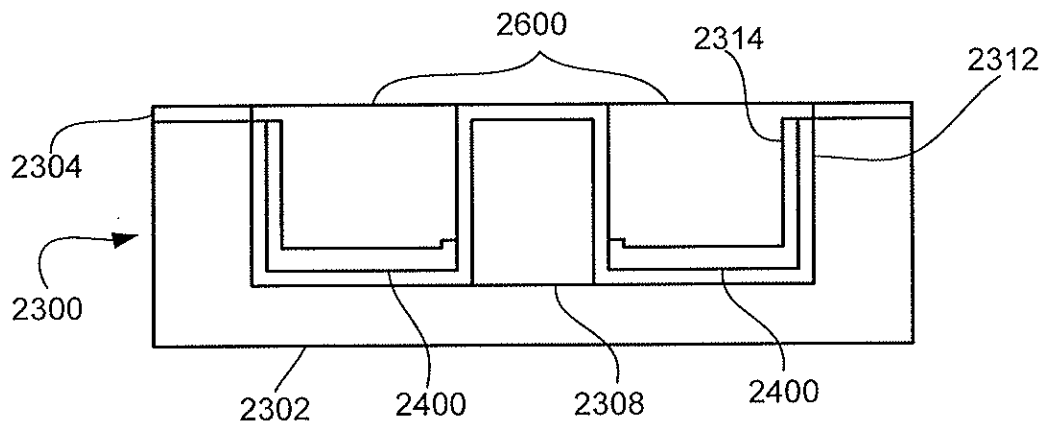


FIG. 26

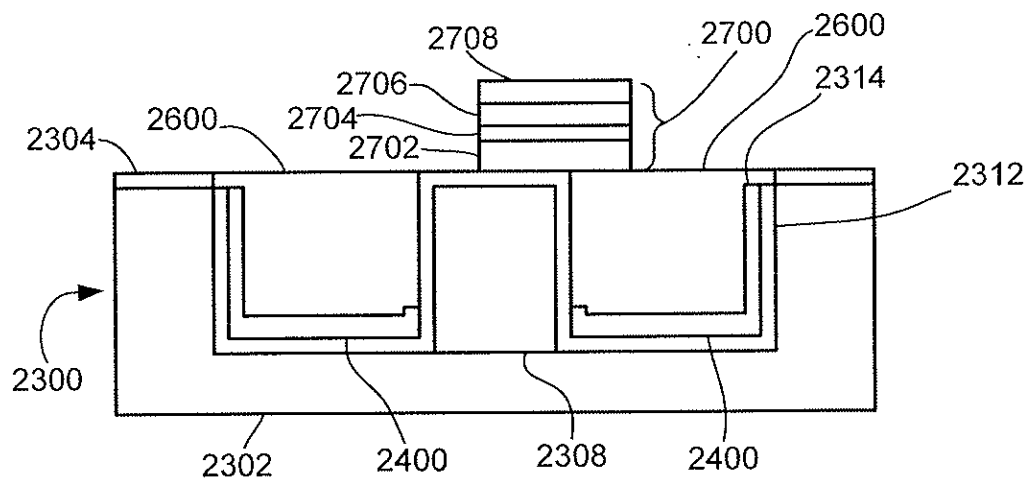


FIG. 27

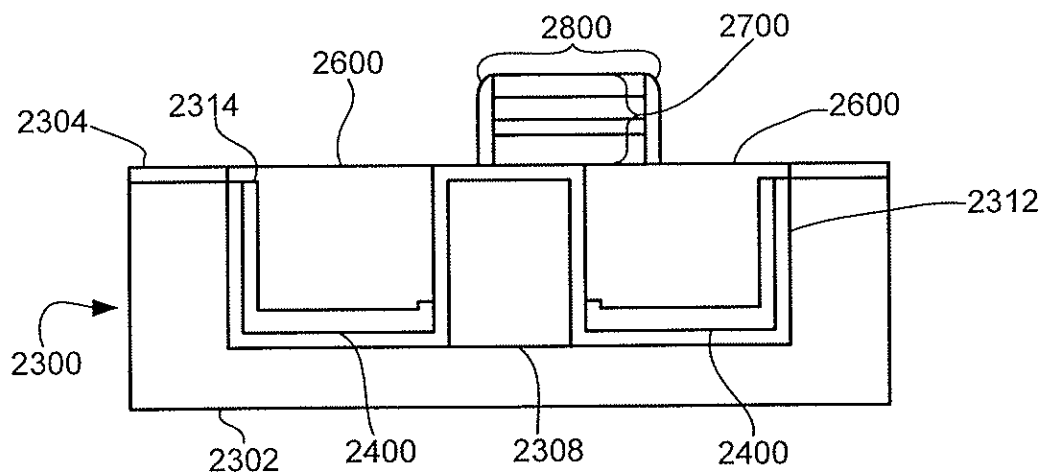


FIG. 28

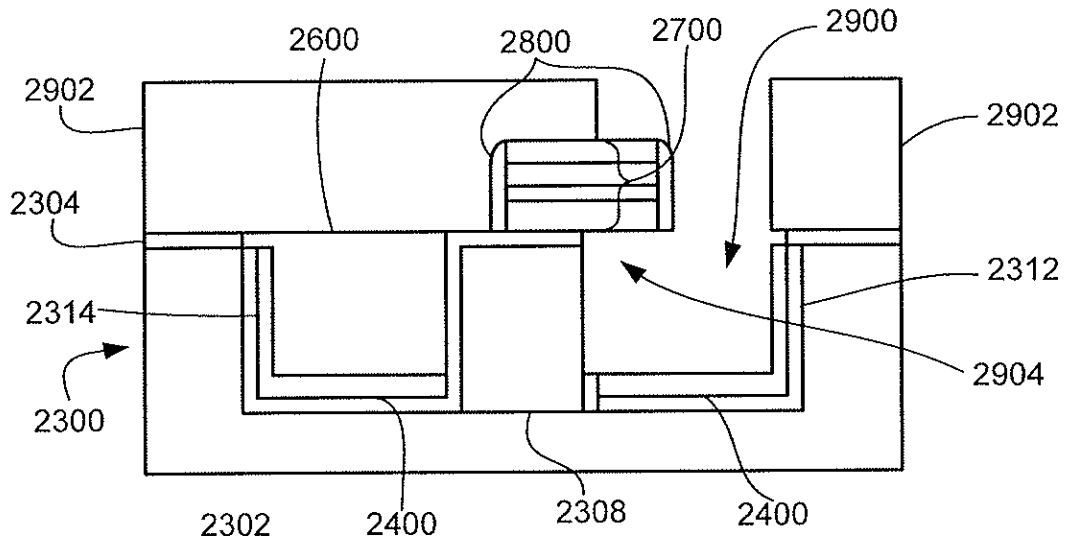


FIG. 29

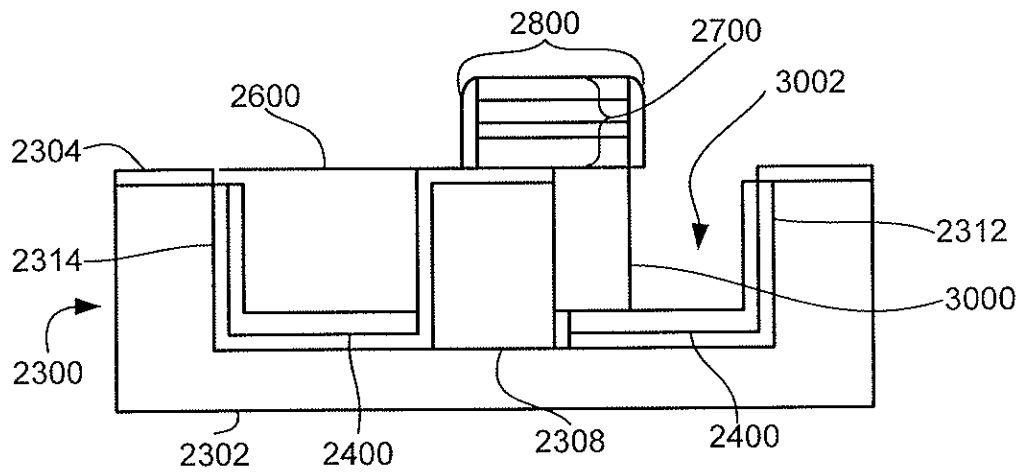


FIG. 30

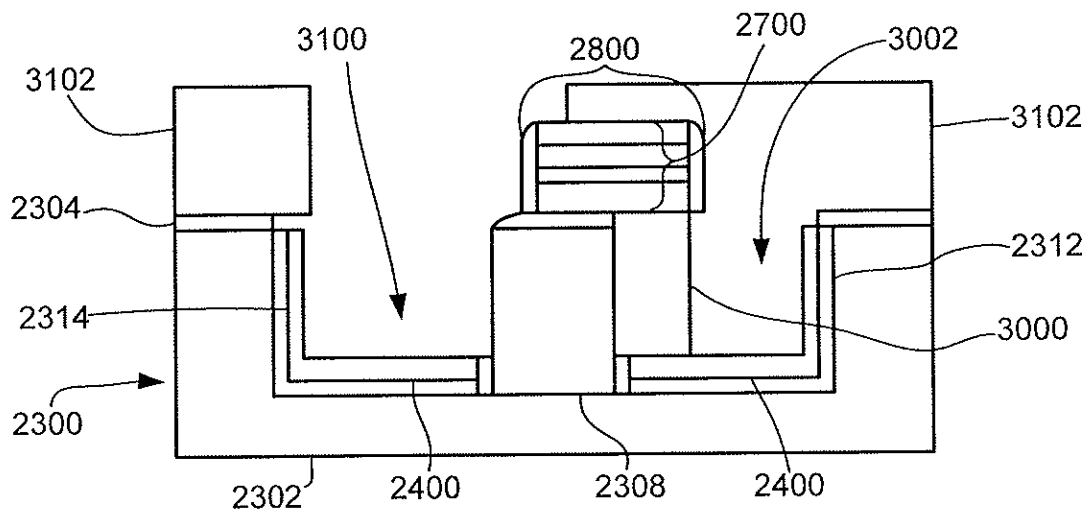


FIG. 31

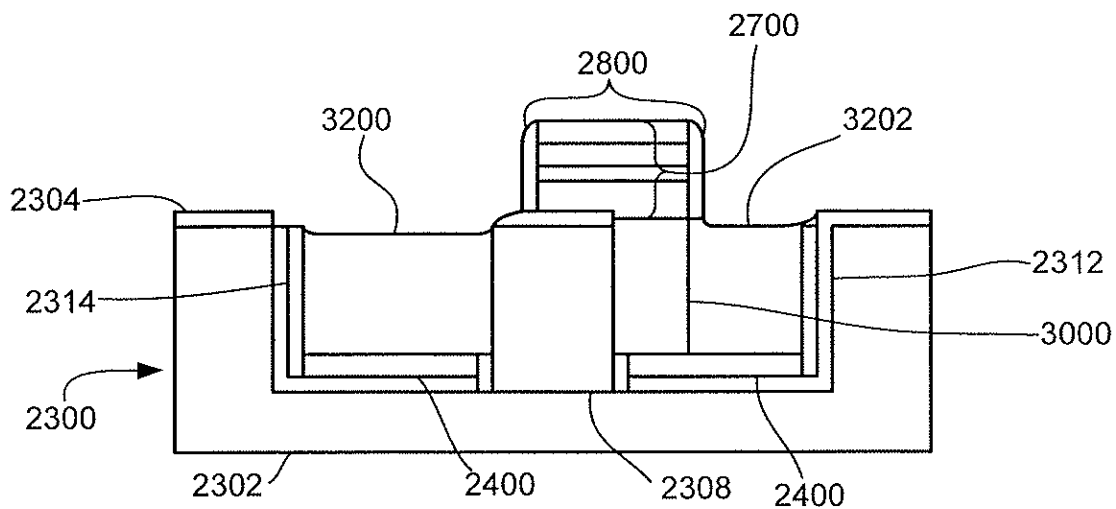


FIG. 32

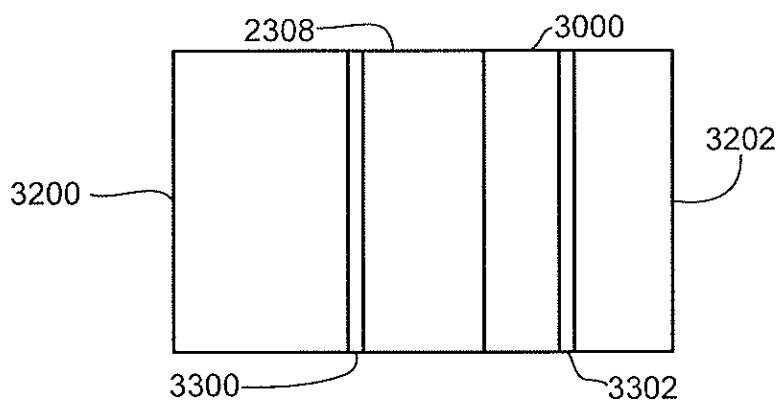


FIG. 33

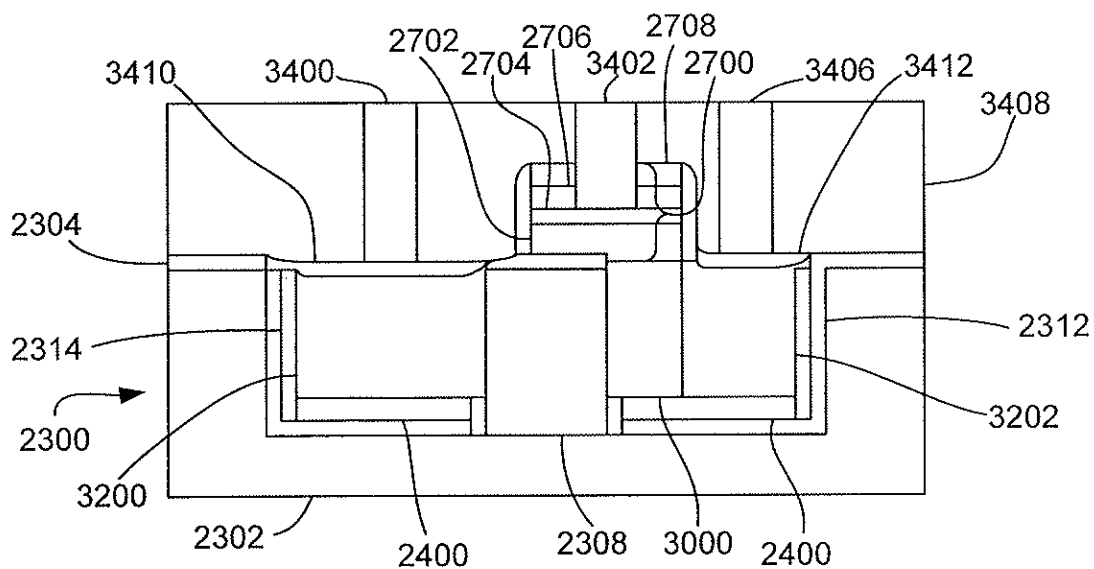


FIG. 34

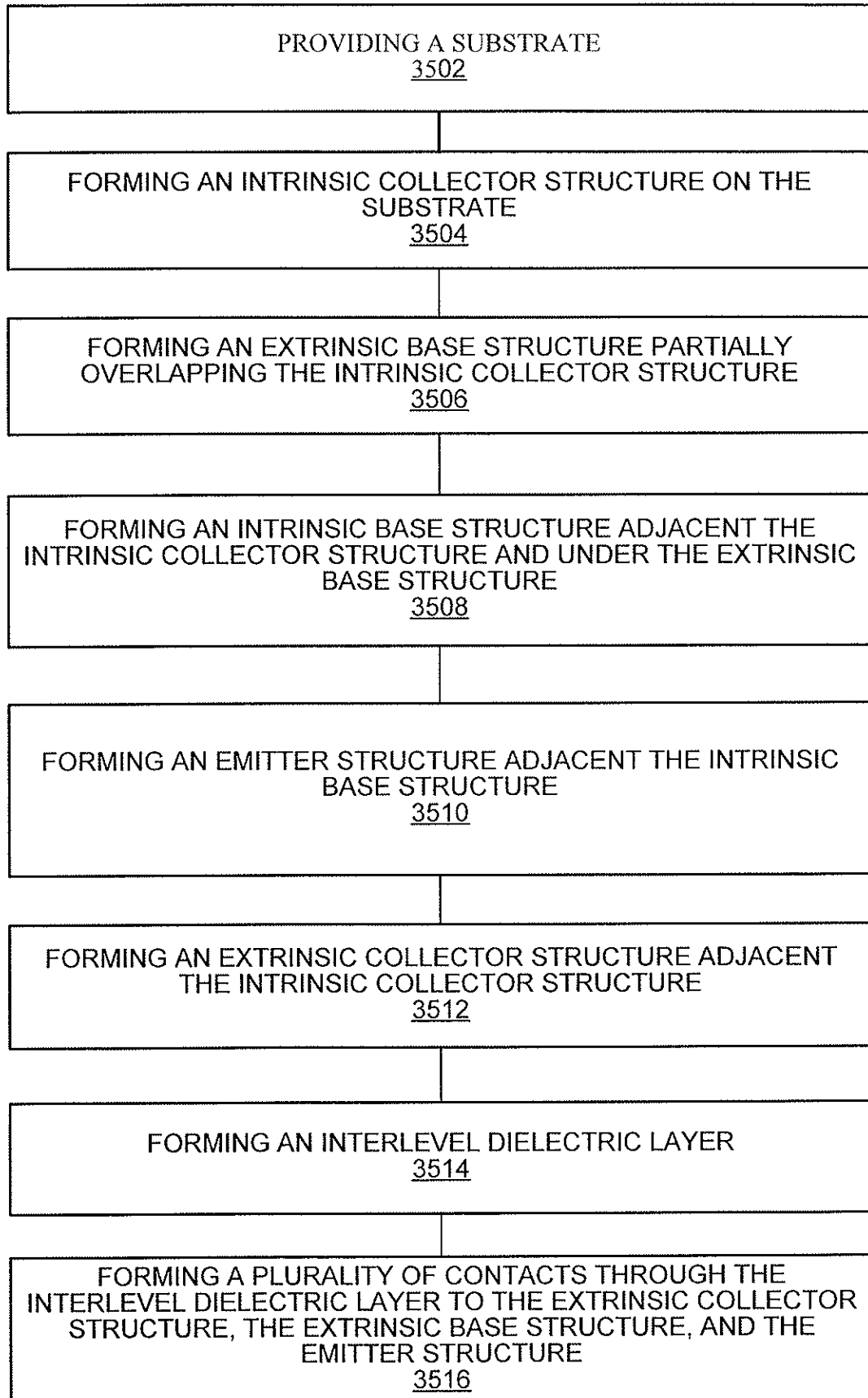
3500 

FIG. 35