Patent claims:

1. A monolithic integrated semiconductor structure containing the following layer structure:

A) a carrier layer based on doped or undoped Si,

B) optionally a layer having the composition $B_xAl_yGa_zN_tP_v$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, t = 0 - 0.1 and v = 0.9 - 1,

C) a relaxation layer having the composition $B_xAl_yGa_zIn_uP_vSb_w$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1 and w = 0 - 1, wherein w and/or u is on the side facing toward layer A) or B) smaller than, equal to, or bigger than on the side facing away from layer A) or B) and varies or is constant within the relaxation layer, and wherein v = 1 - w and/or y = 1 - u - x - z,

D) optionally a layer for blocking misfit dislocations and having the composition $B_xAl_yGa_zIn_uP_vSb_wN_t$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1, w = 0 - 1 and t = 0 - 0.1,

E) optionally a layer for hetero-offset having the composition $B_xAl_yGa_zIn_uP_vSb_wN_tAs_r$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1, w = 0 - 1, t = 0 - 0.1 and r = 0 - 1, and

F) an arbitrary, preferably group III/V, semiconductor material, or a combination of several different arbitrary semiconductor materials,

wherein the sum of the above stoichiometric indices for all group III elements is always 1 and

wherein the sum of the above stoichiometric indices for all group V elements is also always 1.

2. The semiconductor structure according to claim 1, wherein the compositions of layers C), D), and E) are selected such that the lattice constant of one of layers D) and/or E) and/or of the side of layer C) facing away from layer A) or B) substantially corresponds to the lattice constant of layer F).

3. The semiconductor structure according to claim 1 or 2, wherein layer A) on the side facing toward layer B) or C) is a Si 001 surface of a Si monocrystal.

4. The semiconductor structure according to one of claims 1 to 3, wherein layer B) has a thickness of 20 - 100 nm and/or a p- or n-doping concentration of $1*10^{15}$ - $1*10^{21}$ cm^{-3}.

5. The semiconductor structure according to one of claims 1 to 4, wherein layer B) has one of the following compositions:

z = v = 1, x = y = t = 0 or

y = v = 1, x = z = t = 0 or

x = 0.01 - 0.1, y = 0.90 - 0.99, z = t = 0, v = 1 or

x = 0.01 - 0.1, z = 0.90 - 0.99, y = t = 0, v = 1 or

t = 0.01 - 0.1, v = 0.90 - 0.99, y = x = 0, z = 1.

6. The semiconductor structure according to one of claims 1 to 5, wherein in layer C) w and/or u is on the side facing toward layer A) or B) smaller than on the side facing away from layer A) or B) and in the direction of a location coordinate that is orthogonal to the main faces of the layer C) passes a maximum, wherein w and/or u in the maximum optionally may be larger than on the side facing away from layer A) or B).

7. The semiconductor structure according to one of claims 1 to 6, wherein layer C) is formed of a multitude of partial layers, in particular 1 - 30 layers, preferably 2 - 10 layers, wherein w and/or u is variable or constant within a partial layer.

8. The semiconductor structure according to one of claims 1 to 7, wherein layer C) has a thickness of 1 - 500 nm, in particular 100 - 400 nm, and/or is undoped or has a p- or n-doping concentration of $1*10^{15}$ - $1*10^{21}$ cm^{-3}.

9. The semiconductor structure according to one of claims 1 to 8, wherein layer C) or the partial layers thereof have one of the following compositions:

$y = 1$, $x = z = u = 0$, $v = 1 - w$ or

$x = z = 0$, $y = 1 - u$, $v + w = 1$.

10. The semiconductor structure according to one of claims 1 to 9, wherein layer D) has a thickness of 1 - 150 nm and/or is undoped and/or has a p- or n-doping concentration of $1*10^{15}$ - $1*10^{21}$ cm^{-3}.

11. The semiconductor structure according to one of claims 1 to 10, wherein layer D) is formed of an individual layer or a multitude of partial layers, in particular 1 - 10 layers, preferably 2 - 5 layers.

12. The semiconductor structure according to one of claims 1 to 11, wherein layer D) or the partial layers thereof have one of the following compositions:

$x = 0 - 0.1$, $y = 0.9 - 1$, $v = 0 - 0.7$, $w = 0.3 - 1$, $z = u = t = 0$ or

$u = 1$, $w = 0 - 0.5$, $v = 0.5 - 1$, $t = 0 - 0.1$, $x = y = z = 0$ or

$y = 1$, $v = 0 - 0.7$, $w = 0.3 - 1$, $t = 0 - 0.1$, $x = z = u = 0$ or

$u = 0.9 - 1$, $x = 0 - 0.1$, $v = 0.5 - 1$, $w = 0 - 0.5$, $y = z = t = 0$.

13. The semiconductor structure according to one of claims 1 to 12, wherein layer E) has a thickness of 5 - 200 nm, in particular 10 - 100 nm, and/or is undoped and/or has a p- or n-doping concentration of $1*10^{15} - 1*10^{21}$ cm^{-3}.

14. The semiconductor structure according to one of claims 1 to 13, wherein layer E) is formed of an individual layer or a multitude of partial layers, in particular 1 - 10 layers, preferably 2 - 5 layers.

15. The semiconductor structure according to one of claims 1 to 14, wherein layer E) has one of the following compositions:

y = 1, v = 0.2 - 0.5, w = 0.5 - 0.8, x = z = u = t = r = 0 or

y = 1, w = 0.4 - 0.8, r = 0.2 - 0.6, x = z = u = v = t = 0.

16. A method for producing a monolithic integrated semiconductor structure according to one of claims 1 to 15,

wherein on a layer A), optionally a layer B) is epitaxially grown,

on layer A) or B), a layer C) is epitaxially grown,

on layer C), optionally a layer D) and/or E) is epitaxially grown,

on layer C) or D) or E), a layer F) is epitaxially grown.

17. The method according to claim 16, wherein a layer or several of layers A), B), C), D), E), and/or F) are p- or n-doped.

18. The method according to claim 16 or 17 comprising the following steps:

a substrate containing layer A) is placed in an epitaxy apparatus, in particular a metal-organic vapor-phase epitaxy (MOVPE) apparatus,

a carrier gas is loaded with educts in defined concentrations according to the given composition

of a layer A), B), C), D), and E), if applicable also F), or the partial layers thereof,

the loaded carrier gas is conducted over the surface of the substrate heated to a temperature in the range from of 300 °C to 800 °C, in particular 400 °C to 625 °C in the case of layers C) and D) or the partial layers thereof, or 525 °C to 725 °C in the case of layer E) or the partial layers thereof, or on the surface of the uppermost layer on the substrate for a defined time of exposure, wherein the total concentration of the educts and the time of exposure are adjusted to each other such that the semiconductor layer with a given layer thickness is epitaxially formed on the surface of the substrate or the surface the uppermost layer on the substrate, wherein the epitaxial growth mode may be continuous, preferably by means of flow rate modulation epitaxy (FME) or by means of atomic layer deposition (ALD).

19. The method according to claim 18, wherein layer C) is grown in partial layers, and wherein between the growth of two partial layers and/or after the growth of the last partial layer, baking of the substrate at 550 °C to 750 °C, in particular at 600 °C to 725 °C, occurs.

20. The method according to claim 18 or 19, wherein as educts for the construction of the layers are used:

C1-C5 trialkyl gallium, in particular triethyl gallium ($Ga(C_2H_5)_3$), tritertiary-butyl gallium and/or trimethyl gallium ($Ga(CH_3)_3$) as Ga educt,

diborane (B_2H_6)or C1-C5 trialkyl borane, in particular tritertiary-butyl borane and triethyl borane ($B(C_2H_5)_3$)and/or borane-amine adducts such as dimethyl aminoborane as B educt,

alane-amine adducts or C1-C5 trialkyl aluminum, in particular trimethyl aluminum ($Al(CH_3)_3$), tritertiary-butyl aluminum and/or dimethyl ethylamine alane as Al educt,

C1-C5 trialkyl indium, in particular trimethyl indium ($In(CH_3)_3$) as In educt,

phosphine (PH_3) and/or C1-C5 alkyl phosphine, in particular tertiary-butyl phosphine ($t-(C_4H_9)-PH_2$) as P educt,

arsine (AsH_3) and/or C1-C5 alkyl arsine and/or trimethyl arsine ($As(CH_3)_3$), in particular tertiary-butyl arsine ($t-(C_4H_9)-AsH_2$) as As educt,

C1-C5 trialkyl antimony, in particular triethyl antimony ($Sb(C_2H_5)_3$) and/or trimethyl antimony ($Sb(CH_3)_3$) as Sb educt,

ammonia (NH_3), mono(C1-C8)alkyl hydrazine, in particular tertiary-butyl hydrazine ($t-(C_4H_9)NH_2$) and/or 1,1-di(C1-C5)alkyl hydrazine, in particular 1,1-dimethyl hydrazine ($(CH_3)2-N-NH_2$) as N educt,

wherein the C3-C5 alkyl groups may be linear or branched, and

wherein as educts for doping the layers are used: diethyl tellurium (DETe), dimethyl zinc (DMZn), diethyl zinc (DEZn), ditertiary-butyl silane (DitButSi), silane, ditertiary-butyl sulfide, bis-cyclopentadienyl magnesium, tetrabromomethane.

21. The method according to one of claims 18 to 20, wherein the total pressure of carrier gas and

educts is in the range from of 10 to 1,000 hPa, in particular 50 to 500 hPa, wherein the proportion of the sum of the partial pressures of the educts to the partial pressure of the carrier gas is between 1*10E-6 and 0.5, and wherein the deposition rate is 0.01 to 10 µm/h, in particular 0.05 to 5 µm/h.

22. The use a semiconductor structure according to one of claims 1 to 15 for producing a III/V channel transistor or other group III/V-based components such as a laser, light-emitting diode, detector and solar cell on a silicon substrate.

23. A semiconductor structure obtainable by a method according to one of claims 16 to 21.

Patent claims:

1. A monolithic integrated semiconductor structure containing the following layer structure:

A) a carrier layer based on doped or undoped Si,

B) optionally a layer having the composition B_xAl_y-$Ga_zN_tP_v$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, t = 0 - 0.1 and v = 0.9 - 1,

C) a relaxation layer having the composition B_xAl_y-$Ga_zIn_uP_vSb_w$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1 and w = 0 - 1, wherein w and/or u is on the side facing toward layer A) or B) smaller than, or bigger than on the side facing away from layer A) or B) and varies within the relaxation layer, and wherein v = 1 - w and/or y = 1 - u - x - z,

D) optionally a layer for blocking misfit dislocations and having the composition $B_xAl_yGa_zIn_u$-$P_vSb_wN_t$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1, w = 0 - 1 and t = 0 - 0.1,

E) optionally a layer for hetero-offset having the composition $B_xAl_yGa_zIn_uP_vSb_wN_tAs_r$, wherein x = 0 - 0.1, y = 0 - 1, z = 0 - 1, u = 0 - 1, v = 0 - 1, w = 0 - 1, t = 0 - 0.1 and r = 0 - 1, and

F) an arbitrary, preferably group III/V, semiconductor material, or a combination of several different arbitrary semiconductor materials,

wherein the sum of the above stoichiometric indices for all group III elements is always 1 and

wherein the sum of the above stoichiometric indices for all group V elements is also always 1.

2. The semiconductor structure according to claim 1, wherein the compositions of layers C), D), and E) are selected such that the lattice constant of one of layers D) and/or E) and/or of the side of layer C) facing away from layer A) or B) substantially corresponds to the lattice constant of layer F).

3. The semiconductor structure according to claim 1 or 2, wherein layer A) on the side facing toward layer B) or C) is a Si 001 surface of a Si monocrystal.

4. The semiconductor structure according to one of claims 1 to 3, wherein layer B) has a thickness of 20 - 100 nm and/or a p- or n-doping concentration of $1*10^{15}$ - $1*10^{21}$ cm^{-3}.

5. The semiconductor structure according to one of claims 1 to 4, wherein layer B) has one of the following compositions:

z = v = 1, x = y = t = 0 or

y = v = 1, x = z = t = 0 or

x = 0.01 - 0.1, y = 0.90 - 0.99, z = t = 0, v = 1 or

x = 0.01 - 0.1, z = 0.90 - 0.99, y = t = 0, v = 1 or

t = 0.01 - 0.1, v = 0.90 - 0.99, y = x = 0, z = 1.

6. The semiconductor structure according to one of claims 1 to 5, wherein in layer C) w and/or u is on the side facing toward layer A) or B) smaller than on the side facing away from layer A) or B) and in the direction of a location coordinate that is orthogonal to the main faces of the layer C) passes a maximum, wherein w and/or u in the maximum optionally may be larger than on the side facing away from layer A) or B).

7. The semiconductor structure according to one of claims 1 to 6, wherein layer C) is formed of a multitude of partial layers, in particular 1 - 30 layers, preferably 2 - 10 layers, wherein w and/or u is variable or constant within a partial layer.

8. The semiconductor structure according to one of claims 1 to 7, wherein layer C) has a thickness of 1 - 500 nm, in particular 100 - 400 nm, and/or is undoped or has a p- or n-doping concentration of $1*10^{15}$ - $1*10^{21}$ cm^{-3}.

9. The semiconductor structure according to one of claims 1 to 8, wherein layer C) or the partial layers thereof have one of the following compositions:

$y = 1,\ x = z = u = 0,\ v = 1 - w$ or

$x = z = 0,\ y = 1 - u,\ v + w = 1.$

10. The semiconductor structure according to one of claims 1 to 9, wherein layer D) has a thickness of 1 - 150 nm and/or is undoped and/or has a p- or n-doping concentration of $1*10^{15}$ - $1*10^{21}$ cm^{-3}.

11. The semiconductor structure according to one of claims 1 to 10, wherein layer D) is formed of an individual layer or a multitude of partial layers, in particular 1 - 10 layers, preferably 2 - 5 layers.

12. The semiconductor structure according to one of claims 1 to 11, wherein layer D) or the partial layers thereof have one of the following compositions:

$x = 0 - 0.1$, $y = 0.9 - 1$, $v = 0 - 0.7$, $w = 0.3 - 1$, $z = u = t = 0$ or

$u = 1$, $w = 0 - 0.5$, $v = 0.5 - 1$, $t = 0 - 0.1$, $x = y = z = 0$ or

$y = 1$, $v = 0 - 0.7$, $w = 0.3 - 1$, $t = 0 - 0.1$, $x = z = u = 0$ or

$u = 0.9 - 1$, $x = 0 - 0.1$, $v = 0.5 - 1$, $w = 0 - 0.5$, $y = z = t = 0$.

13. The semiconductor structure according to one of claims 1 to 12, wherein layer E) has a thickness of 5 - 200 nm, in particular 10 - 100 nm, and/or is undoped and/or has a p- or n-doping concentration of $1*10^{15} - 1*10^{21}$ cm^{-3}.

14. The semiconductor structure according to one of claims 1 to 13, wherein layer E) is formed of an individual layer or a multitude of partial layers, in particular 1 - 10 layers, preferably 2 - 5 layers.

15. The semiconductor structure according to one of claims 1 to 14, wherein layer E) has one of the following compositions:

$y = 1$, $v = 0.2 - 0.5$, $w = 0.5 - 0.8$, $x = z = u = t = r = 0$ or

$y = 1$, $w = 0.4 - 0.8$, $r = 0.2 - 0.6$, $x = z = u = v = t = 0$.

16. A method for producing a monolithic integrated semiconductor structure according to one of claims 1 to 15,

wherein on a layer A), optionally a layer B) is epitaxially grown,

on layer A) or B), a layer C) is epitaxially grown,

on layer C), optionally a layer D) and/or E) is epitaxially grown,

on layer C) or D) or E), a layer F) is epitaxially grown.

17. The method according to claim 16, wherein a layer or several of layers A), B), C), D), E), and/or F) are p- or n-doped.

18. The method according to claim 16 or 17 comprising the following steps:

a substrate containing layer A) is placed in an epitaxy apparatus, in particular a metal-organic vapor-phase epitaxy (MOVPE) apparatus,

a carrier gas is loaded with educts in defined concentrations according to the given composition

of a layer A), B), C), D), and E), if applicable also F), or the partial layers thereof,

the loaded carrier gas is conducted over the surface of the substrate heated to a temperature in the range from of 300 °C to 800 °C, in particular 400 °C to 625 °C in the case of layers C) and D) or the partial layers thereof, or 525 °C to 725 °C in the case of layer E) or the partial layers thereof, or on the surface of the uppermost layer on the substrate for a defined time of exposure, wherein the total concentration of the educts and the time of exposure are adjusted to each other such that the semiconductor layer with a given layer thickness is epitaxially formed on the surface of the substrate or the surface the uppermost layer on the substrate, wherein the epitaxial growth mode may be continuous, preferably by means of flow rate modulation epitaxy (FME) or by means of atomic layer deposition (ALD).

19. The method according to claim 18, wherein layer C) is grown in partial layers, and wherein between the growth of two partial layers and/or after the growth of the last partial layer, baking of the substrate at 550 °C to 750 °C, in particular at 600 °C to 725 °C, occurs.

20. The method according to claim 18 or 19, wherein as educts for the construction of the layers are used:

C1-C5 trialkyl gallium, in particular triethyl gallium ($Ga(C_2H_5)_3$), tritertiary-butyl gallium and/or trimethyl gallium ($Ga(CH_3)_3$) as Ga educt,

diborane (B_2H_6)or C1-C5 trialkyl borane, in particular tritertiary-butyl borane and triethyl borane ($B(C_2H_5)_3$)and/or borane-amine adducts such as dimethyl aminoborane as B educt,

alane-amine adducts or C1-C5 trialkyl aluminum, in particular trimethyl aluminum ($Al(CH_3)_3$), tritertiary-butyl aluminum and/or dimethyl ethylamine alane as Al educt,

C1-C5 trialkyl indium, in particular trimethyl indium ($In(CH_3)_3$) as In educt,

phosphine (PH_3) and/or C1-C5 alkyl phosphine, in particular tertiary-butyl phosphine ($t-(C_4H_9)-PH_2$) as P educt,

arsine (AsH_3) and/or C1-C5 alkyl arsine and/or trimethyl arsine ($As(CH_3)_3$), in particular tertiary-butyl arsine ($t-(C_4H_9)-AsH_2$) as As educt,

C1-C5 trialkyl antimony, in particular triethyl antimony ($Sb(C_2H_5)_3$) and/or trimethyl antimony ($Sb(CH_3)_3$) as Sb educt,

ammonia (NH_3), mono(C1-C8)alkyl hydrazine, in particular tertiary-butyl hydrazine ($t-(C_4H_9)NH_2$) and/or 1,1-di(C1-C5)alkyl hydrazine, in particular 1,1-dimethyl hydrazine ($(CH_3)2-N-NH_2$) as N educt,

wherein the C3-C5 alkyl groups may be linear or branched, and

wherein as educts for doping the layers are used: diethyl tellurium (DETe), dimethyl zinc (DMZn), diethyl zinc (DEZn), ditertiary-butyl silane (DitButSi), silane, ditertiary-butyl sulfide, bis-cyclopentadienyl magnesium, tetrabromomethane.

21. The method according to one of claims 18 to 20, wherein the total pressure of carrier gas and

educts is in the range from of 10 to 1,000 hPa, in particular 50 to 500 hPa, wherein the proportion of the sum of the partial pressures of the educts to the partial pressure of the carrier gas is between 1*10E-6 and 0.5, and wherein the deposition rate is 0.01 to 10 µm/h, in particular 0.05 to 5 µm/h.

22. The use a semiconductor structure according to one of claims 1 to 15 for producing a III/V channel transistor or other group III/V-based components such as a laser, light-emitting diode, detector and solar cell on a silicon substrate.

23. A semiconductor structure obtainable by a method according to one of claims 16 to 21.