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TEMPORARY SEMICONDUCTOR PACKAGE HAVING DENSE ARRAY EXTERNAL CONTACTS

Field of the Invention

This invention relates generally to semiconductor manufacture and more particularly to an improved package for temporarily packaging semiconductor dice for testing and other purposes.

Background of the Invention

Conventionally packaged semiconductor dice are tested several times during the manufacturing process. A probe test is conducted at the wafer level to test the gross functionality of the dice. Following singulation of the wafer and packaging of the individual dice, full functionality and burn-in tests are performed on each of the

packaged die. These tests are typically performed using standardized equipment that provides an electrical interface between the external contacts on the package (e.g., terminal leads) and test circuitry.

For example, burn-in ovens are adapted to hold a large number of packaged dice in a chamber with temperature cycling capability. During the burn-in test the integrated circuits are electrically tested at different temperatures. A burn-in board mountable within the chamber, includes electrical connectors that mate with the external leads on the packaged dice to establish an electrical interconnection between the individually packaged dice and test circuitry. For packaged dice having a male external contact, such as external leads formed as pins, the burn-in board may include socket connectors. For packaged dice having female external leads the burn-in board may include pogo pin connectors.

Because semiconductor dice are packaged in standardized configurations, the burn-in boards are also standardized. For example, one common semiconductor package for a single die is known as a small outline j-lead package (SOJ). A burn-in board for SOJ packages will include standardized sockets that mate with the j-leads for the packages. In addition, the spacing for the sockets will be such that a large number of packages can be mounted on a single board in a dense closely spaced array.

In addition to the boards being standardized, there is also associated equipment, such as automated handling apparatus, that is standardized for a particular package configuration. Other standardized packages for a single die include the dual in-line (DIP) package and the zigzag in-line package (ZIP).

Recently, semiconductor dice have been supplied by manufacturers in an unpackaged or bare configuration. A known good die (KGD) is an unpackaged die that has been

tested to a quality and reliability level equal to the packaged product. To certify a die as a known good die the unpackaged die must be burn-in tested. This has led to the development of test carriers that hold a single unpackaged die for burn-in and other tests. Each test carrier houses a die for testing and also provides the electrical interconnection between the die and external test circuitry. Exemplary test carriers are disclosed in U.S. Patent No. 5,302,891 to Wood et al. and U. S. Patent No. 5,408,190 to Wood et al.

One aspect of these carriers is that they require specialized test equipment, such as specialized burn-in boards and handling equipment, that are different than the equipment used for testing conventionally packaged dice. In addition, the prior art carriers are larger than conventionally packaged dice and therefore require more and larger test equipment to achieve the same throughputs. It would be advantageous to provide a test carrier for semiconductor dice that could be used with standardized test equipment.

Another aspect of the prior art carriers for testing semiconductor dice is that the external contacts for the carriers have a limited pin out capability. Typically, the carriers include external contacts formed as pins that mate with corresponding sockets on the burn-in board. With this type of external contact configuration there may not be enough external contacts to accommodate a die having a large number of closely spaced bond pads. In general, the bond pads on semiconductor dice are becoming smaller and more densely spaced. It would be advantageous to provide a carrier for semiconductor dice having a dense external contact configuration capable of handling dice with large numbers of bond pads.

The present invention recognizes that a carrier can be constructed as a temporary package having a standard outline and external contacts arranged in a dense array. In view of the foregoing, it is an object of the present invention to provide a temporary package for semiconductor dice that can be used for testing and other purposes. It is another object of the present invention to provide a temporary package for semiconductor dice having output contacts arranged in a dense array with a high packing fraction. It is a further object of the present invention to provide a temporary semiconductor package that has a JEDEC standard outline and JEDEC standard external contact configuration. Other objects, advantages and capabilities of the present invention will become more apparent as the description proceeds.

Summary of the Invention

In accordance with the present invention, an improved temporary package for a semiconductor die is provided. The temporary package has an outline and external lead configuration that matches a conventional semiconductor package. In addition, the external leads are formed in a dense array to accommodate a large number of device bond pads. Suitable dense arrays and lead configurations for the external leads can include: land grid arrays (LGA), pin grid arrays (PGA), ball grid arrays (BGA) and dense perimeter arrays. The standard outline and lead configuration of the temporary package permit standardized burn-in boards and automated package handling equipment to be used during a test procedure for known good die.

The temporary package includes a base, an interconnect and a force applying mechanism. The package base includes internal conductors in electrical communication with the external contacts. The package base can be formed of either

ceramic or plastic. With ceramic, the package base can be formed using a ceramic lamination process or a ceramic dip formation process (Cerdip). The package base can also be formed of plastic using a 3-D injection molding process or using a ceramic dip formation (Cerdip) process combined with injection molding.

The interconnect for the package is mounted to the base and wire bonded to the conductors formed on the package base. The interconnect can be formed of silicon with raised contact members that contact and establish electrical communication with the bond pads on the die. The interconnect can also be formed with microbump contact members mounted on a plastic film similar to two layer TAB tape.

The force applying mechanism for the package includes a pressure plate, a spring and a cover. The force applying mechanism functions to secure the die within the base and to maintain the die and interconnect in electrical contact. The force applying mechanism is secured to the base with a latching mechanism.

The package is assembled by optically aligning the die and the interconnect. Prior to the alignment procedure the interconnect is mounted within the package base and wire bonded to form an electrical path between the contact members on the interconnect and the external contacts on the package base. During the alignment procedure, the die and force applying mechanism of the package can be held by an assembly tool. Flip chip optical alignment can be used to align the bond pads on the die to the contact members on the interconnect. The assembly tool then places the die on the interconnect and attaches the force applying mechanism to the package base.

Brief Description of the Drawings

Figure 1 is an exploded perspective view of a package constructed in accordance with the invention;

Figure 2 is a bottom view of the package base showing the external contacts formed in a dense grid array;

Figure 2A is a cross sectional view taken along section line 2A-2A of Figure 2 showing external contacts formed as flat pads in a land grid array (LGA);

Figure 2B is a cross sectional view taken along section line 2B-2B of Figure 2 showing external contacts formed as pins in a pin grid array (PGA);

Figure 2C is a cross sectional view taken along section line 2C-2C of Figure 2 showing external contacts formed as bumps in a bumped grid array (BGA);

Figure 2D is a cross sectional view taken along section line 2D-2D of Figure 2 showing the laminated ceramic layers of the base for the package;

Figure 3 is a cross sectional view of the assembled package;

Figures 3A is a cross sectional view equivalent to Figure 3 showing an alternate embodiment package;

Figure 4 is a plan view of the interconnect for the package shown in Figure 1;

Figure 5 is a cross sectional view taken along section line 5-5 of Figure 4 showing a raised contact member on the interconnect electrically contacting a device bond pad on the die; and

Figure 5A is a cross sectional view equivalent to Figure 5 of an alternate embodiment interconnect having a microbump contact member.

Detailed Description of the Preferred Embodiments

Referring to Figure 1, an exploded perspective view of a temporary package 10 constructed in accordance with the invention is shown. The package 10 is adapted to hold a semiconductor die 12 and to establish a temporary electrical connection with the die 12 for testing and burn-in. Following the test procedure the die 12 can be removed from the package 10 and used as a known good die.

The package 10, generally stated, includes a package base 14, an interconnect 16, and a force applying mechanism 18. The interconnect 16 establishes electrical communication between the package base 14 and the die 12. The force applying mechanism 18 secures the die 12 to the package base 14 and presses the die 12 against the interconnect 16. The force applying mechanism 18 includes a pressure plate 20, a spring 22 and a cover 24. The package 10 also includes a latching mechanism in the form of clips 26, 28 (Figure 3) which secure the force applying mechanism 18 to the package base 14.

The package base 14 includes a pattern of internal conductors 40 that are in electrical communication with external contacts 38A-38C (Figure 2) formed on a bottom surface 31 (Figure 2) of the package base 14. As will be further explained, the conductors 40 are wire bonded to the interconnect 16 to provide an electrical path between the die 12 and the external contacts 38A-38C. The package base 14 also includes an indicator pocket 37 (Figure 1) that can be used to indicate the orientation of the external contacts 38A-38C with respect to the die 12 (i.e., pin #1 indicator).

As shown in Figure 3, in the assembled package 10, the die 12 is held within a recess 36 formed within the package base 14 and is sandwiched between the interconnect 16 and the cover 24. The interconnect 16 is also mounted within a recess 34 formed within the package base 14. As also shown

in Figure 3, in the assembled package 10, the pressure plate 20 overlies the die 12, and the spring 22 presses the pressure plate 20 and the die 12 against the interconnect 16.

Still referring to Figure 3, the clips 26, 28 attach to corresponding openings 30, 32 in the base 14 to secure the cover 24, spring 22, pressure plate 20, and die 12 to the package base 14. The clips 26, 28 can be formed of a flexible material such as spring steel, or plastic, and are shaped to exert a retention force on the cover 24. Furthermore, in the assembled package 10, the cover 24 is recessed below the top surface of the package base 14. The outer peripheral size and outline of the package 10 are thus substantially determined by the outer peripheral size and outline of the package base 14.

Still referring to Figure 3, the cover 24, spring 22 and pressure plate 20 all include a central opening which are designated 48C, 48S and 48P respectively. As will be further explained, the openings 48C, 48S and 48P are used during assembly and disassembly of the package 10. Specifically, the openings 48C, 48S and 48P permit the die 12 to be held by a vacuum tool (not shown) during optical alignment of the die 12 and interconnect 16 during assembly of the package 10. In a similar manner, a vacuum tool (not shown) can be used to disassemble the package 10.

The package 10 has a standard outline that is substantially equivalent to a conventional semiconductor package. In addition, the external contacts 38A-38C are formed with a standard size and spacing that are substantially equivalent to a conventional semiconductor package. As used herein, the term conventional semiconductor package refers to a plastic or ceramic package having an outline and external lead configuration that conforms to standards of a recognized industry standard setting body. These standard setting bodies can include:

EIA/JEDEC	-	Electronics Industry Association - Joint Electron Device Engineering Council
JEIDA	-	Japanese Electronics Industry Development Association
PCMCIA	-	Personal Computer Memory Card International Association

The standard outline and lead configuration permit the package 10 to be used with standardized burn-in equipment for a conventional package. By way of example, the standardized equipment can include an AMBYX$_{TM}$ intelligent burn-in and test system manufactured by Micron Systems Integration, Inc.

Referring to Figure 2, the external contacts 38A-38C for the package 10 are formed in a dense grid pattern on a bottom surface 31 of the base 14. As shown in Figure 2A, the external contacts 38A can be in the form of land pads arranged in a land grid array (LGA). Alternately, as shown in Figure 2B, the external contacts 38B can be in the form of pins arranged in a pin grid array (PGA). Alternately, as shown in Figure 2C, the external contacts 38C can be in the form of bumps arranged in a bumped grid array (BGA). The external contacts 38A-38C can also be arranged in a dense perimeter pattern (not shown) rather than a grid pattern.

In each of these cases the external contacts 38A-38C are in electrical communication with internal conductive lines 49 formed integrally with the package base 14. The internal conductive lines 49 are in electrical communication with the conductors 40 formed on the package base 14. As shown in Figure 3, the conductors 40 terminate at a bond shelf 42 and are wire bonded to the interconnect 16 using bond wires 44.

Referring to Figure 2A, the external contacts 38A in a land grid array can be formed as flat land pads out of a suitable metal or stack of metals. Exemplary metals can include gold, copper, silver, tungsten, tantalum, platinum

palladium and molybdenum or alloys of these metals. An exemplary stack can include a gold layer with nickel underplating. Other exemplary stacks can include other combinations of the above metals. A metallization process such as plating can be used to form the external contacts 38A as flat land pads. Such a plating process can include electrolytic or electroless deposition of a metal layer followed by resist coating, exposure, development, and selective wet chemical etching. Typically, the exposed surface of the external contacts 38A will be an electroplated metal such as gold.

By way of example, a diameter of the external contacts 38A can be from about 50μm to 500μm. A center line to center line spacing of the external contacts 38A can be from about 50μm to 500μm. A representative thickness for the external contacts 38A can be from 1.25μm to 100μm. The external contacts 38A are adapted to be contacted by a mating electrical connector on a burn-in board such as a pogo pin, solder ball, or other connector in electrical communication with external test circuitry.

As shown in Figure 2B, the external contacts 38B can be formed using the same process as outlined above for external contacts 38A, but with a pin brazed or soldered to the flat land pads. As shown in Figure 2C, the external contacts 38C can be formed using the same process as outlined above for external contacts 38A, but with a solder paste screen printed onto the flat land pads, heated and then reflowed into a ball.

As used herein the term "dense grid pattern" refers to a contact pattern in which the density of the contacts 38A-38C is high in relation to the total area occupied by the contacts. This relationship is sometimes expressed as a "packing fraction". In general, the packing fraction of a pattern of contacts is the area occupied by the contacts over

the total area available. For example, contacts formed in a grid pattern of one hundred and forty four one inch square blocks in an area twelve inches by twelve inches would yield a packing fraction of one. A pattern of one hundred and forty four one inch diameter round contacts in a grid of one hundred forty four one inch squares would yield a packing fraction of 0.7854. In actual practice packing fractions close to one are not possible because some spacing is required between the contacts in order to minimize shorting between adjacent contacts. For example, contacts formed as bumps (e.g., 38C-Figure 2C) require some spacing to prevent shorting during reflow. In general, a "dense grid pattern" will have a packing fraction of 0.25 or greater.

As shown in Figure 2D, the package base 14 can be a multi layer block formed of fired laminated ceramic layers 41A-41E such as alumina (Al_2O_3). Such a process is described in U.S. Patent Application Serial No. 08/398,309 filed March 1, 1995 which is incorporated herein by reference. Briefly, this process involves forming metallized circuits in the x, y and z planes. These circuits are formed on green sheets of ceramic using a suitable metallization process and are interconnected with metal filled vias. The green sheets are then pressed together and sintered at high temperatures to form a unitary structure. Using this process the conductors 40 and external contacts 38A-38C can be formed using suitable metals and then interconnected by forming internal conductive lines 49. In addition, as shown in Figures 2A-2C, the external contacts 38A-38C can be recessed below the outermost ceramic layer 41E.

The package base 14 can also be formed using a 3-D injection molding process out of a high temperature glass filled plastic such as a FR-4 material. Such a process is described in U.S. Patent No. 4,985,116 and in the above incorporated U.S. Patent Application Serial No. 08/398,309

Suitable plastics include polyetherimide (PEI), polyethersulfone (PES), polyarylsulfone (PAS), polyphenylene sulfide (PPS), liquid crystal polymer (LCP) and polyether-ether ketone (PPEK). An injection molding process with these or other suitable material can be used to form the package base 14 into the desired rectangular shape and with cavities as required. During a subsequent metallization process, various circuit patterns including the conductors 40 and external contacts 38A-38C can be formed on the package base 14 and can be interconnected by forming the internal conductive lines 49.

The package base 14 can also be formed using a ceramic dip formation process (Cerdip). In general, with a Cerdip process a mixture of alumina lubricants and binders can be molded and sintered to form the monolithic package base 14. A metal lead frame can then be bonded to the package base 14 using low temperature glasses to form the conductors 40. The external contacts 38A-38C can be part of the lead frame or can be formed separately. Another type of ceramic dip formation process uses a plastic rather than a ceramic body. Briefly, this Cerdip formation process pre-molds a plastic base which is then bonded to a leadframe. Conventional semiconductor packages formed using this process are sold by GTE Products Corporation, Warren, Pennsylvania under the trademark QUAD-PACK$_{TM}$.

Figure 3A illustrates an alternate embodiment package 10A. The alternate embodiment package 10A includes substantially the same elements as previously explained for package 10 which are denoted with an "A" suffix. However, in the alternate embodiment package 10A, the spring 22A is formed as a flat member and the pressure plate 20 (Figure 3) is eliminated. By way of example, the spring 22A can be a flat metal spring (e.g., wave spring) or can be formed of a

resilient elastomeric material such as a silicone elastomer or polyimide material.

In addition, in the alternate embodiment package 10A, the cover 24A includes a recess 50 which encloses the spring 22A and die 12. The cover 24A abuts a bottom surface of the recess 36A in the package base 14A and is retained by a pair of sliding clips 26A, 28A. The sliding clips 26A, 28A are slidably mounted to the base 14A and are formed in an S-shape to exert a retention force on the cover 24A.

Referring to Figure 4, the interconnect 16 for the package 10 is shown separately. The interconnect 16 includes bonding pads 56 that are wire bonded to the conductors 40 formed in the package base 14. The interconnect 16 also includes conductive traces 58 and raised contact members 60. As shown in Figure 5, the raised contact members 60 are adapted to contact and establish an electrical connection with the device bond pads 62 or other contact locations on the die 12. In addition, the raised contact members 60 include penetrating projections 70 formed as elongated blades adapted to penetrate the device bond pads 62 to a self limiting penetration depth.

The interconnect 16 and raised contact members 60 can be formed by etching a silicon substrate 64. An insulating layer 66 and a conductive layer 68 formed on the substrate 64 overlie the raised contact members 60. The conductive layer 68 is in electrical communication with the conductive traces 58 which are wire bonded to bond wires 44. Alternately, in place of wire bonding, an electrical connection can be formed to the conductive traces 58 with slide contacts 44S.

A suitable process for forming the contact members 60 substantially as shown is disclosed in U.S. Patent No. 5,326,428 and U.S. Patent No. 5,419,807 which are incorporated herein by reference. Another suitable process

is disclosed in U.S. Patent Application Serial No. 08/335,267 filed November 7, 1994, incorporated herein by reference.

With reference Figure 5A, the interconnect 16 can also be formed with microbump contact members 60B and conductive traces 58B formed on a plastic film 72. The microbump contact members 60B and plastic film 72 can be similar to two layer TAB tape such as ASMAT manufactured by Nitto Denko. The plastic film 72 can be mounted to a substrate 64B such as silicon using a compliant adhesive layer 74. The compliant adhesive layer can be formed of a silicone elastomer, an epoxy or a polyimide material. One method for forming an interconnect with microbump contact members is described in previously cited U.S. Patent Application Serial No. 08/398,309.

Referring again to Figure 1, the package 10 can be assembled using optical alignment techniques and aligner bonder tools used for flip chip bonding semiconductor dice. Flip chip bonding refers to a process wherein a semiconductor die is placed face down on a substrate, such as a printed circuit board, and the bond pads on the die are bonded to connection points on the substrate. Tools for flip chip bonding are sometimes referred to as aligner bonders. An aligner bonder and method of optical alignment for flip chip bonding are described in U.S. Patent No. 4,899,921 to Bendat et al, entitled "Aligner Bonder". Such an aligner bonder is available from Research Devices of Piscataway, N.J.

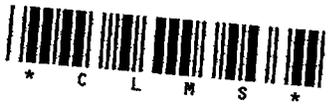
In the present case, an aligner bonder may be modified to provide an assembly apparatus for use in assembling the package 10. The assembly apparatus includes an assembly tool (not shown) that is adapted to retain the force applying mechanism 18 (Figure 1), die 12 and clips 26, 28 (Figure 3). The components of the force applying mechanism 18 include openings 48C, 48S, 48P which allow a vacuum wand (not shown) of the assembly tool to hold the die 12. With the die 12

held by the assembly tool, the bond pads 62 (Figure 5) on the die 12 are aligned with the contact members 60 (Figure 5) on the interconnect 16. The assembly tool then places the die 12 in contact with the interconnect 16 and secures the clips 26, 28 (Figure 3) to the openings 30, 32 in the package base 14.

U. S. Patent Application No. 08/338,345 filed November 14, 1994, incorporated herein by reference, describes an automated apparatus suitable for optically aligning the die 12 and interconnect 16 and securing the force applying mechanism 18 to the package base 14.

Following the assembly procedure the package 10 can be used to test the die 16. Testing can include full functionality as well as burn-in testing. Following the test procedure, the package 10 can be disassembled using an assembly tool (not shown) to remove the clips 26, 28 and force distribution mechanism 18 substantially as previously described for the assembly procedure.

While the invention has been described with reference to certain preferred embodiments, as will be apparent to those skilled in the art, certain changes and modifications can be made without departing from the scope of the invention as defined by the following claims.



WHAT IS CLAIMED IS:

1. A temporary package for a semiconductor die, comprising:

a base for retaining the die, said base including a plurality of external contacts formed on a surface of the base in a dense array;

an interconnect mountable to the base, said interconnect having contact members for electrically contacting contact locations on the die; and

an electrical path formed between the contact members on the interconnect and the external contacts on the base.

2. The package as claimed in claim 1 and wherein the dense array is selected from the group consisting of land grid array (LGA), pin grid array (PGA), ball grid array (BGA) and perimeter array.

3. The package as claimed in claim 1 and wherein the base is formed with an outline corresponding to a conventional semiconductor package.

4. The package as claimed in claim 1 and wherein the base is formed by a process selected from the group consisting of ceramic lamination, 3-D molding and ceramic dip formation.

5. The package as claimed in claim 1 and wherein the electrical path includes wire bonding conductive traces formed on the interconnect to conductors formed on the base in electrical communication with the external contacts.

6. A temporary package for a semiconductor die, comprising:

a base for retaining the die, said base having internal conductive traces in electrical communication with a pattern of external contacts formed in a dense grid array selected from the group consisting of land grid array (LGA), pin grid array (PGA) and ball grid array (BGA);

an interconnect mountable to the base, said interconnect having contact members for electrically contacting contact locations on the die; and

a conductive path formed between the contact members on the interconnect and the external contacts on the base.

7. The package as claimed in claim 6 and wherein the package base has an outline substantially equivalent to a conventional semiconductor package.

8. The package as claimed in claim 6 and wherein the conductive path is formed by forming conductors on the base in electrical communication with the internal conductive traces and wire bonding the conductors to conductive traces formed on the interconnect in electrical communication with the contact members.

9. The package as claimed in claim 6 and wherein the base is formed using a lamination process in which greensheets of ceramic material are bonded using a sintering process.

10. The package as claimed in claim 6 and wherein the base is formed using a 3-D molding process out of a glass filled plastic.

11. The package as claimed in claim 6 and wherein the base is formed using a ceramic dip formation process.

12. The package as claimed in claim 6 and wherein the external contacts are formed with a diameter between 50 m to 500 m and with a pitch between 50 m to 500 m.

13. The package as claimed in claim 6 and wherein the external contacts are formed in the dense grid array with a packing fraction of at least 0.25.

14. The apparatus as claimed in claim 6 and wherein the external contacts are formed of as flat land pads.

15. The apparatus as claimed in claim 6 and wherein the external contacts are formed as pins attached to flat land pads.

16. The apparatus as claimed in claim 6 and wherein the external contacts are formed as solder bumps formed on flat land pads.

17. A temporary package for a semiconductor die comprising:

a package base for mounting the die, said package base including a pattern of conductors in electrical communication with a pattern of external contacts formed in a dense grid array, said package base and external contacts formed with a size and shape corresponding to a conventional semiconductor package;

an interconnect mounted to the base and including a pattern of contact members in electrical communication with the pattern of conductors;

a force applying mechanism for retaining the die within the cavity in electrical communication with the interconnect; and

a latching mechanism for securing the force applying mechanism to the base.

18. The package as claimed in claim 17 and wherein the dense grid array is selected from the group consisting of land grid array (LGA), ball grid array (BGA) and pin grid array (PGA).

19. The package as claimed in claim 17 and wherein the interconnect includes raised silicon contact members having elongated penetrating projections formed on a silicon substrate.

20. The package as claimed in claim 17 and wherein the interconnect includes microbump contact members mounted on a substrate using a compliant adhesive layer.

21. The package as claimed in claim 17 and wherein the package base is formed of a material selected from the group consisting of plastic and ceramic.

22. The package as claimed in claim 17 and wherein the package base is formed by a process selected from the group consisting of ceramic lamination, 3-D molding, and ceramic dip process (Cerdip).

23. The package as claimed in claim 17 and wherein the force applying mechanism includes a spring and a cover.

24. The package as claimed in claim 17 and wherein the spring is formed of an elastomeric material.

25. The package as claimed in claim 17 and wherein the latching mechanism includes clips that removably attach to the package base.

26. The package as claimed in claim 17 and wherein the external contacts in the dense grid array have a packing fraction of at least 0.25.

Abstract

A temporary package for a semiconductor die is provided. The temporary package has an outline and external contact configuration that are the same as a conventional plastic or ceramic semiconductor package. The temporary package can be used for burn-in testing of the die using standard equipment. The die can then be removed from the package and certified as a known good die. The package includes a base, an interconnect and a force applying mechanism. The package base includes external contacts formed in a dense array, such as a land grid array (LGA), a pin grid array (PGA), a bumped grid array (BGA) or a perimeter array. The package base can be formed of ceramic or plastic with internal conductive lines using a ceramic lamination process, a 3-D molding process or a Cerdip formation process.

Figure 1

THIS SHEET HAS BEEN REPLACED

This Sheet Has Been Replaced



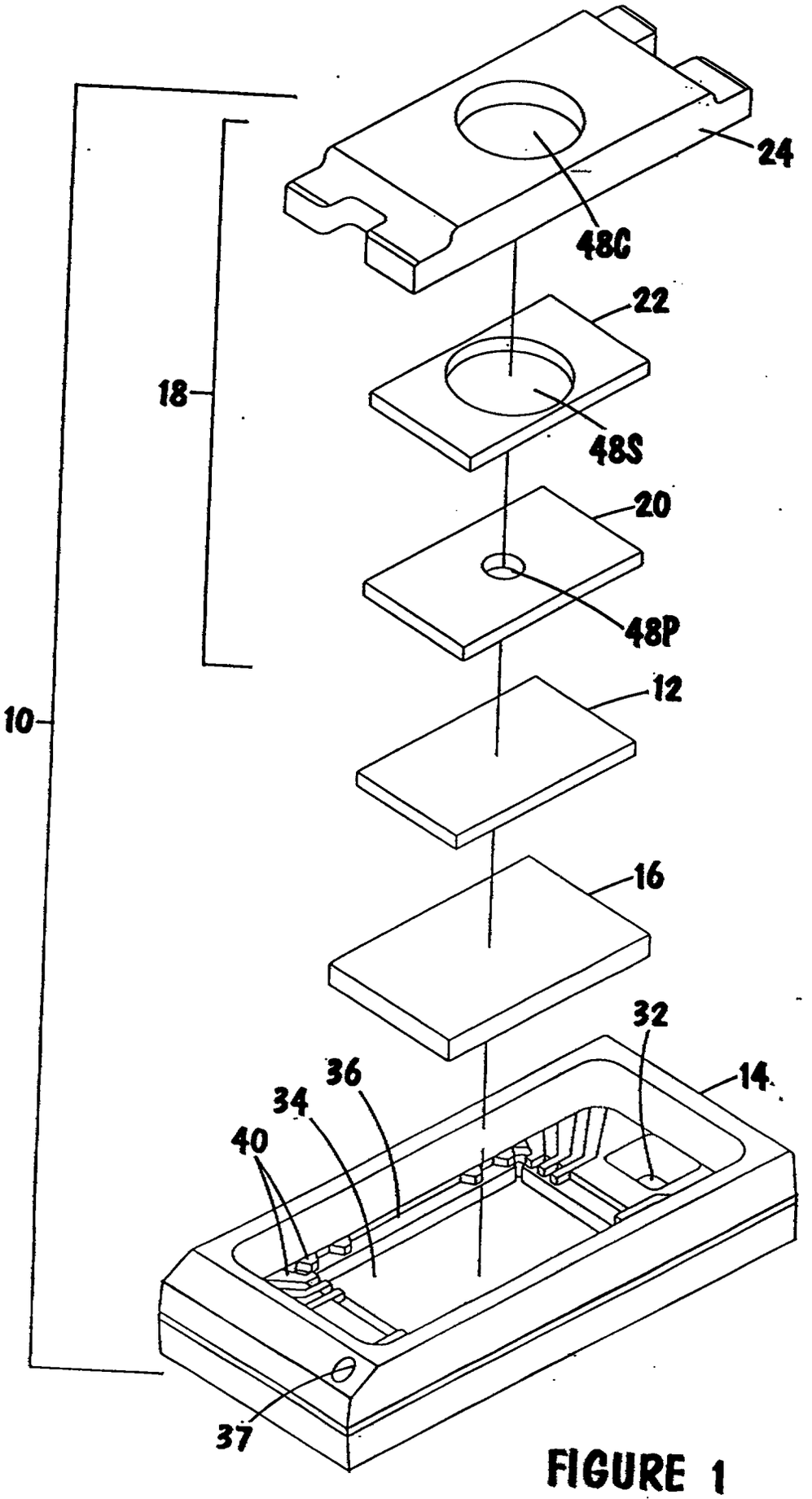


FIGURE 1

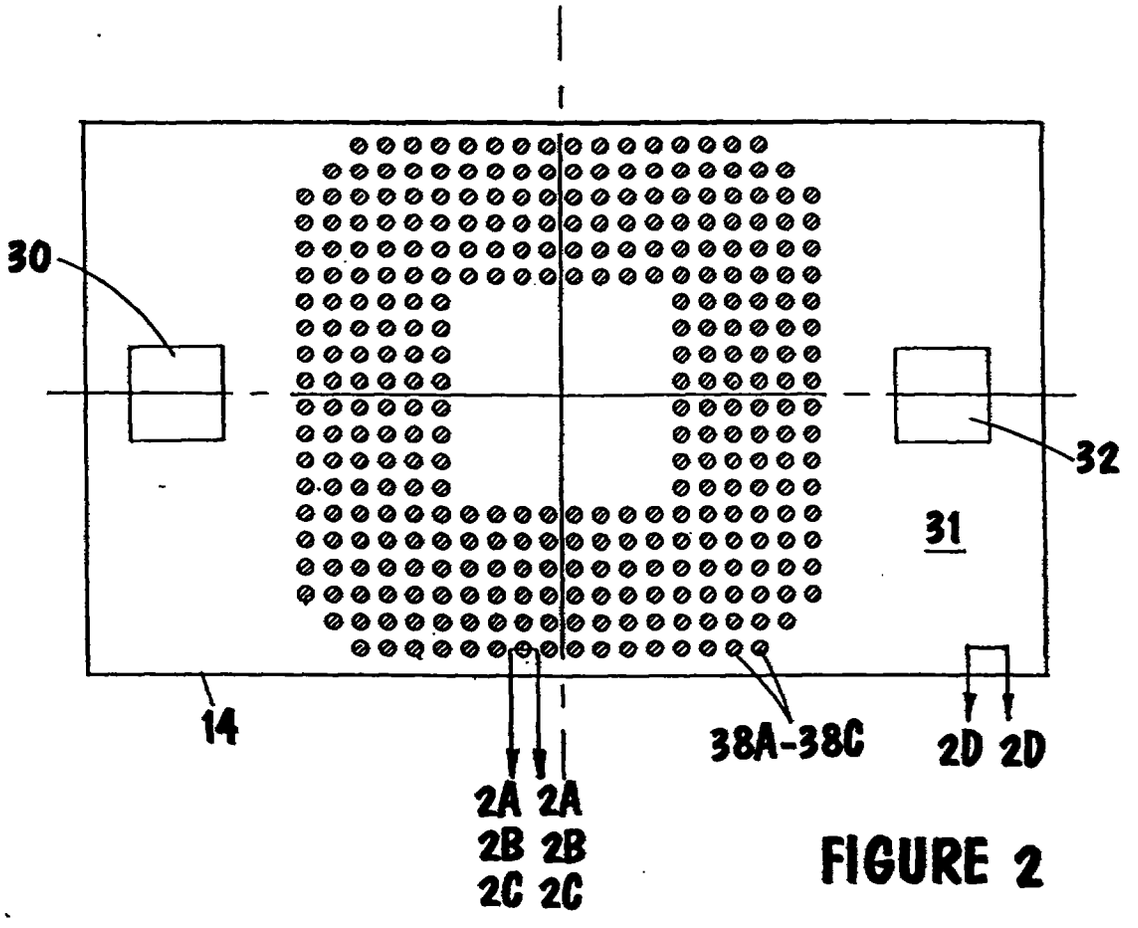


FIGURE 2

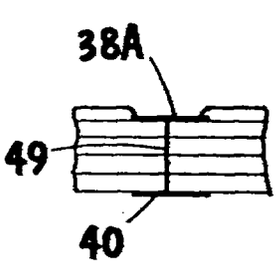


FIGURE 2A

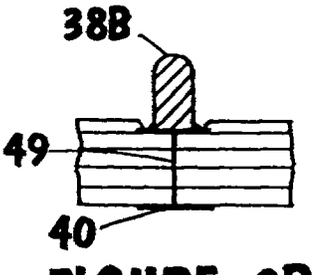


FIGURE 2B

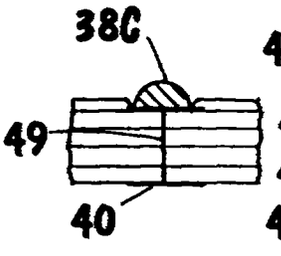


FIGURE 2C

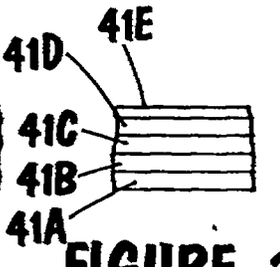


FIGURE 2D

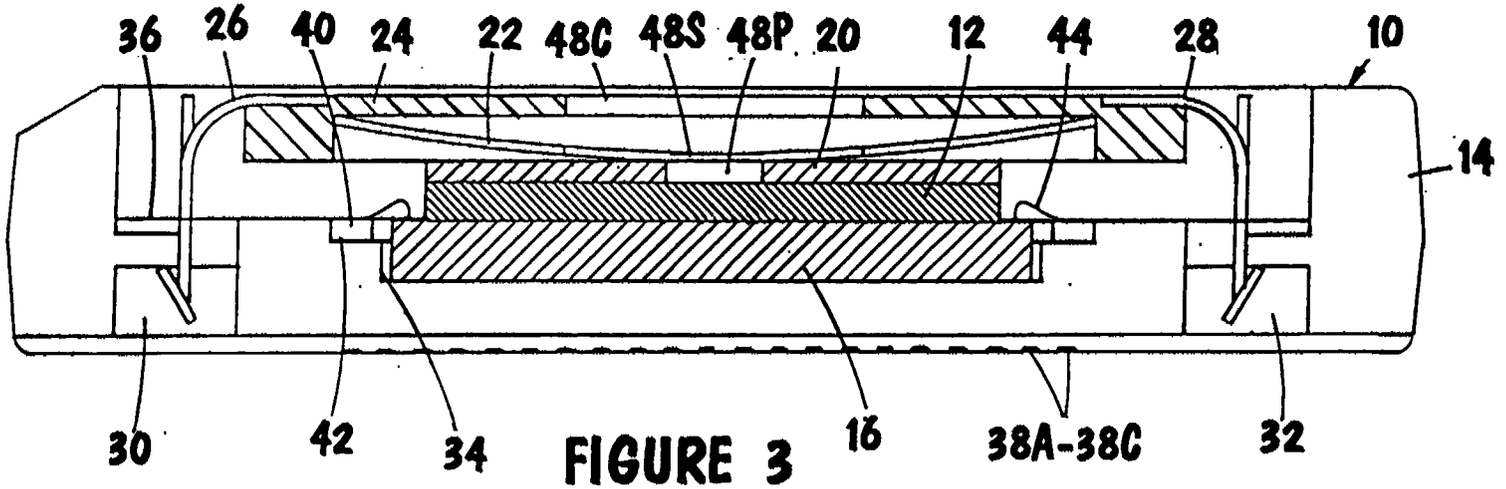


FIGURE 3

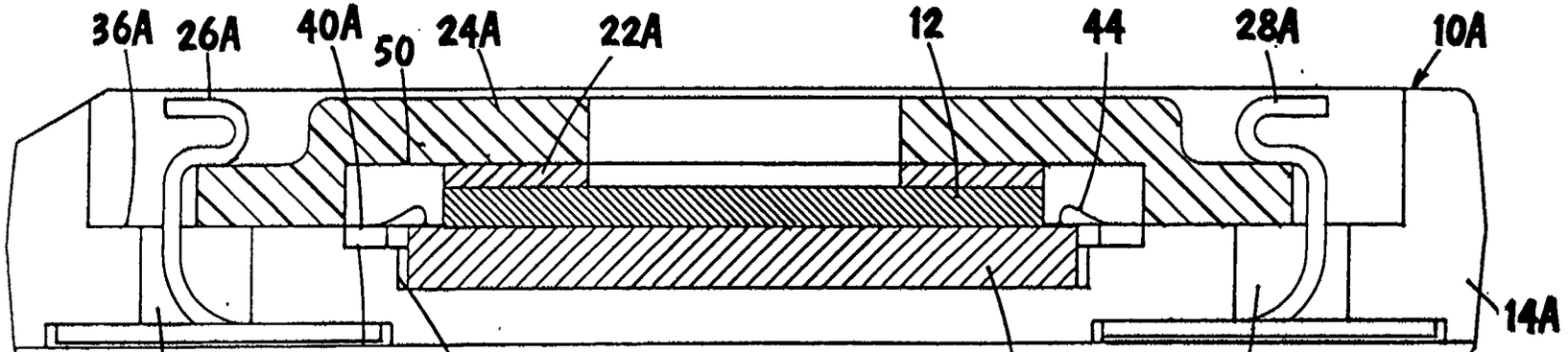


FIGURE 3A

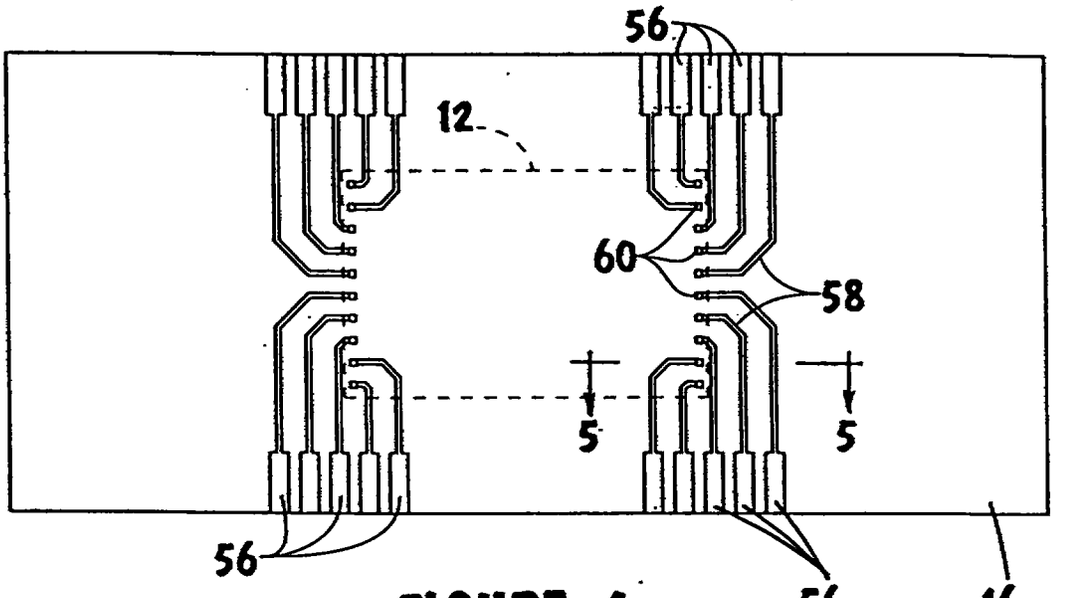


FIGURE 4

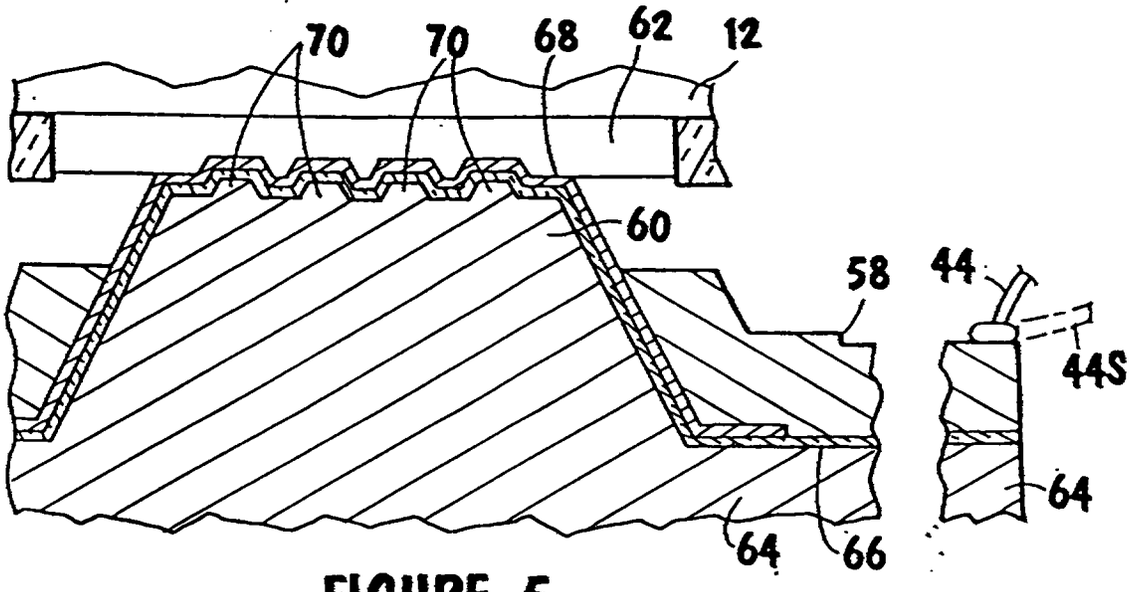


FIGURE 5

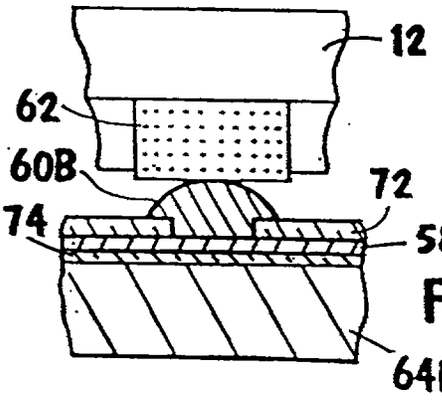


FIGURE 5A

TEMPORARY SEMICONDUCTOR PACKAGE HAVING DENSE ARRAY EXTERNAL CONTACTS

Abstract

A temporary package for a semiconductor die is provided. The temporary package has an outline and external contact configuration that are the same as a conventional plastic or ceramic semiconductor package. The temporary package can be used for burn-in testing of the die using standard equipment. The die can then be removed from the package and certified as a known good die. The package includes a base, an interconnect and a force applying mechanism. The package base includes external contacts formed in a dense array, such as a land grid array (LGA), a pin grid array (PGA), a bumped grid array (BGA) or a perimeter array. The package base can be formed of ceramic or plastic with internal conductive lines using a ceramic lamination process, a 3-D molding process or a Cerdip formation process.

Figure 1

REPLACEMENT SHEET
08 MAR 1997