What is Claimed is:

1. A semiconductor device, comprising:

a gate electrode structure disposed on a substrate;

a capping structure covering an upper surface of the gate electrode structure, the capping structure comprising:

a capping pattern; and

a first etch stop pattern covering a lower surface and a sidewall of the capping pattern;

an alignment key disposed on the substrate, the alignment key including an insulating material; and

a filling structure disposed on the substrate, the filling structure covering a sidewall of the alignment key, and the filling structure comprising:

a first filling pattern;

a second filling pattern covering a lower surface and a sidewall of the first filling pattern; and

a second etch stop pattern covering a lower surface and a sidewall of the second filling pattern, the second etch stop pattern containing a material having a higher etching selectivity than that of the insulating material of the alignment key.

2. The semiconductor device of claim 1, wherein the capping pattern and the second filling pattern include a same material, and the first etch stop pattern and the second etch stop pattern include a same material.

3. The semiconductor device of claim 2, wherein the capping pattern and the second filling pattern include silicon oxycarbide (SiOC), and the first etch stop pattern and the second etch stop pattern include silicon nitride (SiN), silicon oxynitride (SiON) or silicon carbonitride (SiCN).

4. The semiconductor device of any one of claims 1 to 3, wherein the alignment key and the first filling pattern include an oxide.

5. The semiconductor device of any one of claims 1 to 4, wherein a width of the filling structure is greater than a width of the capping structure.

6. The semiconductor device of any one of claims 1 to 5, wherein a lower surface of the filling structure is lower than a lower surface of the alignment key.

7. The semiconductor device of any one of claims 1 to 6, further comprising:

a gate spacer covering a sidewall of the gate electrode structure,

wherein the capping structure covers the upper surface of the gate electrode structure and an upper surface of the gate spacer.

8. The semiconductor device of any one of claims 1 to 7, further comprising:

a first contact plug extending through the capping structure to contact the upper surface of the gate electrode structure.

9. The semiconductor device of any one of claims 1 to 8, wherein the gate electrode structure is formed on an active fin protruding from an upper surface of the substrate, and

wherein the semiconductor device further comprises:

a source/drain layer on the active fin, the active fin adjacent to the gate electrode structure; and

a second contact plug contacting an upper surface of the source/drain layer.

10. The semiconductor device of claim 9, wherein the gate electrode structure comprises an interface pattern, a gate insulation pattern, a work function control pattern and a gate electrode sequentially stacked on an upper surface of the active fin.

11. A semiconductor device, comprising:

a conductive structure disposed on a substrate;

a capping structure covering an upper surface of the conductive structure, the capping structure comprising:

a capping pattern containing silicon oxycarbide (SiOC); and

a first etch stop pattern covering a lower surface and a sidewall of the capping pattern, the first etch stop pattern containing a material, which has a first etching selectivity with respect to the capping pattern;

an alignment key on the substrate, the alignment key containing a material having a second etching selectivity lower than the first etching selectivity with respect to the capping pattern; and

a filling structure disposed on the substrate, the filling structure covering a sidewall of the alignment key, and the filling structure comprising:

a first filling pattern;

a second filling pattern covering a lower surface and a sidewall of the first filling pattern, the second filling pattern and the capping pattern containing a same material; and

a second etch stop pattern covering a lower surface and a sidewall of the second filling pattern, the first etch stop pattern and the second etch stop pattern containing a same material.

12. The semiconductor device of claim 11, wherein the first etch stop pattern and the second etch stop pattern include silicon nitride (SiN), silicon oxynitride (SiON) or silicon carbonitride (SiCN).

13. The semiconductor device of claim 11 or claim 12, wherein the alignment key and the first filling pattern include an oxide.

14. The semiconductor device of any one of claims 11 to 13, wherein a width of the filling structure is greater than a width of the capping structure.

15. The semiconductor device of any one of claims 11 to 14, wherein a lower surface of the filling structure is lower than a lower surface of the alignment key.

16. A semiconductor device, comprising:

an active region disposed on a substrate, the active region defined by an isolation pattern on the substrate;

a gate electrode structure disposed on the active region and the isolation pattern;

a capping structure covering an upper surface of the gate electrode structure, the capping structure comprising:

a capping pattern containing silicon oxycarbide (SiOC); and

an etch stop pattern covering a lower surface and a sidewall of the capping pattern, the etch stop pattern containing a material, the material comprising silicon nitride (SiN), silicon oxynitride (SiON) or silicon carbonitride (SiCN); and

a source/drain layer on the active region adjacent to the gate electrode structure.

17. The semiconductor device of claim 16, further comprising:

a gate spacer covering a sidewall of the gate electrode structure,

wherein the capping structure covers the upper surface of the gate electrode structure and an upper surface of the gate spacer.

18. The semiconductor device of claim 16 or claim 17, further comprising:

a first contact plug extending through the capping structure to contact the upper surface of the gate electrode structure; and

a second contact plug contacting an upper surface of the source/drain layer.

19. The semiconductor device of any one of claims 16 to 18, wherein the active region includes:

an active fin protruding from an upper surface of the substrate, the active fin having an upper surface higher than an upper surface of the isolation pattern.

20. The semiconductor device of claim 19, wherein the gate electrode structure includes an interface pattern, a gate insulation pattern, a work function control pattern and a gate electrode sequentially stacked on the upper surface of the active fin.