

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO DIGITAL ELECTRONIC ALARM TIMEPIECES

5 (71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company, of 31-1, 6-chome, Kaneido, Koto-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to digital electronic alarm timepieces. Although applicable to such timepieces generally, the invention is particularly advantageously applicable to digital alarm wristwatches.

15 In digital electronic alarm timepieces as at present in general use a sound emitting alarm device incorporated in the timepiece sounds the alarm only when a pre-set alarm time and the time as kept by the timepiece correspond with each other. This however
20 has a practical disadvantage that the alarm sound given by different timepieces of similar general design may differ from one timepiece to another quite substantially and, because the only way in which a
25 would-be customer or user can be enabled to hear the sound of the alarm of a particular timepiece is to pre-set the alarm to a chosen time and wait until that time is reached, it is a tedious and time consuming matter for him to listen to the alarm sounds of several timepieces in order to choose the one whose sound he likes best. A similar defect arises in the case of a timepiece having an alarm device the sound of which
35 is adjustable, for it is again a tedious and time consuming matter to adjust the sound to obtain the result which best pleases the user, since each time he wishes the alarm to be sounded he has to set an alarm time and wait until that time is reached.

40 According to this invention there is provided a digital electronic alarm timepiece including time signal generating means, digital time display means, at least one alarm time memory circuit, an alarm device, means for causing operation of said alarm device when an alarm time pre-set in said memory circuit coincides with the time as kept by the timepiece and means,

operable at will at any moment for causing operation of said alarm device without presetting the alarm time to coincide with that moment. 50

Preferably the foregoing last mentioned means comprise one or a combination of switches provided for other purposes in the timepiece, said one switch or combination of switches being arranged to cause the alarm to be sounded if actuated in accordance with a selection other than a selection made when used for any of said other purposes. 55 60

In one embodiment of the invention the timepiece includes time counting means having counters for different time units, at least one alarm time memory circuit having counters for different time units, a display device controlled by a display selecting switching circuit, a multi-output shift register for controlling said switching circuit to determine whether said display device displays the contents of the time counter or the contents of an alarm time memory circuit in dependence upon selection of an output from said register, switch means for controlling said register to select an output thereof, a second multi-output shift register for selecting between different time units upon selection of an output thereof, switch means for controlling said second register to select an output, a coincidence detector for detecting coincidence between the contents of the time counting means and the contents of an alarm memory circuit, and means for actuating the alarm device upon occurrence of such coincidence. 65 70 75 80 85

The invention is illustrated in and further explained in connection with the accompanying drawings in which: 90

Figure 1 is a simplified diagram of one embodiment; and

Figure 2 is a graphical explanatory time chart diagram.

Referring to Figure 1 a time standard quartz crystal controlled oscillator 1 produces relatively high frequency oscillations which are fed to a time counter 95

2 which produces therefrom suitable time unit signals for controlling a digital time display device, e.g. signals at second, minute, hour and day intervals. 5 is a control switch unit comprising four manually operable switches 5a, 5b, 5c and 5d which are respectively a safety switch, a set switch, a mode switch and a select switch. Each of these switches has one terminal connected to the positive terminal V_{DD} of a supply potential source, the remaining terminal of each switch being connected to the input of a respective anti-chatter circuit 6a, 6b, 6c, 6d, for eliminating switch chatter produced by contact bounce or similar undesired switch action when a switch is operated. These anti-chatter circuits are shown in the block 6. In the block 7 are shown four circuits 7a, 7b, 7c and 7d respectively connected to the outputs of the circuits 6a, 6b, 6c and 6d. Of these four circuits each of the circuits 7b, 7c and 7d produces a pulse of predetermined fixed pulse width when the switch 5b, 5c or 5d with which it is associated, is closed. When the switch 5a is closed, the output terminal of circuit 7a assumes and maintains the potential at the positive terminal of the source connected at V_{DD} ; and when said switch is open said output terminal is maintained at the potential of the negative terminal of said source.

The output of the circuits 7a and 7b are connected respectively to the inputs of an AND gate 8 and the outputs of the circuits 7a and 7d are connected respectively to the inputs of an AND gate 9. The output of the circuit 7c is connected to the input of a channel selecting shift register 11 having three outputs W, M1 and M2. There are four groups 12, 13, 14 and 15 of AND gates. The output from AND gate 8 is connected to one input terminal of each of the AND gates 12a, 12b and 12c in group 12 and to one input of AND gate 13a in the group 13, one input of AND gate 14a in the group 14 and to one input of AND gate 15a in the group 15.

The output from AND gate 9 is connected to a time unit selecting shift register 10 having three selectable outputs namely a day output, an hour output and a minute output. Selection of these outputs is effected in dependence on the number of input pulses fed in to the shift register 10. These three outputs of the shift register 10 are respectively connected to the remaining inputs of the AND gates 12a, 12b and 12c in the group 12. The output of AND gate 12a is connected to one input of AND gate 13b; the output of AND gate 12b is connected to one input of each of the AND gates 13c, 14b and 15b; and the output of AND gate 12c is connected to one input of each of the

AND gates 13d, 14c and 15c. The remaining input of the AND gates in the group 13 are connected to the W output of the shift register 11; the remaining inputs of the AND gates in the group 14 are connected to the M1 output of said register 11; and the remaining inputs of the AND gates 15 are connected to the M2 output of said register 11.

The shift register 11 generates signals at its outputs W, M1, M2 in turn in accordance with the number of output pulses from circuit 7c and the said shift register outputs are respectively connected to the three inputs of a discriminating circuit 23 which discriminates between them. The output from said discriminating circuit 23 is fed to one input of a display change-over switching circuit 16 which serves to select between the three possible displays namely a display of normal time (when shift register 11 provides an output at its terminal W), a display of a first alarm time memory content (when shift register 11 provides an output at its terminal M1) or a display of a second alarm time memory content (when shift register 11 provides an output at its terminal M2).

The outputs of the four AND gates in the group 13 are respectively connected to the four inputs of a time counter 2 which, in the present example, counts days, hours, minutes and seconds. There are two alarm memory counters 3 and 4 which may, for convenience, be designated the M1 and M2 counters. Each of these has counters for days, hours and minutes. The outputs of the AND gates in the group 14 are respectively connected to the inputs of the M1 counter 3 and the outputs of the AND gates in the group 15 are respectively connected to the inputs of the M2 counter 4.

The contents of the three counters 2, 3 and 4 are respectively fed to the three remaining inputs of the display change-over switching circuit 16 and are also respectively fed to the three inputs of a coincidence detecting circuit 19 which produces an output signal on the occurrence of equality between the count content of counter 2 and the count content of counter 3 or of counter 4. As will be seen the content of one of the counters 2, 3 and 4 can be selected for display by the display change-over switching circuit 16 (under the control of the discriminating circuit 23) and fed to a decoder-driver 17 for display by a digital display device 18.

When a coincidence signal output is produced by the coincidence detecting circuit 19 this is applied to one input of an OR gate 20 and the output of this gate actuates an alarm driver 21 which thus causes an alarm to be sounded by the alarm device 22.

(11)

The output of the circuit 7a is also connected to an inverted input terminal of an AND gate 24, having two other normal input terminals and the outputs of the circuits 7b and 7d are respectively connected to these normal input terminals of AND gate 24.

The operation of Figure 1 will now be described.

When the switch 5c alone is closed, the circuit 7c produces an output pulse of fixed predetermined width, and when said switch 5c is operated the channel selecting shift register 11 which selects whether the contents of the time counter 2 or of the M1 counter 3 or of the M2 counter 4, are to be displayed by the display device 18, produces a "1" at each of its outputs W, M1 and M2 in turn in response to successive pulses from the circuit 7c. The successive outputs from the shift register 11 are fed to the discriminating circuit 23 which distinguishes between them and provides an output which controls the display change-over switching circuit 16 which accordingly causes the display device 18 to display the contents of the counter 2 or 3 or 4 according as to whether there is a "1" signal at the output W, M1 or M2 respectively of the shift register 11.

The operation of resetting the time counter 2 to zero will now be described. For this operation the switch 5a is closed to cause the output of the circuit 7a to maintain a "1" level. The switch 5c is then closed for the number of times to cause the contents of the time counter 2 to be displayed.

The switch 5b is then pushed and each time this happens a pulse of the predetermined fixed width appears at the output of the circuit 7b.

When time is displayed, the output W of the shift register 11 is a "1" and the outputs M1 and M2 of this register are both "0". Accordingly, the AND gates in the groups 14 and 15 are OFF and the AND gate 13a in the group 13 is conductive to pass a resetting pulse to reset to zero the seconds counter of the time counter 2.

Because the AND gate 9 is OFF all three outputs of the shift register 10 are at "0" level, the outputs of the three AND gates in the group 12 are at "0" and the AND gates 13b, 13c, 13d are accordingly OFF.

The operation of resetting to zero the alarm memory counters 3 or 4, will now be described. This is done by closing the switch 5b after selecting the desired channel by closing the switch 5c the required number of times. In the case of resetting the counter 4 the output terminal M2 of register 11 is selected and a pulsed signal which resets counter 4 appears at the

output of gate 15a. In the case of resetting counter 3, the register terminal selected is terminal M1 and a pulsed signal to reset counter 3 appears at the output of gate 14a. Thus either the memory counter 3 or 4 can be reset and, in either case, an alarm is sounded by a signal fed to alarm driver 21 via OR gate 20 and OR gate 27 and OR gate 25 (in the case of counter 3) or OR gate 26 (in the case of counter 24).

The time correcting operation will now be described. The switch 5a is closed thus making the output of circuit 7a of "1" level. The time unit required to be corrected is selected by pushing the switch 5d the required number of times. If it is required to correct the day counter incorporated in the time counter system 2, the switch 5d is closed once only, whereby one pulse signal appears at the output of the circuit 7d. This opens the AND gate 9 and only the "day" output terminal D of shift register 10 assumes a "1" level, the "hour" and "minute" outputs of this register remaining at "0". Now closure of the switch 5b will produce an output pulse from circuit 7b and this is passed through AND gate 8 to AND gate 12a which is the only gate in the group 12 having its output at level "1". Because at this time only the output W of register 11 is at level "1" only the AND gates 13a and 13b in the group 13 can produce an output pulse. It should be pointed out, however, that if day, hour and minute correcting signals are applied fed to the time counter 2, only the day figure will be corrected if a second reset is arranged to be ineffective in spite of its application. The day collecting signals from AND gates 13a and 13b also actuate the alarm driver 21 via OR gates 24, 27 and 20 and sound the alarm. The hour and minute outputs of the time unit selecting shift register are referenced H and M.

Similarly, in the case of hour and minute correction channel selection is achieved by a suitable number of closures of the switch 5d and a pulse is fed to AND gate 8 at each closure of 5b. In the case of minutes correction pulses are produced at the output of AND gate 12c and in the case of hours correction pulses are produced at the output of AND gate 12b. Pulses are thus produced at the outputs of gates 13a and 13c in hours correction or at the outputs of gates 13a and 13d for minute correction. If the seconds reset signal is arranged to be inoperative, only hours or minutes correcting signals will be effective. Again the hours and minutes correcting pulse signals actuate the alarm driver 21 via OR gates 24, 27 and 20.

Alarm times can be seen in a similar way.

If the M1 or M2 alarm time memory counter is selected by the shift register 11, a

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correcting pulse is produced from the output of the AND gates in the groups 14 or 15 respectively.

5 When a pre-set alarm time and normal time correspond with each other, the output from the coincidence detecting circuit 19 becomes of level "1" and this "1" signal actuates the alarm driver 21 through the OR gate 20 and an alarm is sounded by the alarm device 22. The alarm will however also be sounded if the switch 5a is OFF and the switches 5b and 5d are ON. What happens when the switch 5a is OFF and both the switches 5b and 5d are ON will now be described.

15 When switch 5a is moved to the OFF position, the output from the circuit 7a maintains level "0". When both switches 5b, 5d are moved to the ON position a "1" signal appears at the outputs of the circuits 7b and 7d. The output from the circuit 7a is connected to the inverting input of the AND gate 24 but the other outputs (from circuits 7b and 7d) are connected to the normal (non-inverting) inputs of the said gate 24. Therefore the output from said AND gate 24 becomes level "1" and actuates the driver 21 through the OR gate 20 and an alarm is sounded by the alarm device 22.

30 Figure 2 is a graphical timing chart which will assist in an understanding of the illustration in Figure 1. This figure will, it is thought, be found self-explanatory having regard to the foregoing description and the references in Figure 2. Line 7c shows pulses produced at the output of circuit 7c by operation of the switch 5c; lines 11W, 11M1 and 11M2 show pulses produced at the outputs W, M1 and M2 respectively of the shift register 11; line 9 shows pulses produced at the output of the AND gate 9; and lines 10D, 10H and 10M show pulses produced at the outputs D, H and M respectively of the shift register 10.

45 As will now be seen the timepiece described has the advantage of providing a relatively simple arrangement whereby, by easy and convenient switching operations, an alarm timepiece may be caused to sound its alarm at any time and at will without pre-setting an alarm time, so that a would-be customer can hear what the alarm sounds like, choose from several timepieces the one whose alarm sound he likes best or, in the case of a timepiece having an alarm device the sound of which is adjustable, the customer or user can use the facility of

causing the alarm to be sounded at will to enable the alarm sound to be adjusted to his best liking. A valuable advantage of the invention is that the foregoing facility of causing the alarm to sound at any time without having to provide any manually operable switches additional to those provided for other purposes.

Attention is directed to the specification of our co-pending Application No. 8798/77 (Serial No. 1,539,718).

WHAT WE CLAIM IS:—

1. A digital electronic alarm timepiece including time signal generating means, digital time display means, at least one alarm time memory circuit, an alarm device, means for causing operation of said alarm device when an alarm time pre-set in said memory circuit coincides with the time as kept by the timepiece and means, operable at will at any moment, for causing operation of said alarm device without presetting the alarm time to coincide with that moment.

2. A timepiece as claimed in Claim 1, wherein said last mentioned means comprise one or a combination of switches provided for other purposes in the timepiece, said one switch or combination of switches being arranged to cause the alarm to be sounded if actuated in accordance with a selection other than a selection made when used for any of said other purposes.

3. A timepiece as claimed in Claim 1 or 2 and including time counting means having counters for different time units, at least one alarm time memory circuit having counters for different time units, a display device controlled by a display selecting switching circuit, a multi-output shift register for controlling said switching circuit to determine whether said display device displays the contents of the time counter or the contents of an alarm time memory circuit in dependence upon selection of an output from said register, switch means for controlling said register to select an output thereof, a second multi-output shift register for selecting between different time units upon selection of an output thereof, switch means for controlling said second register to select an output, a coincidence detector for detecting coincidence between the contents of the time counting means and

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correcting pulse is produced from the output of the AND gates in the groups 14 or 15 respectively.

5 When a pre-set alarm time and normal time correspond with each other, the output from the coincidence detecting circuit 19 becomes of level "1" and this "1" signal actuates the alarm driver 21 through the OR gate 20 and an alarm is sounded by the alarm device 22. The alarm will
10 however also be sounded if the switch 5a is OFF and the switches 5b and 5d are ON. What happens when the switch 5a is OFF and both the switches 5b and 5d are ON will now be described.

15 When switch 5a is moved to the OFF position, the output from the circuit 7a maintains level "0". When both switches 5b, 5d are moved to the ON position a "1" signal appears at the outputs of the circuits 7b and 7d. The output from the circuit 7a is connected to the inverting input of the AND gate 24 but the other outputs (from circuits 7b and 7d) are connected to the normal
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55 the case of a timepiece having an alarm device the sound of which is adjustable, the customer or user can use the facility of

causing the alarm to be sounded at will to enable the alarm sound to be adjusted to his best liking. A valuable advantage of the invention is that the foregoing facility of causing the alarm to sound at any time without having to provide any manually operable switches additional to those provided for other purposes.

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2. A timepiece as claimed in Claim 1, wherein said last mentioned means comprise one or a combination of switches provided for other purposes in the timepiece, said one switch or combination of switches being arranged to cause the alarm to be sounded if actuated in accordance with a selection other than a selection made when used for any of said other purposes.

3. A timepiece as claimed in Claim 1 or 2 and including time counting means having counters for different time units, at least one alarm time memory circuit having counters for different time units, a display device controlled by a display selecting switching circuit, a multi-output shift register for controlling said switching circuit to determine whether said display device displays the contents of the time counter or the contents of an alarm time memory circuit in dependence upon selection of an output from said register, switch means for controlling said register to select an output thereof, a second multi-output shift register for selecting between different time units upon selection of an output thereof, switch means for controlling said second register to select an output, a coincidence detector for detecting coincidence between the contents of the time counting means and



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the contents of an alarm memory circuit, and means for actuating the alarm device upon occurrence of such coincidence.

5. 4. A digital electronic alarm timepiece substantially as herein described with reference to the accompanying drawings.

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