METHOD TO THIN A SILICON-ON-INSULATOR SUBSTRATE

The invention lies in the area of the fabrication of silicon-on-insulator substrates known to persons skilled in the art under the acronym "SOI".

A SOI substrate comprises a silicon oxide SiO_2 layer, buried between a silicon carrier substrate and a silicon surface layer called the “active layer” since it is on or in this layer that components will subsequently be fabricated intended for applications in the areas of electronics, optics, optoelectronics or microelectronics.

The present invention more specifically concerns a method to thin an initial substrate of SOI type, making it possible to obtain a SOI substrate having a silicon surface layer that is thin, even extra-thin, and whose surface is free or almost free of polluting particles.

The integration of transistors in microelectronics is made with increasingly smaller dimensions, since it is desired to increase the number of transistors packed on a wafer (or substrate). Breaking the “technological barrier of 22 nanometres”, i.e. fabricating transistors having a width of 22 nanometres or less, may lead to requiring the use of SOI substrates known to those skilled in the art as “fully depleted” substrates.

In said substrates, the silicon surface layer forms a so-called "depletion" layer in which the concentration of mobile charges is much lower than the equilibrium concentration.

The fabrication of a "fully depleted" transistor requires a reduction in the thickness of the active silicon surface layer, which on this account must be equal to or less than 50 nanometres, preferably in the order of 10 to 30 nanometres.

It is also to be noted that the thickness of the buried oxide layer can also be reduced i.e. to less than 15 nanometres, if it is desired to use this type of SOI substrate for the fabrication of components intended for applications of "low power" or "memory" type.

The thinner the desired active silicon surface layer, the more it is required to remove a substantial quantity of material from the initial SOI substrate.

When it is desired to thin the active silicon surface layer of the substrate, notably by etching, it is ascertained that the edges of the wafers are fragile, that they may break and form particles which are re-deposited on said active layer, thereby polluting this layer.

Also, with state of the art methods to fabricate SOI substrates, it is known to conduct treatment called Rapid Thermal Annealing (RTA). It is known that the effect of this treatment is to reduce the roughness of the silicon surface layer to achieve smoothing thereof.

It is also known from document FR-2 852 143 by the applicant, that RTA treatment can have the effect of overlapping and encapsulating the peripheral edge of the buried oxide layer of the SOI substrate, and that this encapsulation can prevent chemical attack and delamination of the edge of the buried oxide layer during a subsequent treatment step of the substrate.

Said RTA treatment is therefore routinely conducted during the finishing steps of a SOI substrate.

However, the applicant has found that when the active silicon layer is considerably thinned, the so-called "encapsulation" layer i.e. the layer facing the peripheral edge of the buried oxide, becomes damaged and no longer fulfils its protective role.

Appended figure 1, showing the state of the art, illustrates an encapsulation layer **CE** partly encapsulating the edge of a substrate SOI whose active silicon layer **CA** has a thickness of at least 100 nanometres. This encapsulation layer is consolidated by the onset of silicon bridges **PT** generated during RTA treatment.

The perspective diagram in figure 1A also shows the bridges **PT** and the oxide layer **OX** which can be seen at certain points between the bridges **PT**.

On the other hand, and as can be seen in appended figure 2 which illustrates a test result obtained by the applicant, if it is sought to further thin the active silicon layer **CA** of a substrate SOI, using a thermal oxidation process followed by an etching step, it is found that the bridges **PT** are either broken or have disappeared.

In this case, after said treatment, since the encapsulation layer is strongly damaged or has disappeared, the chemical product used for etching infiltrates the interface between the buried oxide layer and the surface silicon. The edge of the substrate lifts up and particles of silicon, and silicon together with oxide remnants, may break up and re-deposit on the active surface layer of the SOI substrate. Therefore substantial pollution of the substrate is observed, making it unfit for subsequent use in component fabrication. Additionally, the polluting particles may scratch the surface of the SOI substrate.

The person skilled in the art is therefore dissuaded from using etching to thin a SOI substrate, whether or not said substrate had undergone RTA treatment.

The objective of the invention is to solve the above-cited drawbacks of the prior art.

One particular objective of the invention is to provide a method allowing thinning of the active surface layer of an initial substrate of SOI type, whilst eliminating the particles generated by this thinning, whether or not this SOI substrate has been previously subjected to encapsulation treatment and/or to rapid thermal annealing of RTA type.

One particular objective of the invention is to provide said method with which it is possible to obtain a SOI substrate whose active silicon surface layer has a thickness of less than 50 nanometres and is of suitable quality for the subsequent fabrication of components.

For this purpose, the invention concerns a method to thin a silicon-on-insulator substrate SOI called the "initial substrate" comprising a silicon oxide layer SiO_2 buried between a silicon carrier substrate and a silicon surface layer.

According to the invention, this method comprises the following successive steps, consisting of conducting:

- thermal oxidation treatment of said initial substrate to cause oxidation of part of said silicon surface layer,
- a first cycle of etching then cleaning,
- a second cycle of etching then cleaning,

the etching of the first cycle being performed so as fully to remove the thermal oxide layer formed, to thin said silicon surface layer and to lift off all the unstable parts from the edge of said initial substrate, the etching of the second cycle being performed to

remove from the surface of said thinned substrate, the polluting particles formed during said first etching cycle and which have deposited thereupon, so as to obtain a so-called "final" silicon-on insulator-substrate SOI whose thinned surface layer forms an active layer.

According to other advantageous but non-limiting characteristics of the invention, take alone or in combination:

- the initial SOI substrate, before said thermal oxidation treatment, has undergone overlapping and encapsulation treatment of the peripheral edge of said buried silicon oxide layer SiO_2, with a so-called "encapsulation" layer derived from said surface layer, and the oxidation treatment of said initial substrate is conducted so as to cause oxidation of said lateral encapsulation layer over its entire depth as far as said buried silicon oxide SiO_2 layer;
- said overlapping and encapsulation treatment is conducted using rapid thermal annealing, RTA;
- the thermal oxidation treatment is conducted at a temperature of between 800°C and 1150°C;
- the different oxidation and etching steps are conducted so as to obtain a final silicon-on-insulator substrate whose so-called "extra-thin" active silicon layer has a thickness of 50 nm or less.
- the different oxidation and etching steps are conducted so as to obtain a final silicon-on-insulator substrate whose so-called "extra-thin" active silicon layer has a thickness of 30 nm or less;
- said initial silicon-on-insulator substrate SOI comprises a silicon surface layer whose thickness is 400 nm or less;
- the etching of the first and/or second cycle is performed using a pure hydrofluoric acid HF solution diluted in water to a concentration of between 10% and

50% by volume, at a temperature of between 20°C and 30°C for a time of between 30 seconds and 500 seconds;

- the etching of the first cycle is performed using a pure hydrofluoric acid solution HF diluted in water to a concentration of 10% by volume, it is applied at a temperature of between 20°C and 30°C for a time of between 100 s and 500 s, to remove 100 nm of silicon oxide;

- the cleaning of the first and/or second cycle is performed by immersing in water, then in a first bath of solution containing a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide H_2O_2) and deionized water, then in a second bath of solution containing a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and deionized water.

Other characteristics and advantages of the invention will become apparent from the following description given with reference to the appended drawings in which, in addition to figures 1 and 2 already described and depicting photos of observations under scanning electron microscopy of one edge of a SOI substrate, and figure 1A which is a schematic illustration of the SOI substrate in figure 1:

- figures 3 and 4 derive from observations made under scanning electron microscopy of the surface of the silicon surface layer of a thinned SOI substrate respectively at an intermediate stage of the method conforming to the invention and at the final stage;

- and figures 5A to 5F are schematics illustrating the different steps of the method conforming to the invention.

The method according to the invention will now be described.

Figure 5A illustrates a SOI substrate 1 comprising a carrier substrate 2 in silicon, coated with a layer 3 of silicon oxide SiO_2 and a surface layer 4 in silicon.

The oxide layer 3 is therefore buried between the two layers 2 and 4. Preferably, the thickness of the silicon surface layer is 400 nm or less.

This SOI substrate may have been obtained, for example, using a layer transfer process using the following chief steps:

- creating a weakened region in the thickness of a donor substrate,
- forming an oxide layer on this donor substrate (preferably before creating the weakened region), or on a receiver substrate,
- bonding the donor substrate and receiver substrate,
- detaching along said weakened region.

An example of said transfer process is the SmartCut ® process of which a description can be found in the work: "*Silicon On Insulator Technology : Materials to VLSI* – 2nd Edition" by Jean-Pierre Colinge, published by "Kluwer Academic Publisher", pages 50 and 51.

It will be noted that during the detachment step, it is possible that layer transfer is accompanied by the creation of a substantially annular peripheral shoulder around the substrate that has been formed. This shoulder shall be called a “ring” and carries reference 10.

According to a first embodiment of the invention, the SOI substrate 1 is subjected to rapid thermal annealing RTA, conducted at a temperature of between 1000°C and 1230°C, for a short time, generally less than ten minutes, in a hydrogen and/or argon atmosphere. This process is carried out in a suitable oven.

Preferably, it is conducted at a temperature in the order of 1200°C, for a time of less than three minutes.

As can be seen in figure 5B, the effect of this RTA treatment is to cause the overlapping and encapsulation of the peripheral edge 30 of the buried oxide layer 3,

by a lateral layer called an "encapsulation" layer and referenced 40.

It will also be noted that this encapsulation treatment can also be carried out by long annealing, for example annealing at between 1000°C and 1250°C, for a time of between 5 minutes and a few hours, instead of using RTA.

This encapsulated substrate 1 forms the initial SOI substrate to which the thinning method of the invention is applied.

As shown in figure 5C, this thinning method comprises a first thermal oxidation step, conducted in a horizontal oven (equipment marketed by TEL), over temperature ranges of between 800°C and 1150°C.

This thermal oxidation is conducted under conditions permitting full oxidation of the lateral encapsulation layer 40 i.e. oxidation extending over its entire depth as far as the peripheral edge 30 of the buried oxide layer 3.

The oxidized encapsulation layer carries reference number 40'.

Also, this oxidization treatment additionally has the effect of oxidizing the upper part of the silicon surface layer 4. This oxidized part carries reference 41.

By continuing oxidization of the encapsulation layer 40' as far as the buried oxide layer 3, it is possible during subsequent steps completely to remove and to expose the peripheral edge 30 of layer 3.

As illustrated in figure 5D, a first chemical etch step is then carried out performed firstly to remove the thermal oxide 41 and thereby thin the silicon surface layer 4, and secondly to completely lift away all the unstable parts of the edge of said substrate i.e. the oxidized encapsulation layer 40'. The thinned surface

layer 4 carries reference 4'. The thinned SOI substrate carries reference 1'.

It is noted that oxidation of the silicon surface layer 4 is only conducted over a certain thickness (layer 41), so that after the removal of this layer 41, the thinned layer 4' has the thickness it is desired to obtain. Persons skilled in the art can therefore adapt oxidation parameters taking into account the initial thickness of layer 4 and the desired thickness of the thinned layer 4'.

In one particular application of the invention, a SOI substrate is obtained whose thinned active silicon layer 4' has a thickness of 50 nm or less (extra-thin layer 4'), even of 30 nm or less.

The etch step is preferably conducted using a hydrofluoric acid HF bath. However, it could also be carried out using another strong acid such as sulphuric acid for example.

Preferably, hydrofluoric acid HF solution is used at a concentration of 10% to 50% by volume in water, preferably at a concentration of 10% by volume in water. This solution is applied at a temperature of between 20°C and 30°C, preferably in the region of 25°C. This treatment is conducted for a time of between 30 seconds and 500 seconds, preferably between 100 seconds and 500 seconds, further preferably for 100 seconds.

Typically a hydrofluoric acid solution HF is used at a concentration of 10% by volume in water, applied for between 100 and 500 seconds at between 20°C and 30°C to remove 100 nm of oxide.

The time spent in the HF bath is evidently proportional to the thickness of the oxide generated by the thermal oxidation treatment. This time is slightly increased however, to ensure full removal of the oxide according to the invention.

This first etch bath is followed by a first cleaning step using treatment known under the name RCA. This first treatment consists of successively immersing the SOI substrate in:

- a first bath of water, preferably deionized water,
- a second bath in a solution known as "SC1" (Standard Clean 1) which contains a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized water, then
- a third bath in a solution known as "SC2" (Standard Clean 2) which contains a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and deionized water.

Preferably the SC1 bath is applied at a temperature of 70°C for a time of 3 minutes, whereas the SC2 bath is applied at a temperature of 30°C for a time of 3 minutes.

After this cleaning step, it is observed that numerous particles consisting both of silicon and silicon oxide particles have been deposited on the surface of the thinned layer 4'. These particles carry reference 5 in figure 5E.

An example of the surface of the top layer 4' of a SOI substrate obtained at this stage in the method of the invention is illustrated in figure 3. The substrate 1' emerges from this step in a relatively soiled state, even very soiled since the demolished bridges of the lateral encapsulation layer 40 are deposited in the form of particles or debris.

Next a second etch step is performed, also preferably with hydrofluoric acid HF solution under the conditions described above.

The effect of this second etch step is to lift away the debris 5 which has accumulated on the surface of the thinned SOI substrate 1'.

The first cleaning step and second etch step are successive steps i.e. they follow after each other.

Finally RCA cleaning is carried out such as described previously, to obtain the final substrate 1' illustrated in figure 5F, in which the silicon surface layer 4' is thinned and will subsequently form the layer on which components are to be fabricated.

An example of the result obtained after this cleaning step is illustrated in figure 4, in which it can be ascertained that a large quantity of polluting debris has disappeared.

According to a second variant of embodiment of the invention, the initial substrate 1 has not undergone any encapsulation step. The oxidation treatment is therefore conducted solely so as to form the oxide layer 41. The subsequent steps are identical to those described for the first embodiment.

With the method conforming to the invention, it is therefore possible, if RTA treatment has been used, to maintain the beneficial smoothing effects of this treatment. Additionally, by means of the first extended etch step it is possible to break all the bridges or weakened regions of the encapsulation layer, which is most easy since the silicon oxide layer is very thin, so that subsequently the second etch step does not have any bridge to demolish and therefore does not generate any more polluting particles or debris but allows these particles to be lifted off the surface of the thinned substrate.

This latter advantage also exists even if the initial SOI substrate has not been subjected to any previous encapsulation.

CLAIMS

1. Method to thin a silicon-on-insulator substrate SOI (1) called the "initial substrate" comprising a silicon oxide layer SiO_2 (3) buried between a silicon carrier substrate (2) and a silicon surface layer (4), this method being characterized in that it comprises the following successive steps consisting of conducting:

- thermal oxidation treatment of said initial substrate (1) to cause oxidation of part (41) of said silicon surface layer (4),
- a first cycle of etching then cleaning,
- a second cycle of etching then cleaning,

the etching of the first cycle being conducted so as fully to remove the formed thermal oxide (41), to thin said silicon surface layer (4) and to lift off all the unstable parts of the edge of said initial substrate (1), the etching of the second cycle being conducted to remove from the surface of said thinned substrate, the polluting particles (5) formed during said first etching cycle and which have deposited thereupon, so as to obtain a so-called "final" silicon-on-insulator SOI substrate (1'), whose thinned surface layer (4') forms an active layer.

2. Thinning method according to claim 1, characterized in that the initial SOI substrate (1), before said thermal oxidation treatment, has undergone overlapping and encapsulation treatment of the peripheral edge (30) of said buried silicon oxide SiO_2 layer (3), with a so-called "encapsulation" layer (40) derived from said surface layer (4), and in that the oxidation treatment of said initial substrate (1) is conducted so as to cause oxidation of said lateral

encapsulation layer (40) over its entire depth as far as said buried silicon oxide SiO_2 layer (3).

3. Thinning method according to claim 1 or 2, characterized in that said overlapping and encapsulation treatment is conducted by rapid thermal annealing RTA.

4. Thinning method according to any of the preceding claims, characterized in that the thermal oxidation treatment is conducted at a temperature of between 800°C and 1150°C.

5. Thinning method according to any of the preceding claims characterized in that the different oxidation and etching steps are conducted so as to obtain a final silicon-on-insulator substrate (1´) whose so-called "extra-thin" active silicon layer (4') has a thickness of 50 nm or less.

6. Thinning method according to claim 5, characterized in that the different oxidation and etching steps are conducted so as to obtain a final silicon-on-insulator substrate (1'), whose so-called "extra-thin" active silicon layer (4') has a thickness of 30 nm or less.

7. Thinning method according to any of the preceding claims, characterized in that said initial silicon-on-insulator SOI substrate (1) comprises a silicon surface layer (4) having a thickness of 400 nm or less.

8. Thinning method according to any of the preceding claims, characterized in that the etching of the first and/or second cycle is performed using a pure hydrofluoric acid HF solution diluted in water to a concentration of between 10% and 50% by volume, at a temperature of between 20°C and 30°C for a time of between 30 seconds and 500 seconds.

9. Thinning method according to claim 8, characterized in that the etching of the first cycle is performed using a pure hydrofluoric acid HF solution

diluted in water to a concentration of 10% by volume, in that it is applied at a temperature of between 20°C and 30°C for a time of between 100 s and 500 s, to remove 100 nm of silicon oxide (41).

10. Thinning method according to any of the preceding claims, characterized in that the cleaning of the first and/or second cycle is performed by immersing in water, then in a first bath of solution containing a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized water, then in a second bath of solution containing a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and deionized water.