WHAT IS CLAIMED IS:

1. A dynamic D flip-flop, comprising:

an input terminal, an output terminal and at least one clock signal terminal;

a first latch unit for transmitting data of the input terminal and latching the data under control of a clock signal, wherein the first latch unit is a transmission gate;

a second latch unit for latching data of the output terminal and inversely transmitting the data latched by the first latch unit under control of a clock signal; and

an output driving unit for inverting and outputting the data received from the second latch unit;

the first latch unit, the second latch unit and the output driving unit being sequentially connected in series between the input terminal and the output terminal, and wherein a second node is provided between the second latch unit and the output driving unit;

wherein the second latch unit is a three-state inverter, and the second latch unit outputs in high level, low level and high impedance states by means of a single element under control of a clock signal, and if the three-state inverter is in a high impedance state under control of the clock signals, the data of the second node is latched by parasitic capacitance; and

wherein a positive feedback unit is an inverter connected in parallel to both ends of the output driving unit, and the positive feedback unit for inverting data of the output terminal and feeding the data to the output driving unit, increasing the data latching at the second node.

2. The dynamic D flip-flop according to claim 1, wherein the three-state inverter further comprises a first PMOS transistor, a second PMOS transistor, a first NMOS transistor and a second NMOS transistor sequentially connected in series between a power supply and ground.

3. The dynamic D flip-flop according to claim 2, wherein the first PMOS transistor and the second NMOS transistor perform switch control according to a clock signal, and the clock signals of the first PMOS transistor and the second NMOS transistor are inverted.

4. The dynamic D flip-flop according to claim 2, wherein the second PMOS transistor and the first NMOS transistor perform switch control according to a clock signal, and the clock signals of the second PMOS transistor and the first NMOS transistor are inverted.

5. The dynamic D flip-flop according to claim 1, wherein the second latch unit uses low leakage devices and/or the output driving unit uses high threshold voltage devices.

6. The dynamic D flip-flop according to claim 2, wherein the first NMOS transistor and the second NMOS transistor use low leakage current transistors.

7. The dynamic D flip-flop according to claim 1, wherein the first latch unit uses a delay unit.

8. The dynamic D flip-flop according to claim 7, wherein the clock signal terminal is connected with a clock buffer using low threshold units.

9. The dynamic D flip-flop according to claim 1, wherein a plurality of dynamic D flip-flops are connected in parallel.

10. A data operation unit, comprising a control circuit, an operational circuit and a plurality of dynamic D flip-flops interconnected with each other, the plurality of dynamic D flip-flops being connected in series and/or in parallel, wherein the plurality of dynamic D flip-flops are the dynamic D flip-flop according to any one of claims 1 to 9.

11. A chip, comprising the data operation unit according to claim 10.

12. A hash board for a computing device, comprising the chip according to claim 11.

13. A computing device, comprising a power supply board, a control board, a connection board, a radiator and a plurality of hash boards, the control board connected to the hash boards through the connection board, the radiator provided around the hash boards, and the power supply board configured to supply a power supply for the connection board, the control board, the radiator and the hash boards, wherein the hash board is the hash board according to claim 12.