This Sheet Has Been Replaced



GENERATOR OF CLOCK SIGNALS FOR THE SYNCHRONIZATION OF A SYSTEM FOR PROCESSING DIGITAL DATA PACKETS

ABSTRACT

This generator of clock signals for the synchronization of a system for processing digital data packets (10), on the basis of program clock reference values (PCR) transmitted by the packets, comprising counting means (68-a, 74) for storing a clock reference value (PCR) and incremented under the control of a voltage-controlled oscillator (78), and means (68-b, 76) for storing the contents of the counting means (68-a, 74) includes hardware means (64) for decoding a header signal (12) so as to transfer the contents of the counting means (68-a, 74) into the storage means (68-b, 76) and a processing unit (66) decoding a useful signal (14) of the packets so as to decode the said clock value (PCR) and making a correction to the value held in the storage means (68-b, 76) as a function of the number of transitions of the oscillator between the position of the said characteristic (28) and the position of the said reference clock value (PCR) and furthermore the calculation of the said voltage so as to produce the said clock signals.

Fig. 3