ABSTRACT

FORMATION OF A CAPACITOR USING A SACRIFICIAL ETCH STOP

A method is described for forming capacitors in integrated circuits by making the capacitors concurrently with the fabrication of the interconnection wiring levels. A single additional photolithographic step and two depositions are required to form capacitors within each wiring level. A key feature of the invention is the use of an etch-stop to protect the capacitor dielectric during contact or via etching. The storage plates of the capacitor are formed from two successive conductor levels which can include polysilicon levels as well. The process is particularly suited to the manufacture of logic circuits and can be used effectively in MOSFET, bipolar and BiCMOS processes.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)