CARRIERLESS CHIP PACKAGE FOR INTEGRATED CIRCUIT DEVICES, AND METHODS OF MAKING SAME

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention generally relates to the field of packaging integrated circuit devices, and, more particularly, to a carrierless chip package for integrated circuit devices, and various methods of make same.

2. DESCRIPTION OF THE RELATED ART

Microelectronic devices generally have a die (*i.e.*, a chip) that includes integrated circuitry having a high density of very small components. In a typical process, a large number of die are manufactured on a single wafer using many different processes that may be repeated at various stages (*e.g.*, implanting, doping, photolithography, chemical vapor deposition, plasma vapor deposition, plating, planarizing, etching, etc.). The die typically include an array of very small bond pads electrically coupled to the integrated circuitry. The bond pads are the external electrical contacts on the die through which the supply voltage, signals, etc. are transmitted to and from the integrated circuitry. The die are then separated from one another (*i.e.*, singulated) by backgrinding and cutting the wafer. After the wafer has been singulated, the individual die are typically "packaged" to couple the bond pads to a larger array of electrical terminals that can be more easily coupled to the various power supply lines, signal lines and ground lines.

Electronic products require packaged microelectronic devices to have an extremely high density of components in a very limited space. For example, the space available for

memory devices, processors, displays and other microelectronic components is quite limited in cell phones, PDAs, portable computers and many other products. As such, there is a strong drive to reduce the height of a packaged microelectronic device and the surface area or "footprint" of a microelectronic device on a printed circuit board. Reducing the size of a microelectronic device is difficult because high performance microelectronic devices generally have more bond pads, which result in larger ball/grid arrays and thus larger footprints.

Figures 1A-1B are, respectively, a cross-sectional and top view of an illustrative packaged integrated circuit (IC) device 10. The packaged IC device 10 is comprised of an integrated circuit chip 12 that is affixed to a carrier 14 by an adhesive material 18. The chip 12 and carrier 14 comprise a plurality of bond pads 20 and 22, respectively. A plurality of wire bonds 24 conductively couple the bond pads 20 on the chip 12 with the bond pads 22 on the carrier 14. Also depicted in Figure 1A is a conductive structure 28, such as a printed circuit board, a motherboard, a memory module, or the like. The conductive structure 28 typically comprises a plurality of insulated traces (not shown) and a plurality of bond pads 30. In one illustrative embodiment, the chip 12 is conductively coupled to the conductive structure 28 by a plurality of solder balls 30. The chip 12 is encapsulated with a molding or epoxy compound 16.

Figure 1B is a top view of the device 10 with the epoxy compound 16 removed. As shown therein, the bond pads 22 on the carrier 14 occupy a lot of space. The presence of the bond pads 22 can, in some cases, cause the carrier 14 to delaminate. Such delamination can cause the chip 12 to fail or at least not perform up to its full capabilities. Moreover, the

packaged IC device 10 can be relatively large due to its basic configuration, the components involved, and the manner in which it is fabricated. For example, the distance 11 between the edge of the chip 12 and the edge of the epoxy compound 16 may range from approximately 0.5-1.0 mm. The carrier 14 may have a thickness that varies from approximately 125-450 μm, depending on the application and the composition of the carrier 14. Similarly, the thickness of the epoxy compound 16 may also vary, *e.g.*, from approximately 0.5-1.2 mm. Thus, the overall height 13 of the carrier 14 and epoxy compound 16 may range from approximately 0.40-1.65 mm.

The present invention is directed to a device and various methods that may solve, or at least reduce, some or all of the aforementioned problems.

SUMMARY OF THE INVENTION

The following presents a simplified summary of the invention in order to provide a basic understanding of some aspects of the invention. This summary is not an exhaustive overview of the invention. It is not intended to identify key or critical elements of the invention or to delineate the scope of the invention. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

The present invention is generally directed to a carrierless chip package for integrated circuit devices, and various methods of make same. In one illustrative embodiment, the device comprises an integrated circuit chip comprising an exposed backside surface defining a plane, a plurality of wire bonds that are conductively coupled to the integrated circuit chip, each of the plurality of wire bonds being conductively coupled to a conductive exposed

portion, a portion of the conductive exposed portion being positioned in the plane defined by the backside surface, and an encapsulant material positioned adjacent the integrated circuit chip and the plurality of wire bonds.

In another illustrative embodiment, the device comprises an integrated circuit chip comprising an exposed backside surface defining a plane, a plurality of wire bonds that are conductively coupled to the integrated circuit chip, each of the plurality of wire bonds being conductively coupled to a conductive exposed portion, a portion of the conductive exposed portion being positioned in the plane defined by the backside surface, and an encapsulant material positioned adjacent the integrated circuit chip and the plurality of wire bonds, the encapsulant material comprising a bottom surface that is positioned substantially in the plane, wherein a distance from a side of the integrated circuit chip to a side of the encapsulant material ranges from approximately 0.1-0.4 mm.

In yet another illustrative embodiment, the device comprises an integrated circuit chip comprising an exposed backside surface defining a plane and a plurality of wire bonds that are conductively coupled to the integrated circuit chip, each of the plurality of wire bonds being conductively coupled to a conductive exposed portion, a portion of the conductive exposed portion being positioned in the plane defined by the backside surface, wherein the exposed conductive portions lying in the plane have a substantially rounded configuration. The device further comprises an encapsulant material positioned adjacent the integrated circuit chip and the plurality of wire bonds and a conductive structure that is conductively coupled to the exposed conductive portions.

In one illustrative embodiment, the method comprises positioning an integrated circuit chip adjacent a sacrificial structure comprising a conductive portion, the integrated circuit chip comprising a backside surface, attaching a plurality of wire bonds to the integrated circuit chip, attaching the plurality of wire bonds to the conductive portion of the sacrificial structure to thereby define a conductive portion coupled to each of the wire bonds, forming an encapsulant material adjacent the integrated circuit chip, the wire bonds and the sacrificial structure, and removing the sacrificial structure to thereby expose the backside surface of the integrated circuit chip and at least a portion of the conductive portion that is conductively coupled to each of the plurality of wire bonds.

In another illustrative embodiment, the method comprises positioning an integrated circuit chip adjacent a sacrificial structure comprising a conductive layer, the integrated circuit chip comprising a backside surface, attaching a plurality of wire bonds to the integrated circuit chip and to the conductive layer of the sacrificial structure to thereby define a conductive portion coupled to each of the wire bonds, forming an encapsulant material adjacent the integrated circuit chip, the wire bonds and the conductive layer of the sacrificial structure, and performing a planarization process to remove the sacrificial structure to thereby expose the backside surface of the integrated circuit chip and at least a portion of the conductive portion conductively coupled to each of the plurality of wire bonds.

In yet another illustrative embodiment, the method comprises positioning an integrated circuit chip adjacent a sacrificial structure comprising a plurality of spaced-apart conductive structures, the integrated circuit chip comprising a backside surface, attaching each of a plurality of wire bonds to the integrated circuit chip and to one of the spaced-apart

conductive structures of the sacrificial structure to thereby define a conductive portion coupled to each of the wire bonds, forming an encapsulant material adjacent the integrated circuit chip, the wire bonds and the sacrificial structure, and performing a planarization process to remove the sacrificial structure to thereby expose the backside surface of the integrated circuit chip and at least a portion of the conductive portion conductively coupled to each of the plurality of wire bonds.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figures 1A-1B depict an illustrative prior art packaged integrated circuit device;

Figures 2A-2C are various views of a packaged integrated circuit device in accordance with various aspects of the present invention;

Figures 3A-3E are various views of one illustrative method of forming the device shown in Figures 2A-2C; and

Figure 4 depicts an alternative embodiment of the conductive portion of the sacrificial structure.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Various regions and structures of a packaged integrated circuit device are depicted in the drawings. For purposes of clarity and explanation, the relative sizes of the various features depicted in the drawings may be exaggerated or reduced as compared to the size of those features or structures on real-world packaged devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention. The words and phrases used herein should be understood and interpreted to have a meaning

consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, *i.e.*, a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, *i.e.*, a meaning other than that understood by skilled artisans, such a special definition will be explicitly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

Figures 2A-2C depict one illustrative embodiment of a packaged integrated circuit (IC) device 100 in accordance with one aspect of the present invention. As shown in Figure 2A, the device 100 comprises an integrated circuit chip (IC chip) 102, a plurality of bond pads 104, a plurality of wire bonds 106, each of which are conductively coupled to an exposed conductive portion 108. Also depicted in Figure 2A is the exposed backside 110 of the IC chip 102. An encapsulant material 105, *e.g.*, an epoxy or molding material, encapsulates the IC chip 102 except for the exposed backside surface 110. Figure 2B is a bottom view of the device 100. As shown therein, the conductive portions 108 are positioned in the encapsulant material 105 around the perimeter of the IC chip 102. In the illustrative embodiment depicted in Figures 2A-2C, the exposed conductive portions 108 are on substantially the same plane as the exposed backside 110 of the IC chip 102. Moreover, in one illustrative embodiment, the exposed conductive portions 108 may have a generally circular cross-sectional configuration and a diameter 109 of approximately 16-80 μm.

Figure 2C is one illustrative example that depicts how the device 100 may be conductively coupled to a conductive structure 28. The conductive structure 28 may be any type of structure to which it is desired to operatively couple an integrated circuit device, *e.g.*, a printed circuit board, a silicon interposer, a motherboard, flex tape, a memory module, etc. As shown therein, the device 100 may be operatively coupled to the conductive structure 28 by a plurality of solder balls 32 that are conductively coupled to the exposed conductive portions 108 and the bond pads 30 on the conductive structure 28. As will be recognized by those skilled in the art after a complete reading of the present application, the device 100 may be conductively coupled to the conductive structure 28 by a variety of known techniques.

As will be recognized by those skilled in the art after a complete reading of the present application, the packaged device 100 may be employed with any type of IC chip 102, *e.g.*, memory chips, microprocessors, ASICs, etc. Additionally, the precise shape, location and material of the illustrative bond pads 104 and wire bonds 106 may vary depending upon the particular application. Thus, the illustrative embodiment depicted herein should not be considered a limitation of the present invention.

Figures 3A-3E depict one illustrative method of forming the packaged IC device 100. Figure 3A depicts a plurality of singulated IC chips 102 that are ready to be packaged. The IC chips 102 have been manufactured and singulated using any of a variety of known processing techniques. Initially, as indicated in Figure 3B, the IC chips 102 will be attached to a sacrificial structure 120 using, for example, an adhesive material 103 or adhesive tape. The sacrificial structure 120 comprises at least some conductive material to which the wire bonds 106 will be attached, as described more fully below. In the illustrative embodiment

depicted in Figure 3A, the sacrificial structure 120 comprises a substrate 122 and a layer of conductive material 124, *e.g.*, a metal such as aluminum. In one embodiment, the substrate 122 is comprised of a ceramic material and it may have a thickness of approximately 0.135-0.5 mm. The substrate 122 may also be comprised of other materials, such as an organic laminate, polymer, polyester, silicon, etc. The layer of conductive material 124 may be deposited by a variety of known processes, *e.g.*, sputter deposition, and it may have a thickness of approximately 0.1-30 μm. In the illustrative embodiment depicted in Figure 3A, the conductive portion of the sacrificial structure 120 takes the illustrative form of the conductive layer 124. However, other forms are also possible. For example, as shown in Figure 4, the conductive portion of the sacrificial structure 120 may take the form of a plurality of spaced-apart conductive structures 124A that correspond in location to the conductive end portions 108 of the device 100. The spaced-apart conductive region 124A may be of any desired shape, *i.e.*, rectangular, rounded, etc. Other structures are also possible.

Next, as indicated in Figure 3B, the wire bonds 106 are attached to the IC chips 102 and the conductive portion of the sacrificial structure 120, *e.g.*, the illustrative conductive layer 124. The wire bonds 106 may be comprised of a variety of materials, *e.g.*, gold, aluminum, copper, etc., and they may be attached to the IC chip 102 and the conductive layer 124 using a variety of known techniques. Attaching the wire bonds 106 to the conductive portion of the sacrificial structure 120 results in the formation of the conductive end portions 108. Thus, depending on the particular materials of construction of the wire bond 106 and the conductive portion of the sacrificial structure 120, *e.g.*, the conductive layer 124, the conductive end portions 108 may comprise a combination of such materials.

Then, as shown in Figure 3C, an encapsulant 105, *e.g.*, an epoxy material or molding compound, is formed around the IC chips 102. The encapsulant 105 may be comprised of a variety of known materials, such as epoxy, liquid encapsulant, epoxy mold compound, a powder, etc., and it may be applied or formed around the IC chips 102 using a variety of known techniques.

As shown in Figure 3D, one or more process operations are then performed to remove the sacrificial structure 120 thereby exposing the backside 110 of the IC chips 102 and the exposed conductive portions 108. The sacrificial structure 120 may be removed by a variety of techniques. In one illustrative embodiment, the sacrificial structure 120 may be removed by performing a planarization process. For example, the sacrificial structure 120 may be removed by performing one or more chemical mechanical polishing processes, by performing a grinding process, or by performing an etching process, or a combination of such processes. The end result of these operations is a substantially planar surface 105A which exposes the backside 110 of the IC chips 102 and the exposed conductive portions 108. Figure 3E depicts three individual packaged devices 100 after they have been singulated and after the encapsulant material 105 has been trimmed.

Through use of the present invention, the physical space occupied by the packaged device IC 100 may be reduced as compared to prior art packaged IC devices. Since the present invention does not involve the formation of the relatively large conductive bond pads 22 on a carrier 14, as shown in Figure 1A, the length and width of the overall packaged IC device 100 may be reduced. For example, as shown in Figure 2A, the horizontal dimension 111 from the edge of the IC chip 102 to the edge of the encapsulant material 105 may be

approximately 0.1-0.4 mm. In contrast, the corresponding dimension 11 for the device 10 shown in Figure 1A may be approximately 0.5-1.0 mm. Thus, through use of the present invention, the "footprint" of the packaged IC device 100 may be reduced. Additionally, since the illustrative packaged IC device 100 disclosed herein does not comprise a carrier structure, like the carrier 14 depicted in Figure 1A, it occupies less vertical space, *i.e.*, it is shorter, as compared to prior art packaged IC devices. For example, in one illustrative embodiment, the overall height 113 (see Figure 2A) of the packaged IC device 100 may range from approximately 0.1-0.5 mm.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

WHAT IS CLAIMED:

1. A device, comprising:

an integrated circuit chip comprising an exposed backside surface defining a plane;

a plurality of wire bonds that are conductively coupled to said integrated circuit chip, each of said plurality of wire bonds being conductively coupled to a conductive exposed portion, a portion of said conductive exposed portion being positioned in said plane defined by said backside surface; and

an encapsulant material positioned adjacent said integrated circuit chip and said plurality of wire bonds.

2. The device of claim 1, wherein a distance from a side of said integrated circuit chip to a side of said encapsulant material ranges from approximately 0.1-0.4 mm.

3. The device of claim 2, wherein a distance from said backside surface to a top surface of said encapsulant material ranges from approximately 0.1-0.5 mm.

4. The device of claim 1, wherein said exposed conductive portions lying in said plane have a substantially rounded configuration.

5. The device of claim 1, wherein said encapsulant material comprises an epoxy compound, a molding compound and a liquid encapsulant.

6. The device of claim 5, wherein said encapsulant material has a bottom surface that is substantially positioned in said plane.

7. The device of claim 4, wherein said backside surface is a surface that has been subjected to at least one processing operation after said encapsulant material is formed.

8. The device of claim 1, further comprising a conductive structure that is conductively coupled to said exposed conductive portions.

9. The device of claim 8, wherein said conductive structure comprises a printed circuit board, a silicon interposer, a motherboard, flex tape, or a memory module.

10. The device of claim 8, wherein said integrated circuit chip is conductively coupled to said conductive structure by a plurality of conductive balls.

11. A method, comprising:

positioning an integrated circuit chip adjacent a sacrificial structure comprising a conductive portion, said integrated circuit chip comprising a backside surface;

attaching a plurality of wire bonds to said integrated circuit chip;

attaching said plurality of wire bonds to said conductive portion of said sacrificial structure to thereby define a conductive portion coupled to each of said wire bonds;

forming an encapsulant material adjacent said integrated circuit chip, said wire bonds and said sacrificial structure; and

removing said sacrificial structure to thereby expose said backside surface of said integrated circuit chip and at least a portion of said conductive portion that is conductively coupled to each of said plurality of wire bonds.

12. The method of claim 11, further comprising trimming excess portions of said encapsulant material after removing said sacrificial structure.

13. The method of claim 12, wherein said trimming of said excess portions of said encapsulant material is performed such that a distance from a side of said integrated circuit chip to a side of said encapsulant material ranges from approximately 0.1-0.4 mm

14. The method of claim 11, wherein said conductive portion of said sacrificial structure comprises a layer of conductive material formed above a substrate, and wherein said plurality of wire bonds are attached to said layer of conductive material.

15. The method of claim 11, wherein said conductive portion of said sacrificial structure comprises a plurality of spaced-apart conductive structures, and wherein each of said plurality of wire bonds are attached to one of said spaced-apart conductive structures.

16. The method of claim 11, wherein removing said sacrificial structure comprises performing a planarization process to remove said sacrificial structure.

17. The method of claim 11, wherein removing said sacrificial structure comprises performing at least one chemical mechanical polishing process to remove said sacrificial structure.

18. The method of claim 11, wherein removing said sacrificial structure comprises performing at least one grinding process to remove said sacrificial structure.

19. The method of claim 11, wherein removing said sacrificial structure comprises performing at least one etching process to remove said sacrificial structure.

20. The method of claim 11, further comprising conductively coupling a conductive structure to said exposed portions that are conductively coupled to said wire bonds.

21. The method of claim 11, wherein removing said sacrificial structure further exposes a surface of said encapsulant material.