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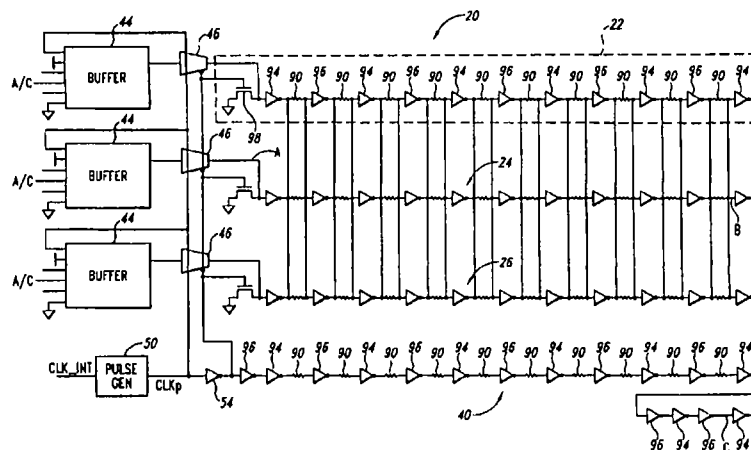
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(54) Title: HIGH SPEED SIGNAL PATH AND METHOD



(57) Abstract: A high speed data path (Fig.3, 22, 24, 26) includes a first plurality of inverters (Fig.3, 96) skewed toward one logic level alternating with a second plurality of inverters (Fig.3, 94) skewed toward a second logic level. As a result, the inverters in the first plurality accelerate one transition of a digital signal and the inverters in the second plurality accelerate the opposite transition of the digital signal. Prior to applying the digital signal to the inverters, the inverters are preset to a logic level from which they will transition in an accelerated manner. As a result, a transition of the digital signal is coupled through the inverters in an accelerated manner. A first of the high speed data paths (Fig.3, 40) is used to couple a clock signal to a clock output terminal. The inverters in the second high speed data path are collectively skewed less than the inverters in the first high speed data path so that the period that the digital signal is present at the signal output terminal encompasses the period that the clock signal is present at the clock output terminal. As a result, the clock signal the clock output terminal can be used to provide a data valid window for the digital signal.



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WO 02/063629 A1