

FIG. 1

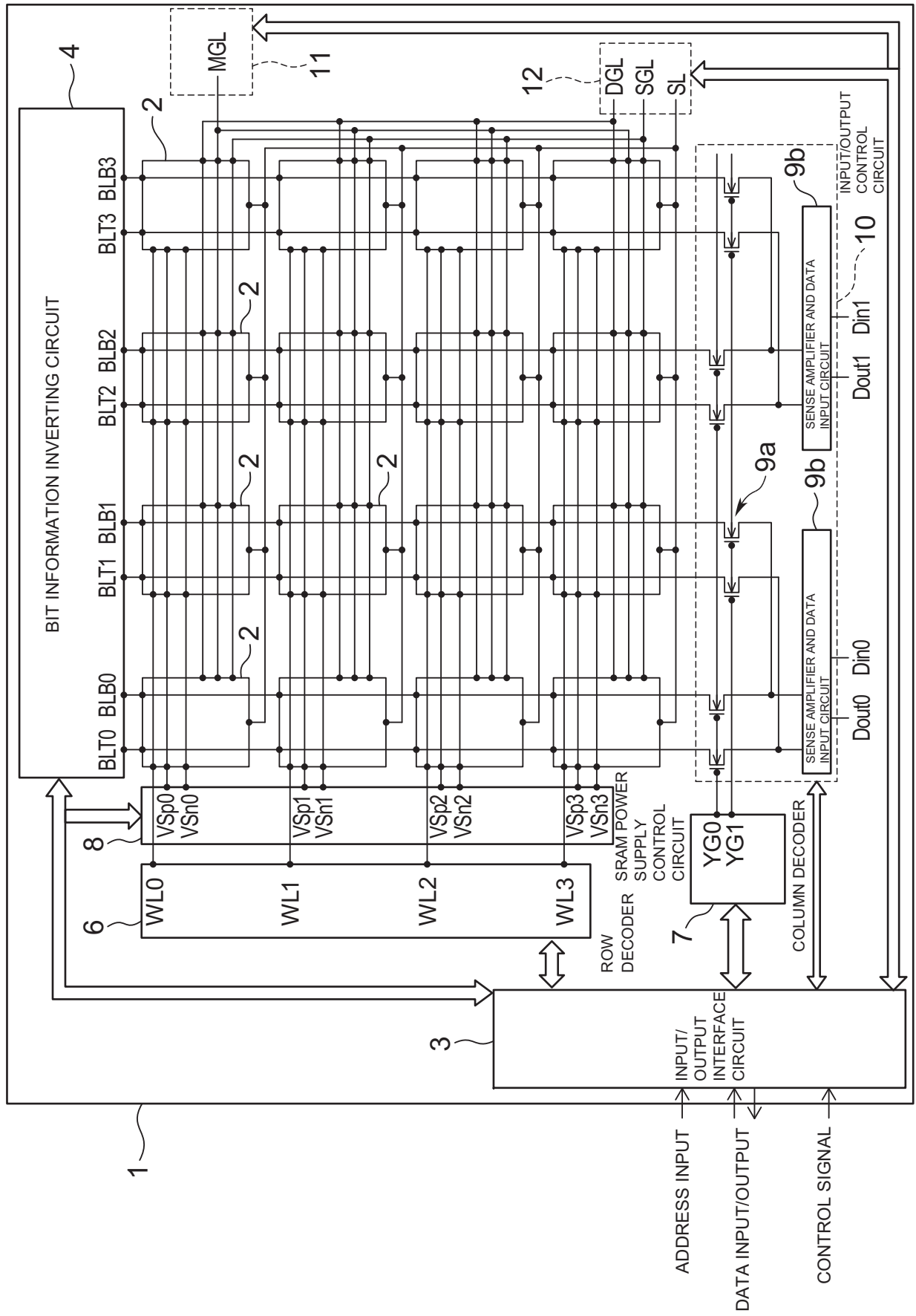


FIG. 2

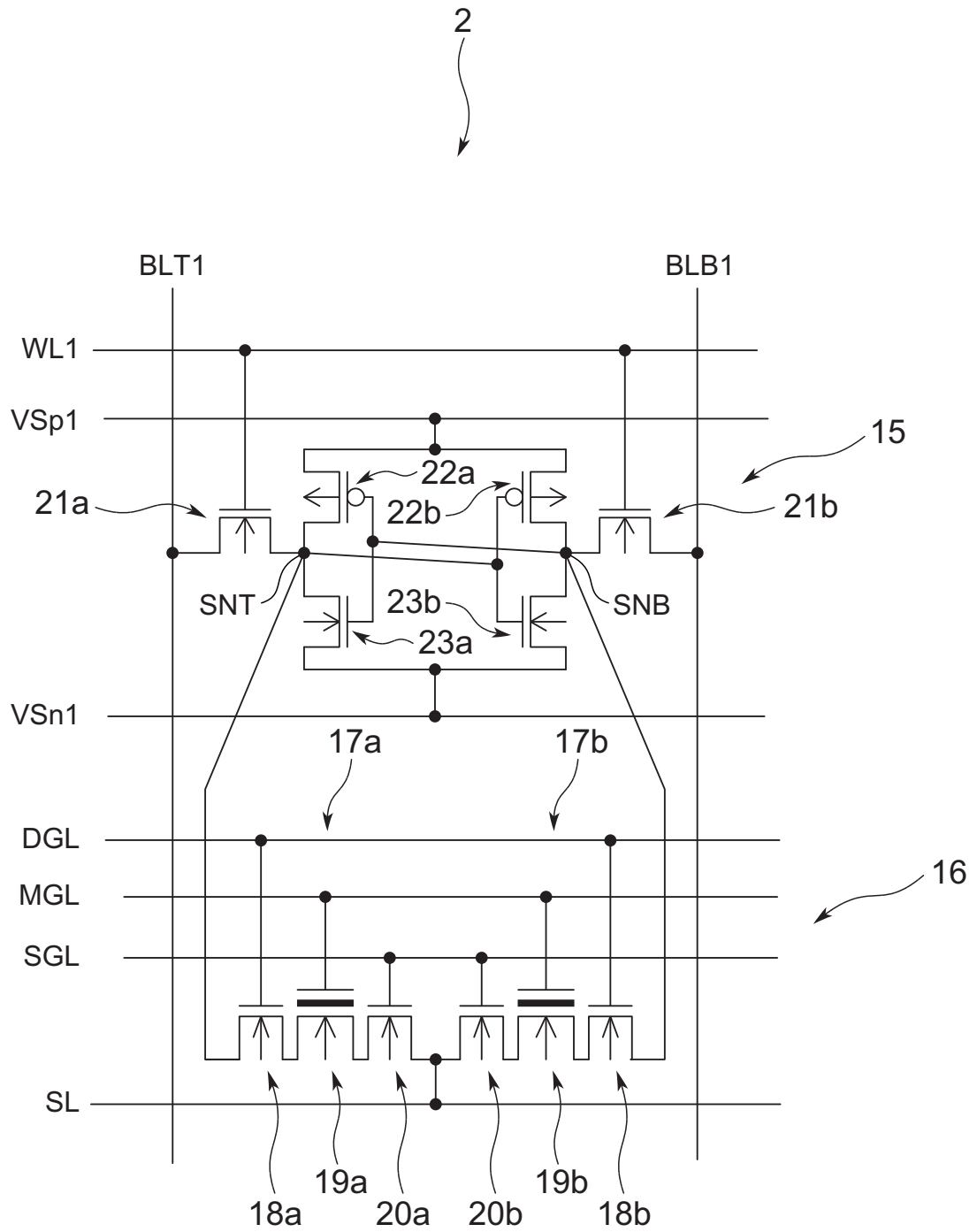


FIG. 3

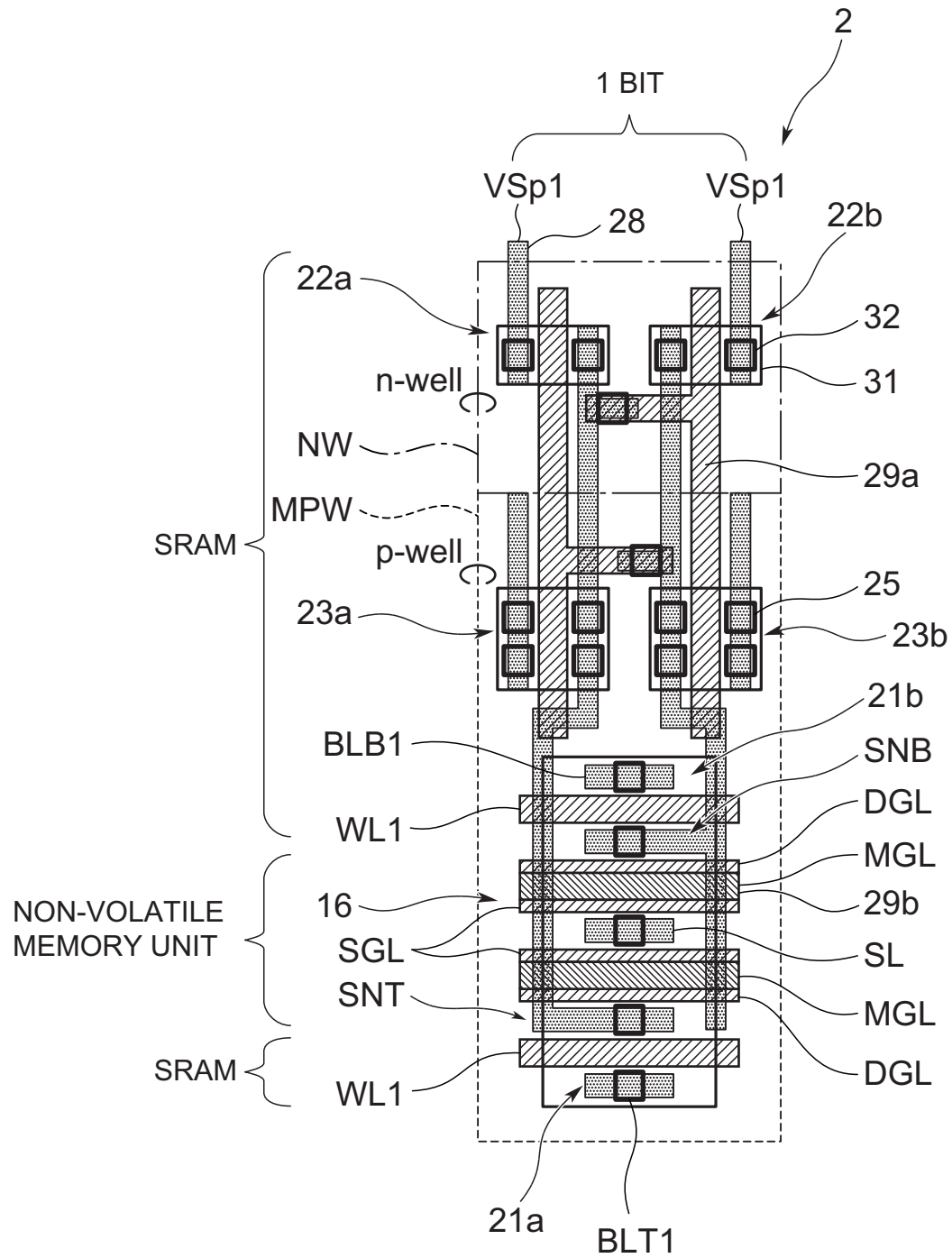


FIG. 4

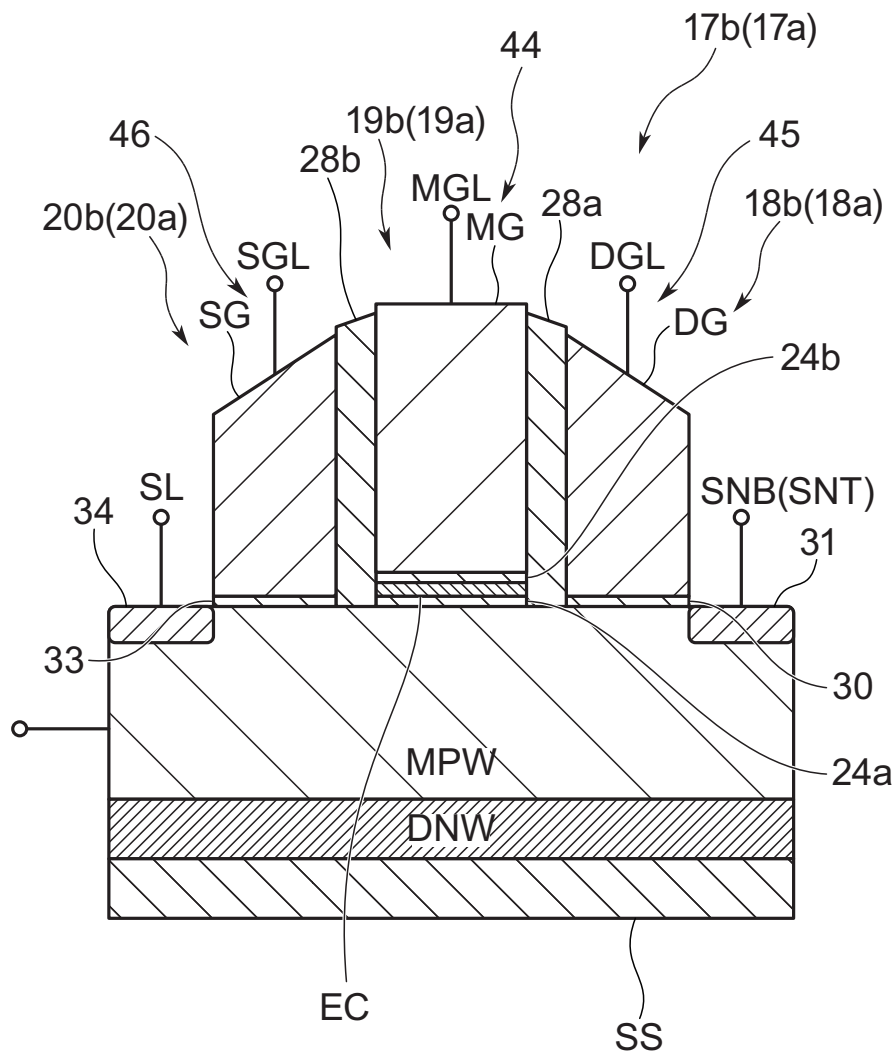


FIG. 5

	MGL	DGL	SGL	SL	SNT/ SNB	WL1
Program(sram to flash)	12	VDD	0	0	0 or VDD	0
Erase(reset data in flash)	-12	0	0	0	Don't care	0
Write(external data to sram)	0	0	0	0	Don't care	VDD/0
Read(output sram data)	0	0	0	0	0 or VDD	VDD/0

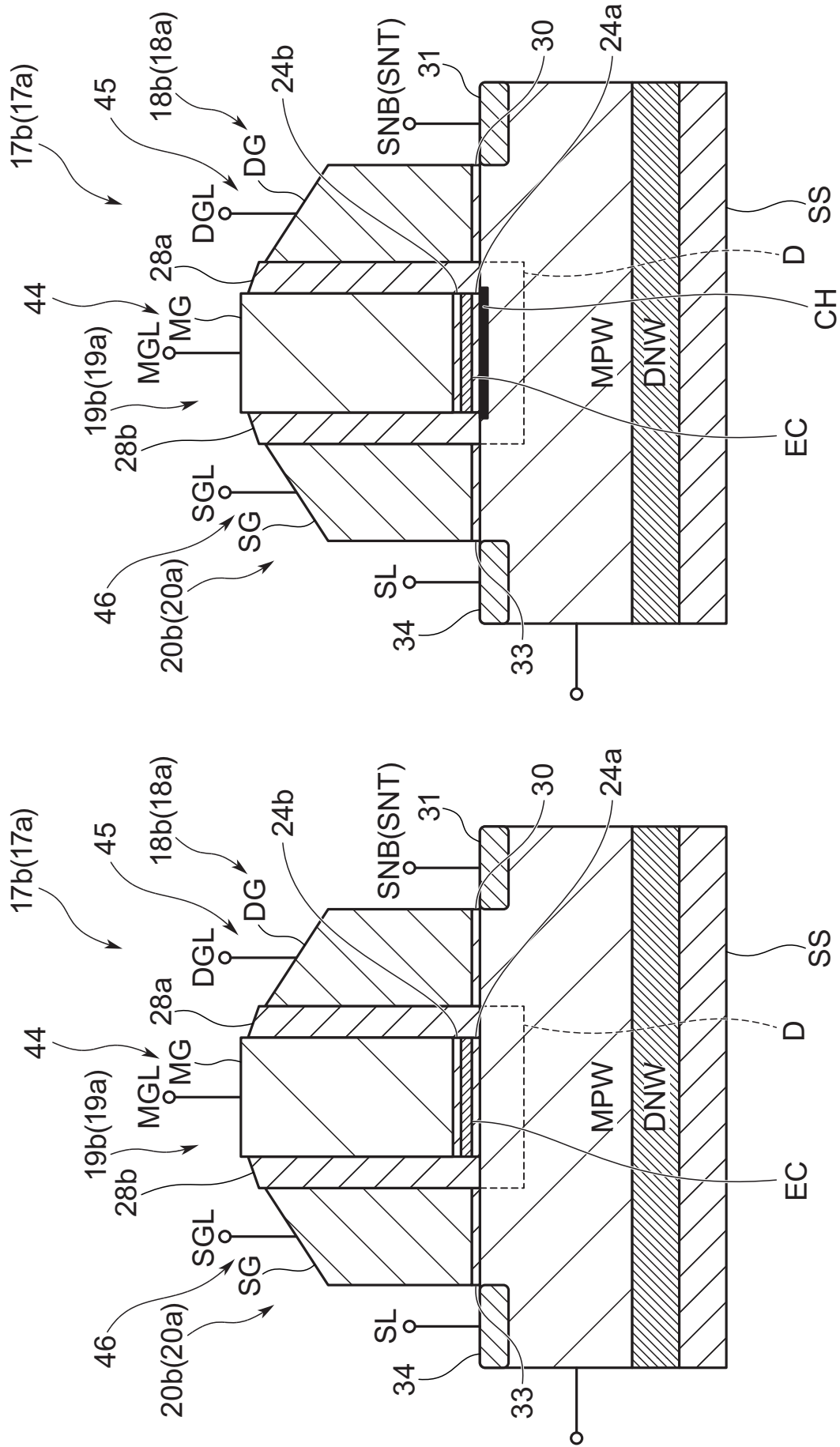


FIG. 6B

FIG. 6A