CLAIMS

What is claimed is:

1. A nanowire transistor, comprising: at least one nanowire channel having a first end, and an opposing second end, wherein the at least one nanowire channel is disposed over a microelectronic substrate; a source structure proximate the at least one nanowire first end, wherein a first underlayer etch stop structure is disposed between the source structure and the at least one nanowire first end and disposed between the entire source structure and the microelectronic substrate; and a drain structures proximate the at least one nanowire second end, wherein a second underlayer etch stop structure is disposed between the drain structure and the at least one nanowire second end and disposed between the entire drain structure and the microelectronic substrate.

2. The nanowire transistor of claim 1, further including a gate dielectric material abutting the nanowire channel between the nanowire channel first end and the nanowire channel second end.

3. The nanowire transistor of claim 2, further including a gate electrode material abutting the gate dielectric material.

4. The nanowire transistor of claim 1, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

5. The nanowire transistor of claim 4, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

6. The nanowire transistor of claim 4, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

7. The nanowire transistor of claim 1, wherein the at least one nanowire channel comprises a plurality of nanowires channels formed above the microelectronic substrate, wherein the nanowire channels are spaced apart from one another.

8. A computing device, comprising: a board including at least one component; wherein the at least one component includes at least one microelectronic structure comprising at least one nanowire transistor including at least one nanowire channel having a first end, and an opposing second end, wherein the at least one nanowire channel is disposed over a microelectronic substrate; a source structure proximate the at least one nanowire first end, wherein a first underlayer etch stop structure is disposed between the source structure and the at least one nanowire first end and disposed between the entire source structure and the microelectronic substrate; and a drain structures proximate the at least one nanowire second end, wherein a second underlayer etch stop structure is disposed between the drain structure and the at least one nanowire second end and disposed between the entire drain structure and the microelectronic substrate.

9. The computing device of claim 8, further including a gate dielectric material abutting the nanowire channel between the nanowire channel first end and the nanowire channel second end.

10. The computing device of claim 9, further including a gate electrode material abutting the gate dielectric material.

11. The computing device of claim 8, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are the same material.

12. The computing device of claim 11, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon germanium.

13. The computing device of claim 11, wherein the nanowire channel, the first underlayer etch stop structure, and the second underlayer etch stop structure are silicon.

14. The computing device of claim 8, wherein the at least one nanowire channel comprises a plurality of nanowires channels formed above the microelectronic substrate, wherein the nanowire channels are spaced apart from one another.