

The invention relates to a circuit arrangement for transformation according to the preamble of patent claim 1.

From NTZ Archive Vol. 3 (1981), Book 1, page 9 ff a new type of function system (m-functions) is known as is its application in picture transmission. With the aid of feedback shift registers two-value periodic pulse sequences may be produced. By ortho-normalisation of these sequences an ortho-normal, binary function system is obtained which serves as the basic function system for a signal transformation (m-transformation) similar to the Fourier or Walsh transformation.

It is the object of the invention to provide a transformation circuit which makes it possible at low cost on circuitry to transform vectors and for example may be used as a discrete cyclic correlator for m-transformation in picture processing.

The object is achieved by the features stated in the characterising part of patent claim 1. Advantageous modifications of the invention are described in the dependent claims.

When transforming an unknown vector $\vec{A}$ with the aid of a matrix $\underline{B}^2$ the matrix is constructed according to the invention such that a known vector $\vec{B}$ is shifted cyclically in lines and thus forms a quadratic matrix. The transformation of the unknown vector $\vec{A}$ with the thus constructed matrix $\underline{B}^2$ produces the transform $\vec{T}$ simply in terms of circuitry. According to the invention the precondition is made that the vectors $\vec{A}$ and $\vec{B}$ have the same

length N and the vector $\vec{B}$ which builds up the matrix $\underline{B}^2$ is present in binary form.

In order to implement the transformation according to the relationship:

$$\vec{T} = \frac{1}{N} * \underline{B}^2 * \vec{A} \quad (1)$$

with:

$$\vec{T} = \begin{bmatrix} T_0 \\ . \\ . \\ T_{N-1} \end{bmatrix}, \vec{A} = \begin{bmatrix} a_0 \\ . \\ . \\ a_{N-1} \end{bmatrix}, \underline{B}^2 = \begin{bmatrix} b_0 & b_1 & b_2 & \dots & b_{N-1} \\ b_1 & b_2 & & & b_0 \\ & . & & & \\ b_{N-1} & b_0 & \dots & \dots & b_{N-2} \end{bmatrix}$$

the unknown vector $\vec{A}$ is subdivided according to the invention into P groups having the length R . The number of groups P is calculated depending on the group length R which is selected and on the vector length N as follows:

$$P = \text{Int} \left(\frac{N}{R} \right) + 1 \quad (2)$$

If the vector length N is not a whole number multiple of the group length R , then the last group is filled up with zeros, so that all the groups are of equal length. Then the following is true:

$$a_i = 0 \quad \text{für } N-1 < i < P * R \quad (3)$$

With parallel processing the individual groups are supplied to one addition stage each, the construction of the individual addition stages being the same. The output signals of the addition stages are then supplied via logic connection circuits, which are in turn constructed the same for each group, to an arithmetic unit. The arithmetic unit delivers the transform as an output signal.

With serial processing of the individual groups only one addition stage and one linking circuit is required. The outputs of the linking circuit are then connected via multiplexers to an accumulator, after which is connected a register, to the outputs of which is applied the transform after all of the groups have been worked through.

By subdividing the vector to be transformed into groups a reduction in the cost of transformation is achieved, since the number of additions to be carried out and thus the number of adders required is substantially reduced. Moreover, multiplication circuits are not required, since the transformation matrix $\underline{B}^2$ is constructed from binary symbols.

Below the invention is described in greater detail together with the drawings so as to make the invention easier to understand. In which:

Fig. 1 shows a general block circuit diagram for parallel processing,

Fig. 2 shows the construction of an addition circuit,

Fig. 3 shows a quadratic matrix,

Fig. 4 shows a calculation table for the linking circuit,

Fig. 5 shows a logic linking circuit,

Fig. 6 shows an arithmetic unit and

Fig. 7 shows a block circuit diagram for serial processing.

Fig. 1 shows a block circuit diagram for transforming an unknown vector $\vec{A}$ of the length N with the aid of a matrix B^2 . The vector $\vec{A}$ with the elements a_i where $i = 0, 1, \dots, N-1$ is read into a buffer 1. The outputs of the buffer 1 a_i are subdivided into P groups 2, 3, 4 of the length R according to the equations (2) and (3). The R signals $a_{n \cdot R}, \dots, a_{n \cdot R + R - 1}$ (group numbers $n = 0, \dots, P-1$) of each group are supplied in each case to an addition circuit U_n 5, 6, 7, the output signals of which $u_{n,j}$ are calculated with $j = 0, \dots, 2^R - 1$ according to the mathematical relationship:

$$u_{n,j} = \sum_{m=0}^{R-1} a_{n \cdot R + m} * x_{j,m} \quad (4)$$

Here $x_{j,m}$ is the m th digit of the binary representation of the number j . For $j=3=(011)_2$ for example $x_{3,0} = 1, x_{3,1} = 1, x_{3,2} = 0$.

The determination of 2^R values $u_{n,j}$ in each block u_n only requires 2^{R-1} additions, since the addition circuit is constructed according to the following table:

- definition of $u_{n,0}$, in which $u_{n,0} = 0$ is always true.
- definition of $u_{n,j}$, for which $j = 2^m$ is true, i.e. according to equation (4) $u_{n,j} = a_{n \cdot R + m}$, since the binary

representation of j only contains one digit with the value 1.

- c) determination of $u_{n,j}$, which are the total of two $u_{n,j}$ according to b). The binary representation of j therefore has two digits with the value 1.
- d) determination of $u_{n,j}$, which is produced by the sum of two values according to b) and c). The binary representation of j thus has three digits with the value 1.
- e) etc.

Fig. 2 shows the construction of an addition circuit U_n corresponding to equation (4) and the illustrated table for a vector length of $N=5$ and a group length of $R=3$.

The output $u_{n,0}$ is connected to zero. The outputs $u_{n,1}$, $u_{n,2}$ and $u_{n,4}$ are connected direct to the inputs a_{n*R} , a_{n*R+1} and a_{n*R+2} . The result of addition of a_{n*R} and a_{n*R+1} is applied across output $u_{n,3}$, the result of addition of a_{n*R} and a_{n*R+2} is applied to output $u_{n,5}$, the result of addition of a_{n*R+1} and a_{n*R+2} is applied to the output $u_{n,6}$ and the result of addition of all the inputs is applied to the output $u_{n,7}$.

According to equation (2) $P = 2$ addition circuits would be required during parallel processing.

The outputs $u_{n,j}$ of the addition circuits 5,6,7 in Fig. 1 are connected in each case to a linking circuit V_n 8,9,10. The linking circuits V_n are constructed in each case so that the output signals $d_{n,k}$ where $k = 0, \dots, N-1$ are linked with the input signals $u_{n,j}$ according to the relationship:

$$d_{n,k} = u_{n,j(k)} \quad (5)$$

with

$$j(k) = \sum_{m=0}^{R-1} 2^{m*b} (k+m) \text{ modulo } N \quad (6)$$

Since the values for $j(k)$ are independent of n , the construction of the linking circuit V_n is the same in each group. For linking the outputs $d_{n,k}$ with the inputs $u_{n,j}$ according to the equations (5) and (6) a calculation table may be derived from the quadratic matrix $\underline{B}^2$ (c.f. equation (1)), which is shown in Fig. 4a. For the example with $N = 5$ and $R = 3$ with a known vector $B = \{0, 1, 1, 0, 1\}$ the quadratic matrix $\underline{B}^2$, which is shown in Fig. 3, is produced and the calculation table for the linking circuit, which is shown in Fig. 4b.

Fig. 5 shows the circuit construction of the linking circuit for the stated example. The outputs $d_{n,k}$ are connected to the inputs $u_{n,j}$ according to the equations (5) and (6) using the values ascertained in the calculation table Fig. 4b. From Fig. 4 for example for $k = 2$ there is the value $j = 5$, i.e. the output $d_{n,2}$ is connected to the input $u_{n,5}$.

The outputs $d_{n,k}$ of the linking circuits 8-10 in Fig. 1 are connected to an arithmetic unit RW1, at the outputs of which occur the values $N * T_k$, from which, simply by division by N , the

components T_k of the transforms $\vec{T}$ may be ascertained. The arithmetic unit RW1 is so constructed that the output signals $N * T_k$ are ascertained according to the relationship:

$$N * T_k = \sum_{n=0}^{P-1} d_{n, (k+n*R) \text{ modulo } N} \quad (7)$$

Fig. 6 shows the implementation of the arithmetic unit RW1 according to equation (7) for the stated example. The value for $5 * T_3$ is apparent for example as the total of the signal $d_{0.3}$ of the first linking circuit V_0 and that of the signals $d_{1.1}$ of the second linking circuit V_1 , which are shifted cyclically by the value $R = 3$.

With serial processing, for which Fig. 7 shows an example with $N = 5$, $R = 3$ and $P = 2$, initially the first R elements of the vector $\vec{A}$ are inserted into a buffer 17 of the length R . The outputs of the buffer 17 are connected to an addition circuit 5, which is constructed exactly as the addition circuits used in parallel processing. A linking circuit 8 is connected to this and is identical in construction to a linking circuit in parallel processing.

The outputs $d_{n,k}$ of the linking circuit V are then supplied to an arithmetic unit RW2 18, which includes in each case a multiplexer 19-23, an accumulator A_k 24-28 and a register RG 29-33 for each of the N values T_k ^{of the transform $\vec{T}$} to be calculated. The N values $d_{n,k}$ of the linking circuit V supplied in succession for each group n at a time spacing T_G , which are ascertained from the R

84H

elements a_i which belong in each case to one group and are read at the timing T_G into the buffer, are added up in the accumulators 24-28 by switching over the subsequent multiplexer 19-23 at the timing T_G , in accordance with the allocation laid down by the equation (7). After working through all of the P groups, i.e. after a time portion of the length $P \cdot T_G$, the accumulators 24-28 include the values $N \cdot T_k$ according to equation (7), which are then entered into the following registers 29-33, i.e. the clock frequency of the registers amounts to $P \cdot T_G$. At the same time as the results are entered into the registers the accumulators are reset so that the next vector $\vec{A}$ may be processed.

This circuit arrangement finds application for example in the implementation of a discrete correlation according to equation (1) or a discrete convolution. The circuit arrangement may for example be used as a discrete cyclical correlator in pulse recognition in code multiplex transmission, for time delay measurement in radar technology, as a matched filter, for m -transformation in picture processing, in cryptography, for error correction or for synchronising in digital data transmission.

With several circuit arrangements connected side by side in parallel according to Figures 1 or 7 several vectors or matrices may be transformed into one spectral range at the same time.

The following circuits are suitable as components for the digital correlator. One or more D-flip-flops may be used for the reference number 1, which exist as integrated circuits '74 (see Texas Instruments ("The TTL Data Book"). One or more full adders

'83 may be used for the reference numbers 5,6 and 7, for reference numbers 8,9 and 10 the conductors are accordingly linked or wired together. One or more full adders '83 or '283 also may be used for reference number 11, one or more full adders '83 or '283 for reference numbers 12-16, one or more serial in/parallel out integrated circuits '95 or '164 for reference number 17, one or more D-flip-flops and full adders '74 and '83 for the reference numbers 24-28, one or more D trigger stages '74 for the reference numbers 29-33 and in each case one or more multiplexers '53 may be used for the reference numbers 19-23. Here, the "" corresponds to TTL circuits of the 74, 74LS, 74ALS, 74S etc. families for example the component '00 corresponds to the integrated circuits 7400, 74LS00, 74AS00 or 74S00.



=====

1. A circuit arrangement for parallel transformation of a vector $\vec{A}$ of the length N comprising the elements $\{a_0, \dots, a_1 \dots a_{N-1}\}$ with the aid of a quadratic matrix B^2 , characterised in that the matrix B^2 is constructed such that the lines of the matrix B^2 include a vector $\vec{B}$ of the length N comprising the elements $\{b_0, \dots, b_1, \dots, b_{N-1}\}$, which vector is shifted cyclically to the left in lines, that the vector $\vec{A}$ is subdivided into P vector parts, which each comprise R successive elements of the vector $\vec{A}$ and which are numbered through from 0 to $P-1$, in which the last vector part is filled up with zeroes, if the length N of the vector $\vec{A}$ is not a whole numbered multiple of the vector part length R , that each vector part is supplied in each case to an addition circuit U_n , which delivers 2^R output signals $u_{n,j}$ with $j = 0, \dots, 2^R-1$, which are calculated according to the mathematical relationship:

$$u_{n,j} = \sum_{m=0}^{R-1} a_{n * R + m} * x_{j,m}$$

in which the symbol $*$ signifies a multiplication and n represents the number of a vector part with $n = 0, \dots, P-1$, $a_{n * R + m}$ elements of the n th vector part and $x_{j,m}$ represents the m th digit of the binary representation of the number j , that the output signals $u_{n,j}$ of each addition circuit U_n are supplied in each case to a linking circuit V_n , which delivers N output signals $d_{n,k}$ with $k = 0, \dots, N-1$, which are ascertained according to the mathematical relationship:



$$d_{n,k} = u_{n,j(K)}$$

with

$$j(K) = \sum_{m=0}^{R-1} 2^{m*b} (K+m) \text{ modulo } N$$

in which $b_{(K+m)} \text{ modulo } N$ represents elements of the vector B , that the output signals $d_{n,k}$ of all the linking circuits V_n are supplied to an arithmetic unit $RW1$, which is constructed according to the mathematical relationship:

$$N * T_K = \sum_{n=0}^{P-1} d_{n, (K+n*R)} \text{ modulo } N$$

in which $N*T_K$ represents an output signal of the arithmetic unit $RW1$ and K is the number of an output signal and that the N output signals $N*T_K$ of the arithmetic unit $RW1$ are the values of the transforms T multiplied by the factor N .

2. A circuit arrangement for serial transformation of a vector $\vec{A}$ of the length N comprising the elements $\{a_0, \dots, a_1 \dots a_{N-1}\}$ with the aid of a quadratic matrix $\underline{B}^2$, characterised in that the matrix $\underline{B}^2$ is constructed such that the lines of the matrix $\underline{B}^2$ include a vector $\vec{B}$ of the length N comprising the elements $\{b_0, \dots, b_1, \dots, b_{N-1}\}$, which is shifted cyclically in lines, that the vector $\vec{A}$ is subdivided into P vector parts, which comprise in each case R successive elements of the vector $\vec{A}$ and which are numbered through from 0 to $P-1$, in which the last vector part is filled up with

zeroes, if the length N of the vector $\vec{A}$ is not a whole numbered multiple of the vector part length R , that the vector parts of an addition circuit U , which operates like an addition circuit U_n as defined in Claim 1, are supplied in succession in the time interval T_G , that the output signals $U_{n,j}$ of the addition circuit U are supplied to a linking circuit V which operates like a linking circuit V_n as defined in claim 1, and that the output signals $d_{n,k}$ of the linking circuit V are supplied to an arithmetic unit $RW2$, which, after working through all of the P vector parts, i.e. after a time interval of the length $P * T_G$, delivers as output signals the values $N * T_K$ of the transforms T multiplied by the factor N , and that in the arithmetic unit $RW2$ for calculating the output signals $N * T_K$ the partly succeeding output signals $d_{n,k}$ over time are linked according to the mathematical relationship:

$$N * T_K = \sum_{n=0}^{P-1} d_{n, (K+n*R)} \text{ modulo } N$$

in which the symbol $*$ signifies a multiplication.

3. A circuit arrangement according to claim 2, characterised in that the arithmetic unit $RW2$ is constructed from N accumulators, which are operated at a clock frequency of $1 / T_G$, to which accumulators the values $d_{n,k}$ which are required to calculate an output signal $N * T_K$ are supplied in each case via multiplexers switched by the timing pulse T_G and after which in each case a register is connected, which is operated at a clock frequency of $P * T_G$ and thus receives the results in the



accumulators after a time spacing $P * T_G$ in each case and passes them to the outputs of the arithmetic unit RW2.