PROCESS FOR FABRICATING A CFET DEVICE

FIELD OF THE INVENTION

The present invention relates to a process for fabricating a CFET device.

PRIOR ART

A CFET device (CFET being the acronym of “complementary field-effect transistor) may be defined as a structure comprising complementary fin field-effect transistors (FinFETs). In other words, it is a three-dimensional electronic device consisting in stacking two FinFET transistors of different types, for example an n-type transistor (so-called nFET) on a p-type transistor (so-called pFET).

Such a stack allows the footprint of the device to be decreased and therefore the density of transistors per unit area to be increased.

Conventionally, a CFET device is produced from a bulk single-crystal silicon substrate integrating a buried sacrificial layer. This sacrificial layer may, for example, be a silicon-germanium (SiGe) layer, in which vertical trenches are etched that allow the various fins of the transistors to be defined. The selective etching of the sacrificial layer allows the vertical physical separation of these two n-type and p-type FinFET transistors.

The active zones intended to form the source and drain regions of the complementary FinFET transistors may be n- and p-doped, for example by selective implantation in the thickness of the structure thus formed.

Moreover, depending on the type of application targeted, the channels could be n- or p-doped. This doping may also be carried out by selective implantation in the thickness of the structure.

The decrease in the width of the fins must be accompanied by an increase in the height of the active zones, and in particular of the channels, in order to allow the amount of electrical current that is able to be passed to be increased.

However, there are technological limitations to the fabrication of the fins, in particular in terms of height/width ratio, so that the density of transistors per unit area achievable while keeping an acceptable electrical performance tends toward a threshold.

SUMMARY

One aim of the invention is to improve the design and fabrication of CFET devices.

According to an aspect of the present invention, there is provided a process for fabricating a CFET device, wherein it comprises:

- forming a double semiconductor-on-insulator substrate comprising, in succession, from its base to its surface: a carrier substrate, a first electrically insulating layer, a first

CLAIMS

1. A process for fabricating a CFET device, wherein it comprises:

- forming a double semiconductor-on-insulator substrate comprising, in succession, from its base to its surface: a carrier substrate, a first electrically insulating layer, a first single-crystal semiconductor layer , a second electrically insulating layer and a second single-crystal semiconductor layer;

- forming trenches from the surface of said substrate, to the first electrically insulating layer, so as to form at least one fin,

- in each fin, forming a channel of a first transistor in the first semiconductor layer and a channel of a second transistor of opposite type to the first transistor in the second semiconductor layer,

the formation of the double semiconductor-on-insulator substrate comprising:

- a first layer-transfer step in order to transfer the first electrically insulating layer and the first single-crystal semiconductor layer to the carrier substrate, so as to form a first semiconductor-on-insulator substrate, said first layer-transfer step comprising a heat treatment at a sufficiently high temperature to smooth the first single-crystal semiconductor layer to a roughness lower than 0.1 nm RMS,

- after said heat treatment, a second layer-transfer step in order to transfer the second electrically insulating layer and the second single-crystal semiconductor layer to the first single-crystal semiconductor layer of the first semiconductor-on-insulator substrate.

2. The process as claimed in claim 1, wherein the trenches are formed by etching, the first electrically insulating layer forming a stop layer for said etching.

3. The process as claimed in either one of claims 1 and 2, wherein the thickness of the first and second single-crystal semiconductor layers is comprised between 25 and 40 nm.

4. The process as claimed in one of claims 1 to 3, wherein the thickness of the second electrically insulating layer is comprised between 10 and 30 nm.

5. The process as claimed in one of claims 1 to 4, wherein the first and second semiconductor layers are made of silicon doped opposite types.

6. The process as claimed in one of claims 1 to 4, wherein the first and second semiconductor layers are made of silicon having different crystal orientations.

7. The process as claimed in one of claims 1 to 4, wherein the first and second semiconductor layers are made of different materials.

8. The device as claimed in one of claims 1 to 4 and 7, wherein the semiconductor layer in which the channel of an n-type transistor is formed is made of strained silicon.

9. The process as claimed in one of claims 1 to 4 and 7 and 8, wherein the semiconductor layer in which the channel of a p-type transistor is formed is made of silicon-germanium.

10. The process as claimed in one of claims 1 to 9, wherein the first and/or second electrically insulating layers are made of silicon oxide (SiO_2).

11. The process as claimed in one of claims 1 to 9, wherein the first and second electrically insulating layers are made of different materials.

12. The process as claimed in one of claims 1 to 9 and 11, wherein the first electrically insulating layer is made of a high-k material.

13. The process as claimed in one of claims 1 to 9, 11 and 12, wherein the second electrically insulating layer is made of a low-k material.

14. The process as claimed in one of claims 1 to 13, comprising growing by epitaxy a semiconductor layer on the carrier substrate.

15. The process as claimed in one of claims 1 to 13, wherein the carrier substrate comprises at least one COP-free CZ silicon layer.

16. The process as claimed in one of claims 1 to 14, wherein the smoothing heat treatment of the first single-crystal semiconductor layer is carried out at a temperature comprised between 1000 and 1200°C, for a time comprised between 10 and 120 minutes.

17. The process as claimed in one of claims 1 to 16, furthermore comprising a heat treatment for finishing the second single-crystal semiconductor layer at a temperature comprised between 1100 and 1250°C, carried out for a time shorter than one minute.