Description

The present invention relates to a semiconductor device provided with a package.

Some proposed semiconductor devices are provided with so-called high-speed IC packages in which IC chips for inputting and outputting various signals, including high-speed signals, are mounted on a multilayer insulative substrate.

In this kind of multilayer high-speed IC package, the major portions of the signal lines which connect an IC chip at the upper part of the IC package with external terminals at the bottom part of the IC package extend vertically with respect to the IC Package.

The length of the vertical portions of the signal lines increase when there are multiple layers of insulative substrates of the IC package and along with the increased thickness of the insulative substrate.

Explaining the thickness of the insulative substrate in more detail, usually, for the purpose of decreasing the load at the driving side for driving the IC chip, it is necessary to increase the characteristic impedance of the signal lines connected to the IC chip. Accordingly, it is necessary to increase the thickness of the insulative substrate, that is, the thickness of the insulative layers positioned at the two sides of the interlayer portions of the signal lines. That is, for the purpose of making the interlayer portions of the signal lines match the characteristic impedance of the signal lines, it is necessary that, when, for example, the interlayer portions are constructed as balanced strip lines (lines in which a ground surface is provided via insulative layers of predetermined thickness and predetermined dielectric constant for both sides of the interlayer portions), the thickness of the insulative layers at the two sides be tripled (for example, the thickness of the insulative plates at the two sides of the interlayer portions be made 1 mm, respectively) to increase the characteristic impedance of the interlayer portions, for example, from 50 to 75 ohms.

In such a case, the transmission length of the vertical portions increases considerably. No particular techniques have so far been applied regarding the impedance characteristics of the vertical transmission lines.

With some of the signal lines connected to the IC chip, particularly, for example, high-speed signal lines, which may have bit rates of as high as a gigabit per second region, the increase of the vertical transmission gradually results in a nonnegligible impedance mismatching.

Further, in some types of semiconductor device, such as the above type, crosstalk occurs between adjacent signals input and output through adjacently arranged signal terminals. This becomes especially serious when the frequency of the signals becomes high, causing undesirable disturbances in the signal waveforms and oscillation (especially in amplifier circuits).

WO 84/01470 discloses a leadless chip carrier for logic components having a multilayer insulative substrate. Semi-cylindrical castellations are formed down the side of the carrier, and portions of these castellations are metallized to provide vertical conductors, some of which are connected to ground lines and others to signal lines. The castellations and consequently the conductors have a predetermined spacing such as 50, 40 or 25 mils. There is no attempt to match the impedance of the vertical conductors to other conducting lines of the carrier.

According to the present invention, there is provided a semiconductor device comprising:

a package;

a chip provided within the package;

a plurality of external terminals extending from the package;

a plurality of signal lines for connection of the chip to respective ones of said external terminals; and a plurality of ground surfaces for connection to a ground potential, wherein

the package comprises a plurality of insulating layers stacked one on another,

the chip is located in an upper part of the package and the external terminals are provided at a bottom part of the package, and

at least one of said signal lines is a high-speed signal line having a portion formed in the package, said portion being impedance matched, and characterised in that,

said ground surfaces are formed as flat ground surfaces on a flat side surface of the package, and in that

a flat side portion of said high speed signal line connected to said portion formed in the package, is formed on said flat side surface, and arranged between and coplanar with two said flat ground surfaces in such a way that a impedance-matched coplanar waveguide is formed.

An embodiment of the present invention may provide a semiconductor device in which the transmission characteristics of high-speed signals can be improved.

An embodiment of the present invention may provide a semiconductor device in which crosstalk between adjacent signals can be eliminated.

Reference is made, by way of example, to the accompanying drawings in which:

Figure 1 is a sectional view of an example of a semiconductor device of a multilayer type;

Figure 2 is a side view from the left of the semiconductor device shown in Figure 1;

Figure 3 is a perspective view of one embodi-

ment of a semiconductor device according to the present invention;

Figure 4 is a perspective view of an embodiment of a semiconductor device according to the present invention;

Figure 5 is a sectional view of the semiconductor device shown in Figure 4;

Figure 6 is a side view from the right of the semiconductor device shown in Figure 5;

Figure 7 is a side view from the left of the semiconductor device shown in Figure 5;

Figure 8 is a plan view of another example of semiconductor device;

Figure 9 is a plan view of a semiconductor device not in accordance with the present invention;

Figure 10 is a sectional view of the semiconductor device shown in Fig. 9; and

Fig. 11 is a plan view of another semiconductor device not in accordance with the present invention.

A semiconductor device with a high-speed IC package is shown in Figs. 1 and 2. This device is not prior art but is a result of in-house development by the applicant.

In Figs. 1 and 2, 10 is an IC package, 11, 12, 13 ... insulative substrates (for example, ceramic plates) superposed on each other, and 7 an IC chip.

The IC chip is connected to high-speed signal lines (for example, high-speed signal lines with a bit rate on a gigabit per second order), low-speed signal lines (for example, control signal lines on a kHz to MHz order), ground lines, and power supply lines. These lines are formed on or in the IC package and connected to corresponding external terminals provided at the lower part of the IC package.

In Fig. 1, for example, a high-speed signal line for connecting an external terminal 211 and an IC chip 7 comprises a side surface portion 212 on a side surface of the IC package 10, an interlayer portion 213 provided between insulative substrates (for example, between insulative plates 12 and 13), and a portion 214 of wire and via holes (through holes) 111, 121 of the insulative plates (for example, insulative plates 11 and 12). Further, a ground line for connecting an external terminal 491 and the IC chip 7 comprises a side surface portion 492, an interlayer portion 493 (for example between the insulative plates 11 and 12), and a portion 494 of wire and via hole of an insulative substrate (for example, an insulative substrate 11). Further, a low-speed signal line and a power supply line for connection with the IC chip are similarly formed.

As mentioned above, the insulative substrate 11, 12, 13 ... are formed in a multilayer manner, the areas between the insulative substrates are used for deploying the interlayer portions mentioned above, with these being insulated from each other. Incidentally, 5 is a frame body enclosing the IC chip 7, 6 a cap, 8 a printed circuit board on which the IC package 10 is placed, and 80 a ground surface provided on a reverse side of the printed circuit board 8.

Figure 2 shows an example of the state of connection on one side surface of the semiconductor device shown in Fig. 1. Figure 2 shows the state where the side surface portion 212 of the high-speed signal line and the side surface portions 312 and 322 of the low-speed signal lines, etc. are arranged at predetermined intervals. Further, in Fig. 2, 311 and 321 show the external terminals of the low-speed signal lines 312, 322, and 313 and 323 the interlayer portions of the low-speed signal lines. Figure 2 thus shows an example where the interlayer portion 213 of the high-speed signal line and the interlayer portions 313 and 323 of the low-speed signal lines are between the same insulation substrates.

Figures 3 to 7 show the construction of a semiconductor device with a high-speed IC package 1 according to one embodiment of the present invention. In Figs. 3 to 7, portions corresponding to the art shown in Figs. 1 and 2 bear the same reference numerals.

In Fig. 3, "a" shows a surface on which elements such as the IC chip 7 are mounted, "b", "d", and "f" ground layers, "c" a high-speed signal layer, "e" a low-speed signal layer, "g" a printed circuit board, "h" a stud, and "i" a screw. A characteristic feature of this embodiment is to provide ground surfaces 442 and 452 on the two sides of the high-speed signal lines 213', 223',... so as to form a coplanar waveguide.

Also, in Figs. 3 to 7, 11, 12, 13 ... are insulative substrates superposed on each other, one or more IC chips 7 being mounted thereon.

High-speed signal lines, low-speed signal lines, a ground line and a power supply line are connected to the IC chip. These lines are connected to the corresponding external terminals provided at the bottom of the package. In the embodiment shown in the drawings, low-speed signal lines are provided on one side surface of the package (refer especially to Fig. 6), and high speed signal lines are provided on the other side surface (refer especially Fig. 7). Of course, it is understood that these signal lines, the ground line, and the power supply line may be provided on four side surfaces of the package in accordance with a predetermined order.

The high-speed signal lines for connecting the external terminals 211, 221 ... and the IC chip 7 are formed by side surface portions 212, 222, ... provided on the side surface of the package 1; interlayer portions 213, 223, ... provided between the

insulative substrates (such as between the insulative plates 12 and 13); and portions 214, ... running through via holes 111, 121, ... of the insulative substrate (for example, the insulative plates 11 and 12). Further, the ground lines for connecting external terminals 411, 421, 431, 441, 451, ... and the IC chip 7 are formed by side surface portions 412, 422, 432, 442, 452, ...; interlayer portions 443, ... (for example, between the insulative substrates 11 and 12 in Fig. 5) connected to one of the side surface portions (for example, 442); and portions 444, ... provided through via holes of the insulative substrate. In embodiments of the present invention, it is essential to provide side surface portions of ground lines (in the embodiment mentioned above, the side surface portions 412, 422, and 432) at predetermined distances at both sides of the side surface portions 212, 222, ... of the high-speed signal lines.

Further, in the above embodiment, the side surface portions 412, 422, 432, 442, 452, ... of the ground lines provided on the side surfaces on the four sides of the package 1 are connected to the cap 6 at the top of the package. The potential of the cap 6 is made the ground potential so as to shield the internal circuits from an external electromagnetic field and thus ensure stable operation of the circuit.

Low-speed signal lines for connecting external terminals 311, 321, ... and the IC chip are also formed by side surface portions 312, 322 and interlayer portions 313, 323, shown in Fig. 6 and in right side of Fig. 4. The power supply line is similarly formed. Further, 5 shows a frame body, 8 a printed circuit board on which the IC package 1 is mounted, and 80 a ground layer which is provided on the reverse side of the printed circuit board 8.

In the construction mentioned above, some important points are that the high-speed signal lines for connecting the IC chip provided at the top of the IC package and the external terminals provided at the bottom of the IC package are connected along the side surface of the package (corresponding to the side surface portions 212, 222 in the above-mentioned embodiment); that ground layers are provided at predetermined distances at the two sides of the side surface portions 212, 222 (the side surface portions 412, 422, and 432 in the above-mentioned embodiment), and that the high-speed signal lines 212, 222 provided on the side surface and ground lines 412, 422, 432 provided at the two sides of the high-speed signal lines form coplaner waveguides respectively, whereby impedance matching of vertical portions 212, 222 of the high-speed signal lines is effected.

If the characteristic impedance of the high-speed signal lines is 50 ohms, the vertical portions 212, 223' are matched to this characteristic impedance, and if the dielectric constant (that is, the dielectric constant of the insulative layer between the high-speed signal lines and the ground surfaces provided at the two sides of the high-speed signal lines) of the insulative substrate (usually formed by a ceramic plate) is 10, the ratio (d/D) between the size D shown in Fig. 4 (the distance between a center of a high-speed signal line and the ground surfaces) and the size d (the distance between a center of the high-speed signal line and the edge portion thereof) is set to about 0.53 (as one example, D is 755 μm and d is 400 μm). Further, when the characteristic impedance is decreased further, the ratio d/D is increased in accordance with it.

In this case, by providing most of the part of the vertical portions of the high-speed signal lines along the side surface of the package (that is, positioning the interlayer portions as high as possible), it is possible to obtain almost a perfect match of the impedance of the vertical portions without giving special consideration to the impedance characteristics of the remainder of the vertical portions (that is, a mainly portion passing through the via hole of the insulative substrate).

Further, in the embodiment shown in the drawings, ground lines are provided not only at the two sides of the side surface portions of the high-speed signal lines (as the side surface portions 412, 422, 432), but also, for example, as the side surface portions 442, 452, in Fig. 6. It is preferable to connect the ground lines provided on the sides of the package to the cap 6.

Further, in the embodiment mentioned above, ground surfaces 110 and 130 are formed, between insulative layers having a predetermined thickness (insulative plates 12, 13 having a predetermined thickness in the embodiment shown in Fig. 5), at the upper side and lower side of the interlayer portions 213 of the high-speed signal lines. The interlayer portion 213 and the ground surfaces 110 and 130 form a balanced strip line, enabling impedance matching of the interlayer portions 213 too. Further, in Fig. 5, the ground surface 110 is between the insulative plates 11 and 12 (except for the portion of the via hole passing through the portions 214, etc.). On the other hand, the ground surface 130 is provided between the insulative plate 13 and the insulative plate provided thereunder.

Further, each printed circuit (wiring) provided on the printed circuit board 8 connected to each external terminal under the IC package forms together with the ground surface on the reverse of the printed circuit board a micro-strip line as a transmission line.

As detailedly mentioned above, impedance

matching of the vertical portions of the high-speed signal lines in a multilayer high-speed IC package can be easily obtained, so the transmission characteristic of high-speed signals can be improved and deterioration of the signal wave form and S/N ratio can be prevented.

Figure 8 is a plan view of a previously proposed semiconductor device. An insulative substrate 12 in the IC package 1 mounted on a printed circuit board has one or more IC chips 7 mounted at the center thereof. At the peripheral portion, various terminals, that is, signal terminals (input terminals and output terminals), ground terminals, and power supply terminals are suitably provided from inside the package 1 (above the insulative substrate 12) to the external portion thereof (above printed circuit board 2) by, for example, plating or thin film conductive materials. In Fig. 8, these terminals are shown by symbols 511, 512, 513, 514, ... These terminals on the printed circuit board 2 are connected to printed circuits for corresponding signal transmission lines (usually, the printed circuit forms a micro-strip line as a transmission line together with the ground metal surface provided on the reverse surface of the printed circuit) 611, 612, 613, 614, ... Further, 531, 532, ... are pads provided on an IC chip 7, and 16 is a line for connecting the pads 531, 532, ... and terminals corresponding to these pads.

In this semiconductor device, the impedance of the terminal portions of the IC package does not sufficiently match with signal lines connected to the terminals. Therefore, when the frequency of the transmitted signal increases so that the level thereof rapidly changes (so-called high-speed signal), there is a problem of a significant impedance mismatching at the signal terminals.

Conceivably, the signal terminal portions may be formed as a micro-strip line to obtain an impedance matching. Formation of the micro-strip line necessitates provision of a ground surface on the insulative substrate opposing the signal terminals. Thus, the insulative substrate of the package must be formed as a two-layer construction, making the construction complicated.

Further, in the above-mentioned semiconductor device, crosstalk occurs between adjacent signals input and output via adjacently arranged signal terminals. This becomes especially serious when the frequency of the signals become high, causing undesirable disturbance in the signal waveforms and oscillation (especially in amplifier circuits).

Figures 9 and 10 show another semiconductor device. The insulative substrate 12 on the IC package 1 mounted on the printed circuit board 2 has one or more IC chips 7 provided at the center portion thereof. At the peripheral portion, many signal lines or terminals (input terminals and output terminals) 511, 512, ... are provided from the internal portion of the package 1 (above insulative substrate 12) to the external terminal portion (on the printed circuit board 2). On the printed circuit board 2, these terminals are connected to the corresponding printed circuits 611, 612, ... for the signal transmission. Here, the printed circuits 611, 612, ... usually form a micro-strip line as the transmission line together with the ground metal surface 30 provided on the reverse of the printed circuit board. Further, 531, 532, ... are pads provided on the IC chip 7, and 16 are wires for connecting the pads 531, 532, ... and the terminal corresponding to these pads.

Ground terminals 501, 502, 503, ... are provided at predetermined distances at the two sides of the signal terminals 511, 512, ... The signal terminals 511, 512, ... and the ground terminals 501, 502, 503, ... (for example, signal terminals 511 and ground terminals 501, 502) form a coplaner waveguide. This enables impedance matching for the signal lines connected to the signal terminals 511, 512, ... (that is, the transmission line formed as a microstrip line on the printed circuit board). In the embodiment shown in Fig. 9, a metal plate 10 is formed (within or on the underside of the package) so as to connect the ground terminals mentioned above, and the IC chip 7 is mounted on the metal plate 10 (refer to Fig. 10).

In this type of device, the signal terminals provided on the IC package form coplaner waveguide together with the ground terminals provided at the two ends, (sides) of the signal terminals, enabling an impedance match for the signal lines connected to the signal terminals (usually formed as microstrip line). The impedance of the coplaner waveguide is determined by the width of the signal terminals, the distance between the signal terminals and the ground terminals, and the dielectric constant of material between the signal terminals and the ground terminals.

Further, the ground terminals 501, 502, 503, ... are formed along the two sides of the signal terminals from the internal portion (above the insulative substrate 12) of the package to the external portion thereof (on the printed circuit board) and are connected to printed circuits 601, 602, 603, ... on the printed circuit board 2. The printed circuits 601, 602, 603, ... are connected to the ground side by connection, for example, via through holes provided in the printed circuit board 2, to the ground metal surface 30 on the reverse surface of the printed circuit board 2. Further those of the IC pads (for example, 533 in Fig. 9) to be connected to the ground terminals are connected to any one of the many ground terminals.

According to this type of device, impedance matching of the signal terminal portion provided on

the IC package can be obtained with a simple construction. Further, crosstalk between the signals transmitted via adjacent signal terminals may be completely prevented by providing ground terminals between adjacent signal terminals. Further, in the IC package shown in the drawings, lines for connecting the signal terminals and IC package exist, however, their impedance characteristics can usually be ignored. If necessary, instead of the line connection, the signal terminals may be directly connected to the IC chip.

Fig. 11 shows a modified version of the semiconductor device shown in Fig. 9. The portion for connecting the ground terminals 501, 502, 503, ... is formed as a metal frame 10' instead of the metal plate 10 shown in Fig. 9. Further, in Fig. 11, the signal terminal 513 is provided with a ground terminal only at the right side, therefore, no coplaner waveguide mentioned above is formed. Therefore, in this signal terminal, a signal for which it is not necessary to consider the impedance matching of the signal terminal portion, for example, a signal which has a low frequency, should be input and output.

According to the above embodiment of the present invention, impedance matching of a signal terminal portion (vertical or horizontal) in the IC package can be easily achieved. Therefore, the transmission characteristics of high-speed signals can be improved, deterioration of signal waveform and S/N ratio can be prevented, and crosstalk between adjacent signals can be completely prevented.

Claims

1. A semiconductor device comprising:
   a package (1);
   a chip (7) provided within the package (1);
   a plurality of external terminals (211, 223, ...) extending from the package (1);
   a plurality of signal lines (212, 231, ...) for connection of the chip (7) to respective ones of said external terminals (211, 221, ...); and a plurality of ground surfaces (412, 422, ...) for connection to a ground potential, wherein
   the package comprises a plurality of insulating layers (11, 12, 13, ...) stacked one on another,
   the chip (7) is located in an upper part of the package (1) and the external terminals are provided at a bottom part of the package, and
   at least one of said signal lines is a high-speed signal line having a portion (213) formed in the package, said portion being impedance matched, and characterised in that,
   said ground surfaces are formed as flat ground surfaces on a flat side surface of the package, and in that
   a flat side portion (212, ...) of said high speed signal line connected to said portion (213) formed in the package, is formed on said flat side surface, and arranged between and coplanar with two said flat ground surfaces in such a way that a impedance-matched coplanar waveguide is formed.

2. A semiconductor device as claimed in claim 1, wherein a ratio d/D for the coplanar waveguide is set to match the characteristic impedance of the high speed signal line (212, 213, ...), where d is half the width of the flat side portion (212) of the high speed signal line, and D is the distance between the centre of the flat side portion (212) of the high speed signal line and an adjacent edge of one of the flat ground surfaces (412, 422, ...), the dielectric constant of the material of the flat side surface of the package (1) also being taken into account.

3. A semiconductor device as claimed in claim 2, wherein the characteristic impedance is about 50 ohms, the dielectric constant is 10, and the ratio d/D is set to about 0.53.

Revendications

1. Dispositif semi- conducteur comprenant :
   un boîtier (1) ;
   un pavé semi- conducteur ou puce (7) disposé à l'intérieur du boitier (1) ;
   une pluralité de bornes externes (211, 221, ...) s'étendant depuis le boîtier (1) ;
   une pluralité de lignes de signal (212, 231, ...) pour la connexion de la puce (7) à celles respectives des dites bornes externes (211, 221,...); et une pluralité de surfaces de masse (412, 422) pour la connexion à un potentiel de masse, dans lequel
   le boîtier comprend une pluralité de couches isolantes (11, 12, 13, ...) empilées les unes sur les autres,
   la puce (7) est placée sur une partie supérieure du boîtier (1) et les bornes externes sont disposées sur une partie formant le fond du boîtier, et
   au moins une des dites lignes de signal est une ligne de signal haute vitesse présentant une partie (213) formée dans le boîtier, la dite partie étant adaptée en impédance, dispositif caractérisé en ce que,
   les dites surfaces de masse sont fabriquées sous forme de surfaces de masse planes sur une surface de côté plan du boîtier, et en ce que
   une partie de côté plan (212, ...) de la dite

the IC package can be obtained with a simple construction. Further, crosstalk between the signals transmitted via adjacent signal terminals may be completely prevented by providing ground terminals between adjacent signal terminals. Further, in the IC package shown in the drawings, lines for connecting the signal terminals and IC package exist, however, their impedance characteristics can usually be ignored. If necessary, instead of the line connection, the signal terminals may be directly connected to the IC chip.

Fig. 11 shows a modified version of the semiconductor device shown in Fig. 9. The portion for connecting the ground terminals 501, 502, 503, ... is formed as a metal frame 10' instead of the metal plate 10 shown in Fig. 9. Further, in Fig. 11, the signal terminal 513 is provided with a ground terminal only at the right side, therefore, no coplaner waveguide mentioned above is formed. Therefore, in this signal terminal, a signal for which it is not necessary to consider the impedance matching of the signal terminal portion, for example, a signal which has a low frequency, should be input and output.

According to the above embodiment of the present invention, impedance matching of a signal terminal portion (vertical or horizontal) in the IC package can be easily achieved. Therefore, the transmission characteristics of high-speed signals can be improved, deterioration of signal waveform and S/N ratio can be prevented, and crosstalk between adjacent signals can be completely prevented.

Claims

1. A semiconductor device comprising:
   a package (1);
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   a plurality of signal lines (212, 231, ...) for connection of the chip (7) to respective ones of said external terminals (211, 221, ...); and a plurality of ground surfaces (412, 422, ...) for connection to a ground potential, wherein
   the package comprises a plurality of insulating layers (11, 12, 13, ...) stacked one on another,
   the chip (7) is located in an upper part of the package (1) and the external terminals are provided at a bottom part of the package, and
   at least one of said signal lines is a high-speed signal line having a portion (213) formed in the package, said portion being impedance matched, and characterised in that,
   said ground surfaces are formed as flat ground surfaces on a flat side surface of the package, and in that
   a flat side portion (212, ...) of said high speed signal line connected to said portion (213) formed in the package, is formed on said flat side surface, and arranged between and coplanar with two said flat ground surfaces in such a way that a impedance-matched coplanar waveguide is formed.

2. A semiconductor device as claimed in claim 1, wherein a ratio d/D for the coplanar waveguide is set to match the characteristic impedance of the high speed signal line (212, 213, ...), where d is half the width of the flat side portion (212) of the high speed signal line, and D is the distance between the centre of the flat side portion (212) of the high speed signal line and an adjacent edge of one of the flat ground surfaces (412, 422, ...), the dielectric constant of the material of the flat side surface of the package (1) also being taken into account.

3. A semiconductor device as claimed in claim 2, wherein the characteristic impedance is about 50 ohms, the dielectric constant is 10, and the ratio d/D is set to about 0.53.

Revendications

1. Dispositif semi- conducteur comprenant :
   un boîtier (1) ;
   un pavé semi- conducteur ou puce (7) disposé à l'intérieur du boitier (1) ;
   une pluralité de bornes externes (211, 221, ...) s'étendant depuis le boîtier (1) ;
   une pluralité de lignes de signal (212, 231, ...) pour la connexion de la puce (7) à celles respectives des dites bornes externes (211, 221,...); et une pluralité de surfaces de masse (412, 422) pour la connexion à un potentiel de masse, dans lequel
   le boîtier comprend une pluralité de couches isolantes (11, 12, 13, ...) empilées les unes sur les autres,
   la puce (7) est placée sur une partie supérieure du boîtier (1) et les bornes externes sont disposées sur une partie formant le fond du boîtier, et
   au moins une des dites lignes de signal est une ligne de signal haute vitesse présentant une partie (213) formée dans le boîtier, la dite partie étant adaptée en impédance, dispositif caractérisé en ce que,
   les dites surfaces de masse sont fabriquées sous forme de surfaces de masse planes sur une surface de côté plan du boîtier, et en ce que
   une partie de côté plan (212, ...) de la dite

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ligne de signal haute vitesse connectée à la dite partie (213), formée dans le boîtier, est formée sur la dite surface de côté plan, et disposée entre les deux dites surfaces de masse plane et de façon co- planaire, d'une manière telle qu'un guide d'onde co- planaire adapté en impédance soit formé.

2. Dispositif semi- conducteur tel que revendiqué à la revendication 1, dans lequel un rapport d/ D pour le guide d'onde coplanaire est choisi de façon à adapter l'impédance caractéristique de la ligne de signal haute vitesse (212, 213, ...), où d est la moitié de la largeur de la partie de côté plan (212) de la ligne de signal haute vitesse, et D est la distance entre le centre de la partie de côté plan (212) de la ligne de signal haute vitesse, et un bord adjacent de l'une des surfaces de masse plane (412, 422, ...), la constante diélectrique du matériau à la surface de côté plane du boîtier (1) etant aussi prise en compte.

3. Dispositif semi- conducteur tel que revendiqué à la revendication 2, dans lequel l'impédance caractéristique est environ de 50 Ohms, la constante diélectrique est de 10, et le rapport d/ D est sélectionné à environ 0,53.

Patentansprüche

1. Halbleitervorrichtung mit:
einer Packung (1);
einem Chip (7), das innerhalb der Packung (1) vorgesehen ist;
einer Vielzahl von externen Anschlüssen (211, 221, ...), die sich von der Packung (1) aus erstrecken;
einer Vielzahl von Signalleitungen (212, 231, ...), zum Verbinden des Chip (7) mit entsprechenden der genannten externen Anschlüsse (211, 221, ...); und einer Vielzahl von Erdungsoberflächen (412, 422, ...), zum Verbinden mit einem Erdpotential, bei der
die Packung eine Vielzahl von isolierenden Schichten (11, 12, 13, ...) umfaßt, die eine auf der anderen gestapelt sind,
wobei das Chip (7) in einem oberen Teil der Packung (1) angeordnet ist und in die externen Anschlüsse an dem Bodenteil der Packung vorgesehen sind, und
wenigstens eine der genannten Signalleitungen eine Hochgeschwindigkeits-Signalleitung ist, die einen in der Packung gebildeten Abschnitt (213) hat, welcher Abschnitt in seiner Impedanz angepaßt ist, und dadurch gekennzeichnet, daß
die genannten Erdungsoberflächen als flache Erdungsoberflächen auf einer flachen Seitenoberfläche der Packung vorgesehen sind, und daß
ein flacher Seitenabschnitt (212, ...) der genannten Hochgeschwindigkeits-Signalleitung, der mit dem in der Packung gebildeten genannten Abschnitt (213) verbunden ist, auf der genannten flachen Seitenoberfläche und zwischen und koplanar mit zwei genannten flachen Erdungsoberflächen in solch einer Weise angeordnet ist, daß ein in der Impedanz angepaßter koplanarer Wellenleiter gebildet ist.

2. Halbleitervorrichtung nach Anspruch 1, bei dem das Verhältnis d/D für den koplanaren Wellenleiter so gesetzt ist, daß die Wellenwiderstand der Hochgeschwindigkeits-Signalleitung (212, 213, ...) angepaßt ist, wobei d die halbe Breite des flachen Seitenabschnitts (212) der Hochgeschwindigkeits-Signalleitung ist, und D der Abstand zwischen dem Zentrum des flachen Seitenabschnitts (212) der Hochgeschwindigkeits-Signalleitung und einem benachbarten Rand von einer der flachen Erdungsoberflächen (412, 422, ...) ist, wobei die Dielektrizitätskonstante des Materials der flachen Seitenoberfläche der Packung (1) ebenfalls berücksichtigt wird.

3. Halbleitervorrichtung nach Anspruch 2, bei der die charakteristische Impedanz etwa 50 Ohm, die Dielektrizitätskonstante 10 ist, und das Verhältnis d/D auf etwa 0,53 gesetzt ist.

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