CLAIMS

1. A transistor comprising a source, a body and a drain, the transistor further comprising

a plurality of semiconductor layers, wherein layers of the plurality of semiconductor layers are made of AlGaN with an aluminum content of 0% or higher, and wherein the plurality of semiconductor layers is configured such that an aluminum content changes between each consecutive layer such that every other layer has a lower aluminum content than the neighboring mutually opposite layers thereof, wherein the transistor is either

a N-channel metal–oxide–semiconductor, NMOS, transistor, wherein part of the plurality of semiconductor layers is p-doped and forms part of the body of the NMOS transistor; or

a P-channel metal–oxide–semiconductor, PMOS, transistor, wherein part of the plurality of semiconductor layers is p-doped and forms part of the source or the drain of the PMOS transistor.

2. The transistor according to claim 1, wherein the plurality of semiconductor layers comprises a repetition of a pair of semiconductor layers, wherein each pair of semiconductor layers comprises

a low Al content layer, having an Al content below 10%; and

a high Al content layer, having an Al content above 15%.

3. The transistor according to claim 1 or 2, wherein each layer, of the plurality of semiconductor layers, has a thickness between 3 nm and 10 nm.

4. The transistor according to any one of claims 1-3, wherein the transistor is configured to pass a current in a direction parallel to the layers of the plurality of semiconductor layers.

5. The transistor according to any one of claims 1-3, wherein the transistor is configured to pass a current in a direction orthogonal to the layers of the plurality of semiconductor layers.

6. The transistor according to claim 5, wherein a nanowire confines at least part of the body of the transistor.

7. The transistor according to claim 6, wherein a gate contact wraps around the nanowire that confines at least part of the body of the transistor, whereby the gate contact forms a wrap-around gate.

8. The transistor according to claim 6 or 7, wherein the nanowire that confines at least part of the body of the transistor also confines at least part of the source and the drain of the transistor.

9. The transistor according to any one of the preceding claims, wherein the source, the drain, and the body of the transistor all comprise the plurality of semiconductor layers.

10. The transistor according to any one of the preceding claims, wherein the transistor is a NMOS transistor, wherein

the source comprises a n-doped GaN layer; and

the drain comprises a n-doped GaN layer.

11. An electrical device comprising:

at least one N-channel metal–oxide–semiconductor, NMOS, transistor, the at least one NMOS transistor comprising a plurality of NMOS semiconductor layers, wherein each layer of the plurality of NMOS semiconductor layers of the NMOS transistor is made of AlGaN with an aluminum content of 0% or higher, and wherein the plurality of NMOS semiconductor layers of the NMOS transistor is configured such that an aluminum content changes between each consecutive layer such that every other layer has a lower aluminum content than the neighboring mutually opposite layers thereof, wherein the plurality of NMOS semiconductor layers of the NMOS transistor forms part of a p-doped body of the NMOS transistor; and

at least one a P-channel metal–oxide–semiconductor, PMOS, transistor, the at least one PMOS transistor comprising a plurality of PMOS semiconductor layers, wherein each layer of the plurality of PMOS semiconductor layers of the PMOS transistor is made of AlGaN with an aluminum content of 0% or higher, and wherein the plurality of PMOS semiconductor layers of the PMOS transistor is configured such that an aluminum content changes between each consecutive layer such that every other layer has a lower aluminum content than the neighboring mutually

opposite layers thereof, wherein the plurality of PMOS semiconductor layers of the PMOS transistor forms part of a p-doped source or drain of the PMOS transistor,

wherein the at least one NMOS transistor and the at least one PMOS transistor of the electrical device are connected to form a complementary metal–oxide–semiconductor, CMOS, circuit.

12. The electrical device according to claim 11, wherein the at least one NMOS transistor and the at least one PMOS transistor of the CMOS circuit share the same plurality of semiconductor layers.

13. The electrical device according to claim 11 or 12, wherein at least one of the at least one PMOS transistor and/or at least one of the at least one NMOS transistor of the CMOS circuit of the electrical device is a transistor according to any one of claims 2-10.

14. A method for producing a transistor, said method comprising;

epitaxially growing a first n-doped layer of AlGaN with an aluminum content of 0% or higher;

epitaxially growing a plurality of semiconductor layers, wherein the plurality of semiconductor layers is grown on top of the first n-doped layer, wherein each layer of the plurality of semiconductor layers is made of AlGaN with an aluminum content of 0% or higher, and wherein the plurality of semiconductor layers is configured such that an aluminum content changes between each consecutive layer such that every other layer has a lower aluminum content than the neighboring mutually opposite layers thereof, wherein the plurality of semiconductor layers is grown p-doped;

epitaxially growing a second n-doped layer of AlGaN with an aluminum content of 0% or higher, wherein the second n-doped layer is grown on top of the plurality of semiconductor layers; whereby the first n-doped layer, the plurality of semiconductor layers, and the second n-doped layer form part of a semiconductor structure, the method further comprising:

electrically connecting one of the first and second n-doped layers to a source contact and the other of the first and second n-doped layers to a drain contact, whereby a transistor source and a transistor drain are formed by the first and second n-doped layers;

arranging a gate contact on the semiconductor structure, the gate

contact being configured to apply an electric field to the plurality of semiconductor layers, such that an electrical conduction between the transistor source and the transistor drain, via the plurality of semiconductor layers, is controllable by the gate contact, whereby a transistor body is formed by the plurality of semiconductor layers.

15. The method according to claim 14, further comprising

etching out a nanowire from the plurality of semiconductor layers.