A METHOD OF FORMING DUAL THICKNESS GATE DIELECTRIC STRUCTURES VIA USE OF SILICON NITRIDE LAYERS

ABSTRACT

A process for forming a first group of gate structures, designed to operate at a lower voltage than a simultaneously formed second group of gate structures, has been developed. The process features the thermal growth of a first silicon dioxide gate insulator layer, on a portion of the semiconductor substrate used for the lower voltage gate structures, while simultaneously forming a thicker, second silicon dioxide gate insulator layer on a portion of the semiconductor substrate used for the higher voltage gate structures. The thermal growth of the first, and second silicon dioxide gate insulator layers is accomplished via diffusion of the oxidizing species: through a thick, composite silicon nitride layer, to obtain the thinner, first silicon dioxide gate insulator layer, on a first portion of the semiconductor substrate; and through a thinner, silicon nitride layer, to obtain the thicker, second silicon dioxide gate insulator layer, on a second portion of the semiconductor substrate.

Fig. 5