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(54) IMPROVEMENTS IN AND RELATING TO SEMICONDUCTOR DEVICES

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to semiconductor devices particularly, but not exclusively, integrated semiconductor devices, and to methods of manufacturing semiconductor devices.

15 In United Kingdom Patent Specification No. 1,208,574 there is described the manufacture of a semiconductor device comprising a semiconductor body including a transistor, a pattern of an insulating material being inset in the semiconductor body and extending from a main surface of the semiconductor body in said body over at least a part of its thickness, the semiconductor body having a layer-shaped part which adjoins the main surface and which, along its full perimeter and throughout its thickness, adjoins a first part of the inset pattern, in said layer-shaped part the base zone of the transistor adjoins the main surface and, along its full perimeter adjoins, the said part of the pattern, the emitter zone of the transistor being provided in the base zone and adjoining the main surface, and the collector zone comprising a part which is present below the base zone.

35 A semiconductor device including a transistor and having such a structure has various advantages.

40 The collector-base junction does not terminate *via* a strong curve near its edge substantially perpendicular to the main surface but, while avoiding said curve, said junction is laterally bounded by the pattern of inset insulating material and this

has a favourable influence on the electrical properties of the transistor. Moreover, the inset pattern enables the use of a combination of thick and thin insulating layers with their respective advantages.

The collector contact of such a transistor having an inset pattern is provided on the lower side of the semiconductor body, the base and emitter zones being contacted on the upper side of the semiconductor body. For a number of applications, in particular for use in an integrated semiconductor device, it is desirable, however, for the collector zone to be contacted on the upper side of the semiconductor body. For that purpose, an aperture can be provided in the inset insulating layer beside the base zone and the collector zone can be contacted *via* said aperture.

This form of contacting, however, has several drawbacks. The accuracy associated with the provision of an aperture in a thick insulating layer is not high. As is known, apertures can be made in an insulating layer the more accurately the smaller the thickness of the insulating layer. Furthermore, a connection contact which is connected to a semiconductor zone *via* an aperture in an insulating layer usually consists of a metal layer which is provided in the aperture and which extends also over the insulating layer. The possibility of damage, for example in the form of hair-line cracks, of such a metal layer on the edge of an aperture in a thick insulating layer is undesirably large. Moreover, the distance between such an aperture for the collector contact and the base zone must be chosen to be larger than the minimum permissible distance, since tolerances in the determination of the location of the aperture to be provided have to be taken into account, and this means that the transistor has to be provided occupying more space than would be necessary if it were

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possible to obtain a more exact determination of the location of said aperture relative to the base zone.

According to the invention in a semiconductor device comprising a semiconductor body including a transistor, a pattern of insulating material is inset in the semiconductor body and extending in said body from a main surface thereof over at least a part of its thickness, the semiconductor body having a first layer-shaped part and a simultaneously provided second layer-shaped part situated beside and spaced from the first layer-shaped part, said first layer-shaped part adjoining the main surface and, along its full perimeter and throughout its thickness, adjoining a first part of the inset pattern, said second layer-shaped part adjoining the main surface and adjoining, along at least a part of its perimeter and throughout its thickness, a second part of the pattern, in said first layer-shaped part the base zone of the transistor adjoining the main surface and, along its full perimeter, adjoining the first part of the pattern, the emitter zone of the transistor being provided in the base zone and adjoining the main surface, and the collector zone comprising a part which is present below the base zone, said second layer-shaped part comprising a connection part of the collector zone which connection part adjoins the main surface and is separated from the first layer-shaped part only by a separation part belonging to at least one of the two said parts of the pattern, said connection part and the part of the collector zone below the base zone being interconnected by an interconnection part of the collector zone present at least partly below the separation part of the inset insulating pattern.

Since the connection part of the collector zone is present beside the inset pattern, as is also the base zone, instead of being present below the inset pattern, the collector zone may be contacted *via* said connection part, while avoiding the provision of an aperture in the pattern. Furthermore, the location of the base zone as well as that of the connection part of the collector zone are determined by the inset pattern. This means that during the manufacture of the semiconductor device the location of the base zone and that of the connection part are determined by the same mask, namely the mask by means of which the inset pattern is provided, and therefore the determination of the location of the connection part relative to the base zone is accurate, and tolerances which inevitably occur when using several masks need not be taken into account.

The surfaces of the first and the second layer-shaped parts of the semiconductor body may be located substantially in the same flat plane.

During the manufacture of the semiconductor device and after the provision of the inset pattern, in which the first and the second part of said pattern are simultaneously formed, said parts have the same homogeneous thickness (viewed in a direction transverse to the main surface of the semiconductor body). If desired, differences in thickness may then be provided, for example, by a local etching treatment of the pattern. For simplicity, however, in the manufactured device the first and the second parts of the pattern may have substantially the same homogeneous thickness.

The pattern or a part thereof may be considered to have a homogeneous thickness when in cross-sections of the semiconductor body which include the pattern or the part thereof, said pattern between two juxtaposed edges of the pattern always has substantially the same thickness, although near said edges the pattern may show a different thickness.

For example, by locally etching the semiconductor body prior to providing the inset pattern, a pattern may be obtained, a part or a number of parts of which extend less deeply in the semiconductor body than another part or a number of other parts of the pattern. In relatively simple forms of the device the first and the second parts of the inset pattern may extend homogeneously substantially to the same distance from the main surface of the semiconductor body in said body.

The pattern or a part thereof may be considered to extend homogeneously substantially to a given distance from the main surface in the semiconductor body when in cross-sections of the semiconductor body which include the pattern or part thereof the pattern between two juxtaposed edges of the pattern always extends to said given distance from the main surface in the semiconductor body, although near said edges the pattern may extend to a smaller distance in the semiconductor body.

The connection part of the collector zone may comprise a highly doped contact zone in the form of a surface adjoining zone of the same conductivity type as the collector zone. The contact zone may be of the same thickness and the same doping profile as the emitter zone. Such a highly doped contact zone enables a good collector connection.

A semiconductor device in accordance with the invention may be an integrated semiconductor device comprising a plurality of circuit elements including the said transistor, such an integrated device comprising isolation zones which consist at least partly of an insulating material, the insulating material part of an isolation zone laterally surrounding the transistor and being consti-

tuted by the said first and/or the said second part of the inset pattern of insulating material.

5 In one form of such an integrated semiconductor device the semiconductor body comprises a plurality of circuit elements, including the transistor, which circuit elements are present in a number of semiconductor islands, the islands adjoining the main surface and being separated from each other by isolation zones which are formed, at least near the main surface, by insulating parts of the inset pattern which laterally surround the islands, the first and the second part of the inset pattern together constituting, in addition to the separation part, a part which surrounds the base zone and the connection part of the collector zone of the transistor collectively, said part belonging at least partly to an insulating part of an isolation zone surrounding the transistor.

15 The isolation zones may consist wholly of an insulating material, while the semiconductor body consists of a number of separate body parts constituted by the islands, in which the islands may be provided, for example on the side of the main surface, on a common support of an insulating material.

25 The semiconductor body may comprise a semiconductor support and an epitaxial layer which is present thereon and adjoins the main surface, said layer being divided by the isolation zones into parts which belong to the islands, the support comprising a substrate which is isolated from the islands by at least one $p-n$ junction. A buried layer may be used for the interconnection part of the collector zone which interconnects the connection part and the part of the collector zone present below the base zone. In one form the collector zone of the transistor forms an isolating $p-n$ junction with the substrate and comprises a part situated in the epitaxial layer, and a buried part situated in the support, the buried part partly being present below the separation part of the inset pattern and at least partly forming part of the interconnection part of the collector zone.

40 The isolation zones may consist entirely of the insulating parts of the inset pattern, the pattern being inset in the semiconductor body throughout the thickness of the epitaxial layer and the insulating parts extending to the substrate. The interconnection part of the collector zone where present below the separation part of the pattern may consist of a buried layer part provided in the support.

50 It is also possible for the insulating parts of the pattern to extend only to the near vicinity of the $p-n$ junction between the substrate and the epitaxial layer such that in operation with the normally applied poten-

65 tials the depletion region of said $p-n$ junction reaches the insulating parts.

However, in one form in which a less deeply inset pattern needs to be provided or, in other words, in which a thick epitaxial layer may be used without it being necessary to provide an unpractically deep inset pattern an isolation zone comprises a semiconductor zone which is of the same conductivity type as the substrate and is present between the insulating part of the inset pattern belonging to said isolation zone and the substrate.

70 The pattern may be provided, for example, by providing recesses in the semiconductor body and filling them with an insulating material. The inset pattern may consist of an insulating material formed by conversion of semiconductor material of the semiconductor body. If the semiconductor body consists of silicon, a pattern of silicon oxide may be obtained by local oxidation of the semiconductor body. Conversion into, for example, silicon carbide is also possible.

75 According to a further aspect of the invention in a method of manufacturing a semiconductor device in accordance with the invention there are masked against oxidation a first part and a second part of a main surface of a semiconductor body, a region of one conductivity type of said body extending below said first and second surface parts, an insulating pattern inset in the semiconductor body being provided by conversion of the non-masked parts of said main surface into insulating material so that a first layer-shaped part of the semiconductor body which, along its full perimeter and throughout its thickness, adjoins the first part of the pattern, and a second layer-shaped part of the semiconductor body which, at least along a part of its perimeter and throughout its thickness, adjoins the second part of the pattern, are obtained, said layer-shaped parts being separated from each other only by a separation part belonging to at least one of the two said parts of the pattern, the pattern being inset in the semiconductor body over such a distance from the main surface that a part of the region of one conductivity type remains present below the separation part, a base zone of the transistor being provided adjoining the first surface part and adjoining along its full perimeter the first part of the pattern, said base zone forming a $p-n$ junction with the region of one conductivity type, there being provided in the base zone an emitter zone of the transistor adjoining the first surface part, at least a part of the region of one conductivity type partly being present below the separation part and below the base zone and constituting the collector zone of the transistor.

In one form of the method in which an integrated semiconductor device is formed, a semiconductor body is used the region of one conductivity type of which adjoins the whole main surface and is isolated from a substrate of the opposite conductivity type present below the region by a $p-n$ junction, the region is divided into juxtaposed islands which are separated from each other by providing in the region isolation zones which, at least near the main surface, consist of parts of an insulating material, and which isolation zones adjoin the isolation provided by the $p-n$ junction at the substrate side, the insulating material parts being provided simultaneously with and forming part of the pattern, a part of the pattern which belongs to at least one of the two parts constituted by the first and the second part of the pattern and which collectively laterally surround the base zone and the connection part of the collector zone adjoining the second surface part constituting at least a part of an insulation zone laterally surrounding the transistor. As is usual in integrated circuits with islands, a number of circuit elements, for example, transistors, diodes, resistors and capacitances, may be provided in the islands.

The semiconductor body having the region of one conductivity type can be obtained in a simple manner by starting from a semiconductor support of which at least the part adjoining one surface is of the opposite conductivity type and by providing on said surface of the support an epitaxial layer of one conductivity type belonging to the said region.

In one form prior to providing the epitaxial layer the support is provided with a surface zone of one conductivity type adjoining the said surface, the surface zone being situated so that it lies below the separation part of the inset pattern when later provided and it is laterally bounded by the isolation zone which laterally surrounds the transistor when later provided. As a result of this a low-resistivity connection part of the collector zone and a reduction of the collector series resistance can be obtained.

In a form of the method in which only an inset pattern need to be provided which extends over a part of the thickness of the epitaxial layer, in surface zones of the support adjoining the support surface, which zones are situated so that they lie below the insulating parts when later provided, the concentration of the impurities determining the opposite conductivity type is increased, after which the epitaxial layer is provided and zones of the opposite conductivity type belonging to the isolation zones and adjoining the substrate are obtained by diffusion into the epitaxial layer of impurities from said zones, the pattern being

inset in said layer only over part of the thickness of the epitaxial layer.

In another form of the method in which only an inset pattern need to be provided which extends over part of the thickness of the epitaxial layer, prior to providing the inset pattern by conversion of non-masked semiconductor material into the insulating material, impurities which cause the opposite conductivity type are provided in non-masked surface parts of the semiconductor body corresponding in surface location to the insulating parts to be provided, said impurities being diffused deeper in the semiconductor body during the provision of the pattern and constituting zones of the opposite conductivity type which are present between the insulating parts and the substrate and which belong to the isolation zones.

When during the provision of the inset pattern semiconductor material of the semiconductor body is converted into insulating material, said insulating material usually occupies a greater volume than the original semiconductor material, as a result of which a pattern is obtained which is inset in the semiconductor body over part of its thickness and projects above the semiconductor body over the remainder of its thickness. If the semiconductor body is of silicon and a pattern of silicon oxide is provided by local oxidation of the semiconductor body, a silicon oxide pattern is obtained which is inset in the semiconductor body approximately over half its thickness. In the method in accordance with the invention prior to providing the inset pattern, surface parts of the semiconductor body may be removed at the location of at least a part of the pattern to be provided, as a result of which recesses are obtained which extend from the main surface over a part of the thickness of the semiconductor body in said body, the pattern being then provided by conversion of non-masked semiconductor material into insulating material which occupies the recesses over at least a part of their depth. By first providing the recesses, a pattern may be obtained which is inset over a very large part of its thickness or even throughout its thickness.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a cross-sectional view of an embodiment of a semiconductor device including a transistor,

Figures 2 and 3 are cross-sectional views of part of the semiconductor body of the device shown in Figure 1 during different stages of the manufacture by means of a method in accordance with the invention,

Figure 4 is a cross-sectional view taken on the line IV—IV of Figure 5 of a part

of another embodiment and in the form of an integrated semiconductor device,

Figure 5 is a plan view of the part of the semiconductor device shown in Figure 4,

Figures 6, 7, 8 and 9 are cross-sectional views of stages of part of the semiconductor body of another embodiment in the form of an integrated semiconductor device and during various stages in the manufacture thereof by means of a method in accordance with the said further aspect of the invention,

Figure 10 shows a detail of an embodiment which is a slight modification of the embodiment shown in Figure 4.

Figure 11 shows a part of another embodiment in the form of an integrated semiconductor device having two transistors and a common collector zone,

Figures 12, 14, 17, 20 and 21 are cross-sectional views of parts of other embodiments in the form of integrated semiconductor devices,

Figure 13 shows a detail of an embodiment which is a slight modification of the device shown in Figure 12,

Figure 15 is a cross-sectional view of part of the semiconductor body of the device shown in Figure 14 during a stage in the manufacture thereof by means of a method in accordance with the further aspect of the invention,

Figure 16 shows a detail of an embodiment which is a slight modification of the device shown in Figure 14,

Figures 18 and 19 show part of the semiconductor body of the device shown in Figure 17 during stages in the manufacture thereof by means of a method in accordance with the further aspect of the invention.

Corresponding components, layers, parts, zones etc. in the Figures of different embodiments are referred to by the same reference numerals.

The first embodiment now to be described with reference to Figure 1 is a semiconductor device in the form of a transistor. The transistor comprises a semiconductor body 1 and a pattern 2 of insulating material inset in said body 1 and extending substantially throughout its thickness from the main surface 3 of the body 1 in said body. The body 1 comprises a first layer-shaped part 4 which adjoins the main surface 3 and which furthermore, along its full perimeter and throughout its thickness, adjoins a first part 5 of the inset pattern 2. The base zone 6 of the transistor adjoining the main surface 3 is present in the layer-shaped part 4. Said base zone 6, along its full perimeter and throughout its thickness, adjoins the first part 5 of the pattern 2. The emitter zone 7 of the transistor adjoining the main surface 3 is provided in the base zone 6. The col-

lector zone 26 comprises a part 8 present below the base zone 6.

The semiconductor body 1 comprises a second layer-shaped part 9 which adjoins the main surface 3 and is present beside the layer-shaped part 4. The layer-shaped part 9, along its full perimeter and throughout its thickness, adjoins a second part 10 of the inset pattern 2, said second part 10 having been provided simultaneously with the first part 5 of the pattern 2. The second layer-shaped part 9 constitutes a connection part of the collector zone 26 which adjoins the main surface 3 and which is separated from the first layer-shaped part 4 and hence from the base zones 6 only by a separation part 11 of the pattern 2 and belonging to the two said parts 5 and 10 of the pattern 2. The connection part 9 and the part 8 of the collector zone present below the base zone 6 are interconnected by an interconnection part 12 of the collector zone 26 present partly below the separation part 11 of the pattern.

The connection part 9 of the collector zone in this embodiment comprises a contact zone 13 in the form of a surface zone of the same conductivity type as the collector zone. The zone 13 has the same thickness and the same doping profile as the emitter zone 7 and hence in the manufacture of the device may be provided simultaneously with the emitter zone 7. The emitter zone of a transistor is a highly doped zone and so is, consequently, the contact zone 13. The contact zone 13 provides for a good electrical connection to the collector zone 26.

As shown in Figure 1, it is not necessary for contacting the collector zone nor for contacting the emitter zone and the base zone to etch an aperture in a thick insulating layer part belonging to the inset pattern, since the collector zone extends upwards in the pattern, see the layer-shaped part 9 belonging to the collector zone, the surfaces of the layer-shaped parts 4 and 9 lying substantially in the same flat plane 3.

The first and the second part (5 and 10) of the pattern 2 have the same homogeneous thickness. This is not always necessary or desirable as will be explained with reference to an embodiment to be described hereinafter.

Furthermore, the first and the second part (5 and 10) of the pattern 2 extend homogeneously at the same distance from the main surface 3 in the body 1. This feature also is not always necessary or desirable as will be described hereinafter with reference to another embodiment.

In a modification of the transistor structure of Figure 1 the connection part 9 of the collector zone extends to the edge of the semiconductor body 1, the second part 10 of

the pattern 2 only partly surrounding the layer-shaped part 9.

In another modification of the transistor structure of Figure 1 the connection part 9 of the collector zone fully surrounds the first layer-shaped part 4, and therefore also the base zone 6.

The pattern 2 extends in the semiconductor body 1 to a larger depth from the main surface 3 than the base zone 6. However, it is also possible for the base zone to extend slightly more deeply in the body 1 than the pattern 2.

The manufacture of the transistor shown in Figure 1 by a method in accordance with the further aspect of the invention will now be described.

A semiconductor body 1 is used (see Figure 2) which consists of a monocrystalline *n*-type silicon support 12 having a thickness of approximately 200 μm and a resistivity of approximately 0.01 ohm.cm, on the surface 15 of which an epitaxial *n*-type silicon layer 14 is provided having a thickness of approximately 5 μm and a resistivity of approximately 0.5 ohm.cm. The surface of the epitaxial layer 14 constitutes a main surface 3, parts 3a and 3b of the surface 3 being masked by means of masking layers 16 and 17.

The masking layers 16 and 17 consist of silicon nitride and may be provided in a conventional manner, for example, by first providing throughout the surface 3, a silicon nitride layer by vapour deposition from a mixture of hydrogen, silane and ammonia at a temperature of approximately 1000°C and then removing said nitride layer locally by etching.

By the conversion of non-masked semiconductor material into insulating material (see also Figure 3) the first part 5 which fully laterally surrounds the first surface part 3a, and the second part 10 which laterally surrounds the second surface part 3b of the inset pattern 2 of insulating material which extends from the main surface 3 in the body 1, are simultaneously provided.

By oxidation in a usual manner, non-masked silicon is converted into the pattern 2 of silicon oxide. However, without any initial material removal at the exposed silicon surface parts a silicon oxide pattern 2 would be obtained which is inset in the body 1 only over approximately half its thickness. Therefore, prior to providing the pattern 2, surface parts of the semiconductor body 1 are removed at the region of the said pattern as a result of which recesses 18 are obtained which extend from the main surface 3 over part of the thickness of the body 1 in said body, after which the pattern 2 is provided by conversion of non-masked silicon into silicon oxide which fills the recesses 18. The recesses 18 are provided

having a depth of approximately 1 μm and the pattern 2 of silicon oxide has a thickness of approximately 2 μm .

By providing the pattern 2, a first layer-shaped part 4 of the semiconductor body is obtained which, along its full perimeter and throughout its thickness, adjoins the first part 5 of the pattern 2 and a second layer-shaped part 9 of the body 1 is obtained which, along its full perimeter and throughout its thickness, adjoins the second part 10 of the pattern 2.

The layer-shaped parts 4 and 9 are separated from each other only by the separation part 11 of the pattern 2 belonging to the parts 5 and 10.

The pattern 2 is inset in the semiconductor body over such a distance that a part of the region of one conductivity type remains present below the separation part 11.

After providing the pattern 2, the silicon nitride layers 16 and 17 are replaced in a conventional manner by the silicon oxide layers 19 and 20 having a thickness of approximately 0.2 μm .

My means of conventional masking and diffusion methods, the base zone 6 is provided in the first layer-shaped part 4. The base zone 6 adjoins the first surface part 3 and along its full perimeter adjoins the first part 5 of the pattern 2. The *p-n* junction 19 is formed by the base zone 6 and the region (8, 9, 12, 13) (see Figure 1). The *p*-type base zone is obtained, for example, by diffusion of boron and has a thickness of approximately 1.8 μm and consequently adjoins throughout its thickness the first part 5 of the pattern 2.

An accurate masking method is not necessary in the base diffusion, since the pattern 2 has a masking effect and it is intended that the base zone to be provided adjoins the part 5 of the pattern 2 along its full perimeter.

The emitter zone 7 and the collector contact zone 13 are provided in a conventional manner, for example by diffusion of phosphorous, and have a thickness of approximately 1 μm . For the same reasons as for the base diffusion, no accurate masking method is necessary for the collector contact zone diffusion.

The *n*-type region (8, 9, 12, 13) which partly adjoins the second surface part 3b and is partly present below the separation part 11 and below the base zone 6 constitutes the collector zone 26 of the transistor.

In the method described it is of importance that the location of the connection part 9 of the collector zone 26 relative to the layer-shaped part 4, thus relative to the base zone 6, is determined by means of only one masking operation, namely that for providing the pattern 2, as a result of which said determination of the location is very

exact and substantially without tolerances, which means a gain in space. The distance between the zones 6 and 13 is approximately 10 μ m.

It is to be noted that for simplicity of illustration underetching and underoxidation have not been taken into account in Figures 1 to 3. Actually the recesses 18 and the pattern 2 slightly extend laterally below the masking layer parts 16, 17.

The zones 6, 7 and 13 are provided in a conventional manner with a base contact layer 21, an emitter contact layer 22 and a collector contact layer 23, respectively, which consist, for example, of a metal layer of aluminium. The metal layers 21 and 22 extend to over the pattern 2 and a connection conductor is connected to the parts of said metal layers present on the pattern, which is shown in Figure 1 only for the base contact layer 21, see the connection conductor 24 connected to said layer. The metal layer 23 is present substantially entirely on the collector contact zone 13 and a connection conductor 25 is connected to the said layer. The collector contact zone 13 may also be constructed so as to be smaller, the metal layer 23 extending over the pattern 2 and being connected to the connection conductor 25 above said pattern 2.

Viewed in a direction perpendicular to the pattern 2 the various zones and parts of the transistor have the dimensions which are normal for a transistor, the collector contact zone 13 with the collector contact layer 23 present thereon having the dimensions which are normal for a metal contact layer.

In a modification of the described method the base zone 6 is provided prior to providing the pattern 2 in which during the provision of the pattern 2 the remainder of the semiconductor body 1 constitutes the region of one conductivity type which does not adjoin the surface part 3a but does extend below said surface part.

An embodiment in the form of an integrated semiconductor device will now be described with reference to Figures 4 and 5 where parts and regions corresponding to those present in the single transistor in Figure 1 are indicated by the same reference numerals.

The pattern 2 of insulating material extends from the main surface 3 in the semiconductor body 1 over a part of a thickness of said body. The first layer-shaped part 4 of the semiconductor body 1 adjoins, along its full perimeter and throughout its thickness, adjoins the first part 5 of the inset pattern 2. In the part 4 is provided the base zone 6 or a transistor T adjoining the main surface 3 which zone along its full perimeter and throughout its thickness adjoins the part

5 of the pattern 2, and the emitter zone 7 adjoining the main surface is provided in said base zone 6. The collector zone 26 comprises a part 8 present below the base zone.

Beside the first layer-shaped part 4, a second layer-shaped part 9 of the semiconductor body 1 is present which, along its full perimeter and throughout its thickness, adjoins the second part 10 of the inset pattern 2. The second layer-shaped part 9 constitutes a connection part of the collector zone 26 adjoining the main surface 3, which zone is separated from the first layer-shaped part 4 and hence from the base zone 6 by the separation part 11 which belongs to the parts 5 and 10 of the inset pattern 2. The connection part 9 and the part 8 of the collector zone present below the base zone 6 are interconnected by an interconnection part 32 which is partly present below the separation part 11.

The parts 5 and 10 of the pattern have the same homogeneous thickness (measured transverse to the main surface 3) and extend homogeneously the same distance from the main surface 3 in the body 1.

The surfaces 3a and 3b of the layer-shaped parts 4 and 9 are located substantially in the same flat plane 3.

The collector zone 26 comprises a collector contact zone 13 which is present in the connection part 9 and has the same thickness and the same doping profile as the emitter zone 7. The collector contact zone 13 adjoins, along its full perimeter and throughout its thickness, the second part 10 of the pattern 2 and is separated from the base zone 6 only by the separation part 11. The metal contact layers 21, 22 and 23 are connected to the zones 6, 7 and 13.

In the present embodiment, the semiconductor body comprises a plurality of circuit elements, including the transistor T, which circuit elements are present in a number of semiconductor regions (6, 7, 26), and 40 to 49, termed islands, which are separated from each other and adjoin the main surface 3.

For simplicity, Figures 4 and 5 only show the islands (6, 7, 26) and 40 completely. Furthermore for clarity the insulating layers covering the islands and contact layers connected to semiconductor zones are not shown in Figure 5; the apertures for the contact layers in the insulating layers being denoted by broken lines.

The circuit element in the island 40 is a resistor element R comprising a surface zone 50 provided with contact layers 51 and 52. The surface zone 50 is of the same conductivity type as the base zone 6 and furthermore said zones have the same doping profile and the same thickness.

Isolation zones which are formed by parts 130

surrounding the islands, termed isolation parts, of the inset pattern are present between the islands. The island (6, 7, 26) is laterally surrounded by an insulating part 53 and the island 40 is laterally surrounded by an insulating part 54 of the inset pattern 2.

The first part 5 and the second part 10 of the pattern 2 not only comprise the separation part 11 but also an insulating part 53 laterally surrounding the base zone 6 and the connection part 9 of the collector zone 26 collectively, which part 53 constitutes an isolation zone laterally surrounding the transistor.

The semiconductor body 1 comprises a semiconductor support 55 and an epitaxial layer 56 which is provided thereon and adjoins the main surface 3 and which is divided, by the isolation zones, for example, the zones 53 and 54, into parts belonging to the islands (6, 7, 26) and 40 to 49. The support comprises a substrate 57 from which the islands are isolated by a $p-n$ junction. The island (6, 7, 26) is isolated from the substrate 57 by the $p-n$ junction 58 and the island 40 is isolated from the substrate 57 by the $p-n$ junction 59.

The collector zone 26 of the transistor T forms the isolating $p-n$ junction 58 with the substrate 57 and comprises a part 8, 9 present in the epitaxial layer 56 and a buried layer part 32 present partly in the support 55. The buried part 32 is present partly below the separation part 11 of the inset pattern 2 and constitutes the interconnection part of the collector zone 26.

The inset pattern consists of insulating material formed by the conversion of semiconductor material of the body 1.

The transistor T is obtained in a similar manner to the transistor shown in Figure 1.

The manufacture of the integrated semiconductor device shown in Figures 4 and 5 will now be described with reference to Figures 6 to 9.

Of a silicon body 1, see Figure 6, having an n -type region 69 adjoining the main surface 3, surface parts 3a and 3b of the main surface 3 separated from each other are masked by providing in a conventional manner silicon nitride layer parts 60 and 61. A first part 5 (see also Figure 7) which surrounds the surface part 3a and a second part 10 which surrounds the surface part 3b of the inset pattern 2 are simultaneously provided by converting non-masked silicon into insulating silicon oxide, for example, in a flow of steam at a temperature of approximately 1000°C. The layer-shaped parts 4 and 9 of the semiconductor body which, along their full perimeters and throughout their thickness, adjoin the parts 5 and 10, respectively, of the pattern 2 are thus obtained. The layer-shaped parts 4 and 9

are separated from each other only by the separation part 11 which belongs to the first part 5 and the second part 10 of the pattern 2.

The pattern 2 is inset in the semiconductor body to such a distance from the main surface 3 that a part 32 of the region 69 remains present below the separation part.

In order to inset the pattern 2 substantially throughout its whole thickness in the body 1 and hence to obtain a substantially plane surface of the semiconductor device, recesses 62 are etched prior to the oxidation treatment to obtain the pattern 2 of silicon oxide, while using the nitride layers as an etching mask, which recesses extend in the semiconductor body 1 to a distance from the main surface 3 which is approximately half as large as the desirable distance over which the pattern 2 to be provided extends in the body 1, after which the pattern 2 is provided by an oxidation treatment, the recesses 62 being filled with silicon oxide.

After providing the pattern 2, the silicon nitride layer parts 60 and 61 are replaced by silicon oxide layers 63 and 64 and the n -type base zone 6, the n -type emitter zone 7 and the n -type collector contact zone 13 are provided by conventional masking and diffusion methods, by the diffusion of boron, phosphorus and phosphorus, respectively, in which the zones 7 and 13 may be provided simultaneously.

The base zone 6 forms a $p-n$ -junction 19 with the part 26 of the region 69.

This part which partly adjoins the second surface part 31 and is partly present below the separation part 11 and below the base zone 6, constitutes the collector zone of the transistor T.

In the present embodiment a semiconductor body 1 is used the n -type region 69 of which, see Figure 6, adjoins the whole main surface 3 and which is isolated from a p -type substrate 57 present below the region 69 by a $p-n$ junction 66. The region 69 is divided into juxtaposed islands (6, 7, 26) and 40 to 49, see also Figures 7 and 5, by providing in the region 69 isolation zones consisting of parts of an insulating material, termed insulating parts, of the pattern 2 which adjoin the isolation on the substrate side. See the insulating parts 53 and 54 in Figures 7 and 4 and 5 around the islands (6, 7, 26) and 40.

The isolation zones are thus obtained simultaneously with the provision of the pattern 2 as parts of said pattern. In this case the part 55 which belongs to the first part 5 and the second part 10 of the inset pattern 2 and surrounds the base zone 6 and the connection part 9 of the collector zone 26 collectively is designed as an isolation part, thus in this example as an isolation

zone which laterally surrounds the transistor T.

In addition to the island (6, 7, 26) to be provided, which, during the provision of the pattern 2, is masked by the silicon nitride layers 60 and 61, see Figure 6, the other islands to be obtained are also masked against said conversion during the provision of the pattern 2 by conversion of non-masked semiconductor material. For example, the island 40 to be obtained is masked against oxidation by the silicon nitride layer 65. After providing the pattern, all masking layers are replaced by silicon oxide layers, the silicon nitride layer 65 being replaced by the silicon oxide layer 67.

The *p*-type zone 50 of the resistance element R, see Figures 4 and 5, is obtained by a boron diffusion which is carried out simultaneously with that to obtain the base zone 6.

The semiconductor body 1 with the *n*-type region 69 is obtained by starting from a semiconductor support 55, see Figure 8, of silicon having *p*-type conductivity, a resistivity of approximately 2 ohm.cm and a thickness of approximately 200 μ m, and by providing on the support surface 68 an *n*-type epitaxial silicon layer 56 having a resistivity of approximately 0.2 ohm.cm and a thickness of approximately 2 μ m, see Figure 9.

In the present embodiment the support is provided with an *n*-type surface zone 32a adjoining the support surface 68, for example by diffusion of arsenic, see Figure 8. The surface zone 32a is situated below the separation part 11 of the pattern 2 (see Figure 7), and this diffused surface zone will be laterally bounded by the insulation zone 53 which will surround the transistor T when later provided. After the provision of the surface zone 32a the epitaxial layer 56 is provided. The support 55 then comprises the *p*-type substrate 57 and the *n*-type buried layer part 32 which together with the epitaxial *n*-type layer 56 constitutes the *n*-type region 69 (Figure 9). The buried layer part 32 has a thickness of approximately 5 μ m. A small amount of arsenic can diffuse from the buried layer 32 in the epitaxial layer 56 which is denoted in Figure 9 by a broken line.

The pattern 2 is inset in the semiconductor body 1 to a depth larger than the thickness of the epitaxial layer, for example, to a distance of between 2.1 and 2.2 μ m from the main surface 3.

The masking silicon nitride layer parts 60, 61 and 65 each have a thickness of approximately 0.2 μ m and may be provided by vapour disposition from a stream of a mixture of hydrogen, silane and ammonia at a temperature of approximately 1000°C.

These layers are later replaced in a normal manner by silicon oxide layers 63, 64 and 67 having thicknesses of approximately 0.2 μ m.

The base zone 6 and the resistance zone 50 have thicknesses of approximately 1 μ m and the emitter zone 7 and the collector contact zone 13 have thicknesses of approximately 0.6 μ m. In Figure 5 the dimensions of the base zone 6 are approximately 45 $\times$ 30 μ m, those of the emitter zones approximately 20 $\times$ 20 μ m, those of the collector contact zone 13 approximately 20 $\times$ 30 μ m, and the width B of the isolation parts 53 and 54 and the separation part 11 is approximately 10 to 15 μ m.

Since the *p*-type substrate 57 is of comparatively high resistivity (2 ohm.cm), conductive channels adjoining the pattern 2 may occur in the substrate 57 and interconnect the islands. These channels can be prevented by increasing the *p*-type doping in the substrate below the pattern 2, which is denoted in Figures 4, 6, 7 and 9 by the zones 71 which are obtained by a boron diffusion in the zones 71a of the support, see Figure 8. It is alternatively possible to choose a support 55 which is entirely of low resistivity material and has a resistivity of, for example, 0.02 ohm.cm, which, however, results in a lower breakdown voltage of the *p-n* junctions 58 and 59, see Figure 4.

Another possibility is shown in Figure 10 which Figure for simplicity shows only a part of the semiconductor device which corresponds to the left-hand part of Figure 4. The inset insulating pattern 2 does not extend up to the substrate 57 but only up to the depletion region 73 of the *p-n* junction 66 which is bounded by the broken line 74. This depletion region 73 occurs during operation of the semiconductor device due to a usual voltage in the reverse direction across the *p-n* junction 66. During operation said depletion region closes the isolation between the islands.

In the embodiments described the base zone 6 may alternatively be provided prior to providing the pattern 2.

Figure 11 shows a transistor T₁ of the same kind as the transistor T shown in Figures 4 and 5. This transistor T₁, however, has a collector zone 26 in common with a transistor T₂ which is also of the same kind as the transistor T shown in Figures 4 and 5. In this structure, the part 53 of the pattern 2 which surrounds the base zone 6 and the connection part 9 of the collector zone of the transistor T₁ collectively, does not entirely belong to an isolation zone, since the part 75 of the part 53 serves as a separation part between the connection part 9 of the collector zone and the base zone 6 of the transistor T₂.

Figure 12 is a cross-sectional view of a

part of an embodiment of a semiconductor device in accordance with the invention which differs from that shown in Figures 4 and 5 only in that the isolation zones (2, 76) comprise zones 76 of the same conductivity type as the substrate 57 which are present between the substrate 57 and the inset insulating pattern parts 53 and 54 of the isolation zones (2, 76). The zones 76 thus have *p*-type conductivity.

The manufacture of the device shown in Figure 12 differs only slightly from the manufacture of the device shown in Figures 4 and 5.

In surface zones 71a of the support 55 adjoining the support surface 68 (see Figure 8), which zones are present below the insulating pattern parts 53, 54 to be provided, the concentration of impurities causing *p*-type conductivity is increased, for example, by diffusion of boron. The *n*-type epitaxial layer 56, see also Figure 12, is then provided and the zones 76 of *p*-type conductivity which adjoin the substrate 57, belong to the isolation zones (2, 76) and are present in the epitaxial layer 56, are obtained by diffusion of impurities from the zones 71a in the epitaxial layer. The pattern 2 is inset in the epitaxial layer 56 only over part of the thickness of the said layer and the isolation zones (2, 76) are constituted only near the main surface 3 by the inset insulating pattern parts 53 and 54 of the inset pattern 2.

The zones 76 adjoin the pattern 2. It is also possible that the pattern 2 is not inset in the semiconductor body 1 up to the zones 76, but only up to the depletion region 78 of the *p-n* junction 77, see Figure 13, bounding the substrate and the zone 76. Figure 13 shows only a part corresponding to the left-hand part of the semiconductor device of Figure 12. The depletion region 78 between the *p-n* junction 77 and the broken line 80 occurs during operation due to the normally applied voltage in the reverse direction across the *p-n* junction 77.

In structures having the form shown in Figures 12 and 13, a thicker epitaxial layer 56, for example of a thickness of 4 μm , may be used while avoiding a pattern 2 to be inset to an unpractical depth and in which more space is available below the separation part 11 of the pattern 2 for the interconnection part of the collector zone. If desirable, the buried layer 32 may be omitted in this case.

Figure 14 shows another embodiment in which the isolation zones (2, 81) comprise *p*-type zones 81 which are present between the substrate 57 and the inset insulating pattern parts 53 and 54. The zones 81, however, have not been obtained by diffusion from the substrate 57 as will now be described with reference to Figure 15.

Prior to providing the pattern 2, *p*-type zones 81a adjoining recesses 62 which correspond in surface location to the inset insulating pattern parts 54 and 53 to be provided are provided in the epitaxial layer 56. In this respect Figure 15 should be compared with Figure 6. The zones 81a may be provided, for example, by ion implantation while using the masking effect of the silicon nitride layers (60, 61 and 65). The silicon nitride layers project slightly above the recesses 62, since during the provision of the recesses 62 underetching occurs. For simplicity this latter is not shown in Figure 15 (or in Figure 6). The inset pattern 2 of silicon oxide is then provided by oxidation, the zones 81a diffusing inwards in the body ahead of the inset pattern 2. The pattern 2 is inset in the epitaxial layer 56 only over part of the thickness of the layer, the *p*-type zones 81 which adjoin the pattern 2 extending up to the *p*-type substrate 57. For the remainder, the manufacture of the device shown in Figure 14 is carried out in a manner similar to that of the device shown in Figures 4 and 5.

The zones 81 need not reach the substrate 57, it is sufficient for them to reach the depletion region 82 of the *p-n* junction 83, see Figure 16. This depletion region occurs during operation of the semiconductor device due to the normally applied reverse voltage across the *p-n* junction 83. For simplicity, Figure 16 shows only a part corresponding to the left-hand part of the semiconductor device of Figure 14.

It will be obvious that the structure shown in Figure 11 may be provided with isolation zones (2, 76) according to Figure 12 or with the isolation zones (2, 81) according to Figure 14.

In respect of the isolation zones of the kind described reference is invited to our copending Patent Application No. 31839/71.

In the examples described, the whole pattern 2 is inset in the semiconductor body 1 substantially throughout its thickness. In order to achieve this, the recesses 62 are provided in the body 1 prior to providing the pattern 2, see Figures 6 and 15. If the recesses 62 are not provided, a pattern 2 of silicon oxide is obtained which is inset approximately over half its thickness.

It is possible to inset a part of the pattern 2 throughout its thickness and another part of the pattern only over a part of its thickness in the semiconductor body. Figure 17 shows an example of this and relates to a semiconductor device which differs only from that shown in Figures 4 and 5 in that the separation part 11 of the pattern 2 is inset in the semiconductor body 1 to substantially half its thickness, while the remainder of the pattern 2 is inset in the semiconductor body substantially throughout

its thickness. The structure may be obtained by providing recesses 62 at the region of the pattern to be provided, see Figure 6, with the exception, however, of the region where the separation part 11 of the pattern 2 is to be provided, and then providing the pattern 2 by oxidation.

An advantage of the structure shown in Figure 17 is that, due to inseting the separation part 11 to a smaller depth, a better interconnection is obtained between the connection part 9 and the part 8 of the collector zone 26 present below the base zone 6, while, if desirable, the buried layer part 32 may be omitted.

The pattern 2 shown in Figure 17 can be provided in a simple manner as will now be described with reference to Figures 18 and 19.

On the semiconductor body 1, see Figure 18, a masking layer is provided which consists of a silicon nitride layer 85 having provided thereon a silicon oxide layer 86, which layers are removed at the region of the inset insulating pattern parts 53 and 54 to be provided. Only the silicon oxide layer 86 is then removed at the region of the separation part 11 to be provided, and the recesses 62 are then etched at the region of the inset insulating pattern parts 53 and 54, as a result of which the structure shown in Figure 18 is obtained.

The silicon nitride layer 85 is then removed by a selective etching treatment at the region of the separation part 11 to be provided, the silicon oxide layer 86 serving as an etching mask. The structure shown in Figure 19 is then obtained and the pattern 2 may now be provided by an oxidation treatment.

In the embodiment shown in Figure 17, the first part 5 of the pattern 2 which surrounds the base zone 6 and the second part 10 of the pattern 2 which surrounds the connection part 9 of the collector zone 26, do not extend homogeneously up to the same distance from the main surface of the semiconductor body 1, as contrasted with the preceding embodiments. The parts 5 and 10, however, have the same homogeneous thickness and have been provided simultaneously. It is possible, however, to remove the projecting part of the separation part 11 at least partly by etching. In that case the parts 5 and 10 no longer have a homogeneous thickness. The layer-shaped parts 4 and 9 in this embodiment extend to the same distance from the main surface 3 in the body 1 as the separation part 11, while the inset insulating pattern parts 53 and 54 extend deeper in the body 1.

In the embodiments described it is possible to remove the substrate 57 entirely or partly, for example by etching, Figure 20 shows a semiconductor device of the form

shown in Figure 12 but in which the substrate 57 is removed up to the buried layer part 32. A metal layer 90 to reduce the collector series resistance may be provided on the buried layer part 32, while in addition, if desired, the collector may also be connected or through-connected on the lower side via said metal layer.

It is also possible to remove the remaining *p*-type parts 57, 71 and 76 in the device shown in Figure 20 by etching, after which no substrate at all is present any longer and the isolation zones consist of the inset insulating pattern parts 53 and 54 and of grooves at the location of the zones 76. These grooves may be filled with an insulating material, if desired. No *p-n* junction isolation and associated stray capacitances are present any longer and the semiconductor body 1 then consists of a number of parts (islands) which are separated from each other.

In a manner similar to that described with reference to the device shown in Figure 12, the substrate 57 of the device shown in Figures 4 and 5 and of the device shown in Figure 11 may be removed and also the substrate 57 and the zones 81 of the device shown in Figure 14.

It is furthermore possible in the devices shown in Figures 12 and 14 not to provide the zones 76 and 71, and the zones 81, respectively, but to provide a buried layer part 32 which extends below all the islands, to remove the substrate 57 and to etch grooves below the isolation parts 53 and 54 of the pattern 2 transversely through the buried layer part 32 and up to said isolation parts, after which the device shown in Figure 21 is obtained having buried layer parts 32a, 32b, and so on. For the provision of the buried layer parts 32a, 32b and so on, no masking is necessary. Starting material may be a *p*-type support 55 which is provided with a highly doped *p*-type epitaxial or diffused layer and the less highly doped *n*-type epitaxial layer 56 may be provided thereon. It is also possible to start from a support which consists entirely of low-resistivity *n*-type silicon.

In the device shown in Figure 21, the semiconductor body consists of the parts (islands) 1a, 1b, 1c, and so on which are separated from each other.

The devices described may be provided in a conventional manner with conductive tracks which have widenings to which connection conductors can be connected and which widenings are preferably provided on the inset pattern 2.

Many variations are possible to those skilled in the art without departing from the scope of this invention. For example, only the part of the support used which adjoins the support surface 68, see Figure 8, 130

need have *p*-type conductivity and, for example, the part of the support below the broken line in Figure 8 may have *n*-type conductivity. The masking layers 60, 61 and 65, see Figure 6, may consist of a silicon layer provided on the semiconductor body 1, on which layer a silicon nitride layer is provided in which, after providing the pattern 2 and after removing the silicon nitride layer, the silicon oxide layers 63, 64 and 67, see Figure 7, are obtained directly. The emitter zones 7 of the embodiments described may also adjoin the inset pattern 2 along a part of their perimeters. The oxidation treatment to obtain the pattern 2 may be interrupted, in which during the interruption the already obtained silicon oxide may be removed at least partly, for example, by etching, it is not necessary then, for obtaining a pattern 2 which is inset substantially throughout its thickness in the semiconductor body, to provide the recesses 62, see for example Figure 6, prior to the oxidation treatment. It is not necessary to replace the silicon nitride layers 60, 61 and 65 by the silicon oxide layers 63, 64 and 67, see Figures 6 and 7. The silicon nitride layers 60, 61 and 65 may also be used for masking during diffusion steps. The second layer-shaped part 9 of the semiconductor body 1, see for example Figure 14, need not belong entirely to the connection part of the collector zone 26 and may comprise, for example, in addition a diode. Two different islands may be connected together in a manner similar to that of the connection part 9 to the part 8 of the collector zone present below the base zone in the examples described. Usual semiconductor materials other than silicon may be used in which the pattern may consist of grooves filled with insulating material or of insulating material which has been obtained by the conversion of semiconductor material into insulating material. For example, the semiconductor material silicon carbide may be converted, for example by oxidation, into silicon oxide.

50 WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor body including a transistor, a pattern of an insulating material being inset in the semiconductor body and extending
55 in said body from a main surface thereof over at least a part of its thickness, the semiconductor body having a first layer-shaped part and a simultaneously provided second layer-shaped part situated beside and
60 spaced from the first layer-shaped part, said first layer-shaped part adjoining the main surface and along its full perimeter and throughout its thickness, adjoining a first part of the inset pattern, said second layer-
65 shaped part adjoining the main surface and

adjoining, along at least a part of its perimeter and throughout its thickness, a second part of the pattern, in said first layer-shaped part the base zone of the transistor adjoining the main surface and, along its full perimeter, adjoining the first part of the pattern, the emitter zone of the transistor being provided in the base zone and adjoining the main surface, and the collector zone comprising a part which is present below the base zone, said second layer-shaped part comprising a connection part of the collector zone which connection part adjoins the main surface and is separated from the first layer-shaped part only by a separation part belonging to at least one of the two said parts of the pattern, said connection part and the part of the collector zone below the base zone being interconnected by an interconnection part of the collector zone present at least partly below the separation part of the inset insulating pattern.

2. A semiconductor device as claimed in Claim 1, wherein the first and the second part of the inset pattern have substantially the same homogeneous thickness.

3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein the surfaces of the first and the second layer-shaped part are located substantially in the same flat plane.

4. A semiconductor device as claimed in any of the preceding Claims, wherein the first and the second part of the inset pattern extend homogeneously substantially to the same distance from the main surface of the semiconductor body in said body.

5. A semiconductor device as claimed in any of the preceding Claims, wherein the connection part of the collector zone comprises a highly doped contact zone in the form of a surface adjoining zone of the same conductivity type as the collector zone.

6. A semiconductor device as claimed in any of the preceding Claims, wherein the semiconductor body comprises a plurality of circuit elements, including the transistor, which circuit elements are situated in a number of semiconductor islands, the islands adjoining the main surface and being separated from each other by isolation zones which are formed, at least near the main surface, by insulating parts of the inset pattern which laterally surround the islands, the first and the second part of the inset pattern together constituting, in addition to the separation part, a part which surrounds the base zone and the connection part of the collector zone of the transistor collectively, said part belonging to at least partly to an insulating part of an isolation zone surrounding the transistor.

7. A semiconductor device as claimed in Claim 6, wherein the semiconductor body comprises a semiconductor support and an

need have *p*-type conductivity and, for example, the part of the support below the broken line in Figure 8 may have *n*-type conductivity. The masking layers 60, 61 and 65, see Figure 6, may consist of a silicon layer provided on the semiconductor body 1, on which layer a silicon nitride layer is provided in which, after providing the pattern 2 and after removing the silicon nitride layer, the silicon oxide layers 63, 64 and 67, see Figure 7, are obtained directly. The emitter zones 7 of the embodiments described may also adjoin the inset pattern 2 along a part of their perimeters. The oxidation treatment to obtain the pattern 2 may be interrupted, in which during the interruption the already obtained silicon oxide may be removed at least partly, for example, by etching, it is not necessary then, for obtaining a pattern 2 which is inset substantially throughout its thickness in the semiconductor body, to provide the recesses 62, see for example Figure 6, prior to the oxidation treatment. It is not necessary to replace the silicon nitride layers 60, 61 and 65 by the silicon oxide layers 63, 64 and 67, see Figures 6 and 7. The silicon nitride layers 60, 61 and 65 may also be used for masking during diffusion steps. The second layer-shaped part 9 of the semiconductor body 1, see for example Figure 14, need not belong entirely to the connection part of the collector zone 26 and may comprise, for example, in addition a diode. Two different islands may be connected together in a manner similar to that of the connection part 9 to the part 8 of the collector zone present below the base zone in the examples described. Usual semiconductor materials other than silicon may be used in which the pattern may consist of grooves filled with insulating material or of insulating material which has been obtained by the conversion of semiconductor material into insulating material. For example, the semiconductor material silicon carbide may be converted, for example by oxidation, into silicon oxide.

50 WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor body including a transistor, a pattern of an insulating material being inset in the semiconductor body and extending
55 in said body from a main surface thereof over at least a part of its thickness, the semiconductor body having a first layer-shaped part and a simultaneously provided second layer-shaped part situated beside and
60 spaced from the first layer-shaped part, said first layer-shaped part adjoining the main surface and along its full perimeter and throughout its thickness, adjoining a first part of the inset pattern, said second layer-
65 shaped part adjoining the main surface and

adjoining, along at least a part of its perimeter and throughout its thickness, a second part of the pattern, in said first layer-shaped part the base zone of the transistor adjoining the main surface and, along its full perimeter, adjoining the first part of the pattern, the emitter zone of the transistor being provided in the base zone and adjoining the main surface, and the collector zone comprising a part which is present below the base zone, said second layer-shaped part comprising a connection part of the collector zone which connection part adjoins the main surface and is separated from the first layer-shaped part only by a separation part belonging to at least one of the two said parts of the pattern, said connection part and the part of the collector zone below the base zone being interconnected by an interconnection part of the collector zone present at least partly below the separation part of the inset insulating pattern.

2. A semiconductor device as claimed in Claim 1, wherein the first and the second part of the inset pattern have substantially the same homogeneous thickness.

3. A semiconductor device as claimed in Claim 1 or Claim 2, wherein the surfaces of the first and the second layer-shaped part are located substantially in the same flat plane.

4. A semiconductor device as claimed in any of the preceding Claims, wherein the first and the second part of the inset pattern extend homogeneously substantially to the same distance from the main surface of the semiconductor body in said body.

5. A semiconductor device as claimed in any of the preceding Claims, wherein the connection part of the collector zone comprises a highly doped contact zone in the form of a surface adjoining zone of the same conductivity type as the collector zone.

6. A semiconductor device as claimed in any of the preceding Claims, wherein the semiconductor body comprises a plurality of circuit elements, including the transistor, which circuit elements are situated in a number of semiconductor islands, the islands adjoining the main surface and being separated from each other by isolation zones which are formed, at least near the main surface, by insulating parts of the inset pattern which laterally surround the islands, the first and the second part of the inset pattern together constituting, in addition to the separation part, a part which surrounds the base zone and the connection part of the collector zone of the transistor collectively, said part belonging at least partly to an insulating part of an isolation zone surrounding the transistor.

7. A semiconductor device as claimed in Claim 6, wherein the semiconductor body comprises a semiconductor support and an



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epitaxial layer provided therein and adjoining the main surface, said layer being divided by the isolation zones into parts belonging to the islands, the support comprising a substrate which is isolated from the islands by at least one $p-n$ junction.

8. A semiconductor device as claimed in Claim 7, wherein the collector zone of the transistor forms an isolating $p-n$ junction with the substrate and comprises a part situated in the epitaxial layer and a buried part situated in the support, the buried part partly being present below the separation part of the inset pattern and at least partly forming part of the interconnection part of the collector zone.

9. A semiconductor device as claimed in Claim 8, wherein the interconnection part of the collector zone where present below the separation part of the pattern consists of a buried layer part provided in the support.

10. A semiconductor device as claimed in any of Claims 7 to 9, wherein an isolation zone comprises a semiconductor zone which is of the same conductivity type as the substrate and which is present between the insulating part of the inset pattern belonging to said isolation zone and the substrate.

11. A semiconductor device as claimed in any of the preceding Claims, wherein the inset pattern consists of an insulating material formed by conversion of semiconductor material of the semiconductor body.

12. A method of manufacturing a semiconductor device claimed in any of the preceding Claims, wherein there are masked against oxidation a first part and a second part of a main surface of a semiconductor body, a region of one conductivity type of said body extending below said first and second surface parts, an insulating pattern inset in the semiconductor body being provided by conversion of the non-masked parts of said main surface into insulating material, so that a first layer-shaped part of the semiconductor body which, along its full perimeter and throughout its thickness, adjoins the first part of the pattern, and a second layer-shaped part of the semiconductor body which, at least along a part its perimeter and throughout its thickness, adjoins the second part of the pattern, are obtained, said layer-shaped parts being separated from each other only by a separation part belonging to at least one of the two said parts of the pattern, the pattern being inset in the semiconductor body over such a distance from the main surface that a part of the region of one conductivity type remains present below the separation part, a base zone of the transistor being provided adjoining the first surface part and adjoining, along its full perimeter, the first part

of the pattern, said base zone forming a $p-n$ junction with the region of one conductivity type, there being provided in the base zone an emitter zone of the transistor adjoining the first surface part, at least a part of the region of one conductivity type partly being present below the separation part and below the base zone and constituting the collector zone of the transistor.

13. A method as claimed in Claim 12, wherein a semiconductor body is used of which the region of one conductivity type adjoins the whole main surface and is isolated from a substrate of the opposite conductivity type present below the region by a $p-n$ junction, the region is divided into juxtaposed islands which are separated from each other by providing in the region isolation zones which, at least near the main surface, consist of parts of an insulating material, and which isolation zones adjoin the insulation provided by the $p-n$ junction at the substrate side, the insulating material parts being provided simultaneously with and forming part of the pattern, a part of the pattern which belongs to at least one of the two parts constituted by the first and the second part of the pattern and which collectively laterally surrounds the base zone and the connection part of the collector zone adjoining the second surface part, collectively laterally surrounding the transistor.

14. A method as claimed in Claim 13, wherein the semiconductor body with the region of one conductivity type is obtained by starting from a semiconductor support of which at least the part adjoining one surface is of the opposite conductivity type and by providing on said surface of the support an epitaxial layer of one conductivity type belonging to the said region.

15. A method as claimed in Claim 14, wherein prior to providing the epitaxial layer the support is provided with a surface zone of one conductivity type adjoining the said surface, the surface zone being situated so that it lies below the separation part of the inset pattern when later provided and it is laterally bounded by the isolation zone which laterally surrounds the transistor when later provided.

16. A method as claimed in Claim 14 or Claim 15, wherein in surface zones of the support adjoining the support surface, which zones are situated so that they lie below the insulating parts when later provided, the concentration of the impurities determining the opposite conductivity type is increased, after which the epitaxial layer is provided adjoining the substrate and belonging to the isolation zones are obtained by diffusion of impurities into the epitaxial layer from said zones, the pattern being inset in said layer



only over part of the thickness of the epitaxial layer.

17. A method as claimed in any of Claims 13 to 15, wherein prior to providing the inset pattern by conversion of non-masked semiconductor material into insulating material, impurities which cause the opposite conductivity type are provided in non-masked surface parts of the semiconductor body corresponding in surface location to the insulating parts to be provided, said impurities being diffused deeper in the semiconductor body during the provision of the pattern and forming zones of the opposite conductivity type which are present between the insulating parts and the substrate and which belong to the isolation zone.

18. A method as claimed in any of Claims 12 to 17, wherein prior to the provision of the inset pattern, surface parts of the semiconductor body are removed at the location of at least a part of the pattern to be provided so that recesses are obtained

which extend from the main surface over a part of the thickness of the semiconductor body in said body, the pattern being then provided by conversion of non-masked semiconductor material into insulating material which occupies the recesses over at least a part of their depth.

19. A method of manufacturing a semiconductor device as claimed in Claim 12 and substantially as herein described with reference to the accompanying drawings.

20. A semiconductor device substantially as herein described with reference to Figure 1, Figures 4 and 5, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 16, Figure 17, Figure 20 or Figure 21 of the accompanying drawings.

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