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(54) WIDE BAND AMPLIFIERS

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

THE INVENTION relates to a wide-band amplifier including a cascode-style arrangement of a first transistor of a first conductivity type and a second transistor of a second conductivity type opposite to said first type. The term "cascode-style" is used throughout this specification, including the appended claims, to denote that in such an amplifier the first (or input) transistor has its emitter connected to the base of the second transistor and its collector connected to the emitter of the second transistor, in such a way that there is substantially zero impedance in these connections.

The invention is particularly though not exclusively for use in integrated circuits in which the number of transistors and diodes used is not so important as is the number of resistors and in which inductances and transformers are to be completely avoided whilst capacitors are preferably to be avoided.

The frequency response of a wide-band amplifier, particularly one having a high cut-off frequency, is greatly influenced by the parasitic capacitance between the base and the collector of the input transistor. In order to reduce the influence of this capacitance a cascode-style arrangement of two transistors is frequently used at the input of the amplifier. This cascode-style arrangement counteracts voltage variations at the collector of the input transistor and hence reduces the voltage variations between the base and the collector of this input transistor. The higher the degree to which these voltage variations are suppressed, the better will be the high-frequency behaviour of the amplifier.

In differential amplifiers, it is further desirable to provide a voltage-level shift between the input and output of the amplifier, for in order to allow for a maximum common-mode input signal it is desirable for the voltage level at the input to be as high as possible, i.e. as close as possible to the supply voltage. However, in order to obtain a maximum latitude for variations of the output voltage it is desirable for the voltage level at the output to lie as close as possible to a point midway between the voltage at the positive terminal and that at the negative terminal of the supply voltage source. Hence, if both a large common-mode input signal and a large output signal capacity are to be provided for, a voltage-level shift between the input and the output of the amplifier is indispensable.

This voltage-level shift can simply be realised by means of lateral *pnp* transistors. However, the use of a lateral *pnp*-transistor introduces into the circuit an element having very poor high-frequency properties so that the bandwidth of the circuit is restricted. In order to eliminate the frequency behaviour of this *pnp* transistor it is known to shunt its emitter-collector path by a capacitor so that it is short-circuited for high frequencies. However, the value of this capacitor is such that it gives rise to great difficulty in integrated circuit technology.

It is an object of the present invention to provide an amplifier in which both a cascode-style operation and a suitable voltage-level shift are simply obtainable and which may readily be realised in an integrated circuit form.

The invention provides a wide-band amplifier including a cascode-style arrangement (as hereinbefore defined) of a first transistor of a first conductivity type and a second transistor of a second conductivity type, opposite to that of said first type, the connection between the collector of said first transistor and the emitter of said second transistor

being additionally connected to the collector of a third transistor of said first conductivity type, the base of said third transistor being connected to the collector of said second transistor whilst its emitter is connected to a voltage supply terminal.

As has been stated hereinbefore, the cascode-style arrangement of the first and second transistors reduces the influence of the parasitic input capacitance. Because of their satisfactory frequency behaviour *nnp* transistors will preferably be used in the amplifier. Thus, the second transistor will be of the *pnp* type. This second transistor also provides the voltage-level shift, for the collector of the input transistor is preferably connected to the base of a fourth (or output) transistor through the emitter-collector path of the said second transistor, so that a voltage drop is produced between the input and the output of the amplifier. The third and fourth transistors together form a current amplifier circuit in which the amplification is determined by the ratio between the emitter surface areas of the respective transistors.

Owing to the transistor configuration according to the invention, the additional advantage is obtained that in signal transmission the properties of said second transistor, such as for example its drift, do not play an important part, for only a very small portion of the signal current flows through this transistor. The larger portion, namely a portion $\frac{\beta}{2}$ times greater than that flowing through the second transistor, flows through the third transistor, where β is the current amplification factor of the third transistor. Therefore, when the circuit arrangement according to the invention is used in a differential amplifier, any difference between the corresponding second transistors of the two circuits exert substantially no influence on the circuit.

The use of a transistor of the lateral type adversely affects the high-frequency properties of the amplifier. To prevent this impairment the emitter-collector path of the second transistor may be shunted by a capacitor in known manner. In the circuit arrangement according to the invention this provides the additional advantage that this capacitor can be very small and hence can readily be made in integrated circuit form. The small value of the capacitor is due to the fact that it also shunts the base-collector path of the third transistor and hence is apparently increased by the consequent Miller effect.

The influence of the parasitic capacitance at the input can be further reduced by inserting a current source between the collector of the second transistor and voltage supply terminal. This current source increases the quiescent current of the second transistor. The

load impedance of the input transistor, which before was determined by the gain of the second transistor, now will be reduced by a factor which depends on the adjustment of the aforesaid current source and on the current amplification of the third transistor. Thus, the voltage variations at the collector of the input transistor will be decreased with a consequent decrease of the influence of the parasitic capacitance.

As an alternative, there may be included between the collector of the second transistor and the base of the third transistor the base-emitter path of a further transistor the collector of which is connected to a point of constant potential and the quiescent current of which is provided by the aforesaid current source. By the inclusion of this transistor, which operates as an emitter follower, the load impedance is reduced by a factor which depends on the current amplification of this transistor and on the adjustment of the aforesaid current source.

Thus, with an adjustment of the aforesaid current source equal to the quiescent current of the third transistor, the load impedance of the input transistor will be reduced by a factor equal to the current amplification of the transistor operating as an emitter follower.

When the invention is used in the two branches of a differential amplifier, it may readily be extended so as to have a very high discrimination factor, i.e. the ratio between the sensitivity to difference signals and that to common-mode signals. This need involve merely the addition of two transistors, a diode and a capacitor.

The above and other features of the invention will be described more fully with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram of a first embodiment of an amplifier according to the invention as used in a differential amplifier.

Figure 2 shows a first modification of the amplifier of Figure 1 and

Figure 3 a second modification.

Referring now to Figure 1, there is shown a differential amplifier built up symmetrically from two circuits according to the invention. Since both branches of the circuit arrangement shown are identical in configuration and operation, only one of the branches will be described in detail.

The branch to be described includes an input transistor T_1 of the *nnp* type. The collector of transistor T_1 is connected to the emitter of a transistor T_2 of the *pnp* type which together with transistor T_1 forms a cascode circuit-style arrangement these two transistors being biased from a current source I_1 . The collector of transistor T_2 is connected to the bases of two transistors T_3 and T_4 , both of the *nnp* type, the emitters of which

are connected to the negative terminal “-” of a voltage supply source. The collector of transistor T_4 constitutes one of the output terminals of the circuit arrangement, and the collector of transistor T_3 is connected to the collector of transistor T_1 and, through a current source I_2 , to the positive terminal “+” of the voltage supply source.

The cascode-style arrangement of the transistors T_1 and T_2 ensures suppression of the influence of the parasitic base-collector capacitance of the input transistor T_1 , because the voltage difference between these two electrodes is substantially equal to zero, so that substantially no voltage is set up across that capacitance.

The *pnp* transistor T_2 which may be of the lateral type also provides the desired voltage-level shift between the input and the output of the amplifier, because the emitter-collector path of this transistor, across which a voltage drop is produced, forms the connection between the collector of the input transistor T_1 and the base of the output transistor T_4 . Thus, the circuit arrangement permits both a large common-mode input signal and a large output signal.

In order to reduce the effects of the frequency-sensitive behaviour of the lateral *pnp* transistor T_2 , the emitter-collector path of this transistor is shunted by a capacitor C in known manner. However, this capacitor may be very small and hence will be suitable for integrated circuit technology, because it also shunts the base-collector path of transistor T_2 , so that the value of the capacitor is apparently increased owing to the Miller effect.

The transistors T_3 and T_4 form a current amplifier for of necessity the base-emitter voltages of these two transistors are equal. The ratio between the collector currents and consequently the amplification factor is determined by the ratio between the emitter surface areas of these transistors.

Thus, the circuit arrangement according to the invention simply and efficiently combines a cascode-style operation, voltage-level shifting and satisfactory coupling to the output of the amplifier, whilst it may cover a wide frequency range and yet be suitable for manufacture by integrated circuit techniques.

To suppress the influence of the parasitic input capacitance even more strongly, the circuit arrangement may be extended in the manner shown in Figure 2. The extended modification includes an additional *nnp* transistor T_5 inserted between the collector of transistor T_2 and the base of transistor T_3 , the base of transistor T_5 being connected to the collector of transistor T_2 , whilst the emitter of transistor T_5 is connected to the base of transistor T_3 . The collector of transistor T_5 is connected to a point “+” of constant

potential and its quiescent current is provided by a current source I_2 which connects the base of transistor T_3 to the negative terminal of the supply source. The load impedance of the input transistor T_1 now is reduced by a factor which depends on the adjustment of the current source I_2 and on the current amplification of the transistor T_5 which operates as an emitter follower. Consequently, the voltage variations at the collector of transistor T_1 will be greatly reduced, as will the influence of the parasitic input impedance.

As an alternative, the transistor T_5 may be omitted and the current source I_2 alone may be included in the manner shown, in which case the adjustment of this current source must be chosen to have a suitable value. In this case, the load impedance of the input transistor T_1 will be reduced by a factor which depends on the adjustment of the current source I_2 and on the current amplification of the transistor T_3 .

Figure 3 shows an extended modification of the arrangement shown in Figure 1 which provides a large discrimination factor for the differential amplifier. The emitter of transistor T_3 is connected to the negative terminal of the supply source through the collector-emitter path of a transistor T_7 . The same configuration is used in the emitter circuit of the corresponding transistor T_3' in the opposite branch of the differential amplifier which includes the collector emitter path of a transistor T_6' . The bases of transistor T_6 and T_6' are interconnected. The commoned emitters of the output transistors T_4 and T_4' are connected to the negative terminal of the voltage supply source through a transistor T_7 which is connected as a diode shunting the base emitter paths of transistor T_6 and T_6' . The collectors of transistors T_6 and T_6' are interconnected through a capacitor C . A feature of this circuit arrangement is its large discrimination factor which is due to the fact that the transistors T_6 and T_6' can only absorb the common-mode input signal, since their base emitter voltages necessarily are equal and hence, with equal emitter surface areas, their emitter currents also will be equal. The difference signal perforce provides the base current for transistor T_4 and T_4' and hence is amplified by a factor equal to the current amplification of those transistors. The “diode” T_7 provides the quiescent current setting for transistors T_4 and T_4' , which adjustment is determined by the emitter surface area of T_7 as compared with that of the transistors T_6 and T_6' . The capacitor C forms a possible path for the signal current at high frequencies. Thus, the transistors T_3 and T_4 again operate as a current amplification circuit, the amplification depending on the quiescent current setting of these transistors.

Finally, in the circuit arrangement of

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Figure 3, further transistors, such as T_3 and T_3' in Fig. 2, may also be inserted in order to eliminate the influence of the parasitic input capacitance. This provides the advantage that current sources corresponding to I_2 and I_2' in Fig. 2, may each be constituted by a single transistor (not shown), the collector-emitter paths of which respectively connect the emitters of the transistors corresponding to T_3 and T_3' to the negative terminal of the supply source, and the bases of which are connected respectively to the bases of transistors T_3 and T_3' . The choice of the emitter areas of such "current-source" transistors determines the quiescent current of the added transistors corresponding to T_3 and T_3' .

WHAT WE CLAIM IS:—

1. A wide-band amplifier including a cascode-style arrangement (as hereinbefore defined) of a first transistor of a first conductivity type and a second transistor of a second conductivity type opposite to that of said first type, the connection between the collector of said first transistor and the emitter of said second transistor being additionally connected to the collector of a third transistor of said first conductivity type, the base of said third transistor being connected to the collector of said second transistor whilst its emitter is connected to a voltage supply terminal.

2. A wide-band amplifier as claimed in Claim 1, in integrated circuit form, in which said second transistor is a lateral transistor, a capacitor being connected between the emitter and collector of said second transistor.

3. A wide-band amplifier as claimed in Claim 1, or Claim 2, in which a current source is connected in parallel with the base-emitter path of said third transistor.

4. A wide-band amplifier as claimed in any preceding claim, wherein the connection of the emitter of the third transistor to said voltage supply terminal is effected via the collector-emitter path of a further transistor.

5. A wide-band amplifier as claimed in Claim 4, wherein said third transistor is biased in operation by means of a connection from its base to a current source provided by the collector-emitter path of an additional transistor, the emitter and base of which are respectively connected to corresponding electrodes of said further transistor.

6. A wide-band amplifier as claimed in Claim 3, in which the connection between the collector of said second transistor and the base of said third transistor includes the base-emitter path of a further transistor the collector of which is connected to a point of constant potential.

7. A wide-band amplifier as claimed in any of the preceding Claims, in which the base of said third transistor is connected to the base of a fourth transistor which carries the output current of said amplifier and the emitter of which is connected to a voltage supply terminal.

8. A wide-band differential amplifier in the form of a circuit incorporating first and second amplifiers as claimed in Claim 7, arranged and connected symmetrically, the commoned emitters of the fourth transistors of said first and second amplifiers being connected to a voltage supply terminal through an unidirectional conducting device which is connected in a path in parallel with the base-emitter paths of two further transistors.

9. A wide-band amplifier as claimed in Claim 8, in which the collectors of said two further transistors are interconnected through a capacitor.

10. A wide-band differential amplifier substantially as herein described, with reference to Figure 1, Figure 2 or Figure 3 of the accompanying drawings.

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2. A wide-band amplifier as claimed in Claim 1, in integrated circuit form, in which said second transistor is a lateral transistor, a capacitor being connected between the emitter and collector of said second transistor.

3. A wide-band amplifier as claimed in Claim 1, or Claim 2, in which a current source is connected in parallel with the base-emitter path of said third transistor.

4. A wide-band amplifier as claimed in any preceding claim, wherein the connection of the emitter of the third transistor to said voltage supply terminal is effected via the collector-emitter path of a further transistor.

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