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Method and arrangement for data and clock recovery in a
biphase-coded data signal

The invention relates to a method and an arrangement according to the precharacterising clause of the main claim.

5 There are two types of biphase codes, the so-called biphase mark code and the so-called biphase space code. In the biphase mark code, the logical ones are specially coded, and, in the biphase space code, the logical zeros are specially coded. In the biphase mark code, there is always
10 a change of the logical states between the data bits of the data signal, and in the case of a logical one there is also a change in the data-bit middle, whereas there is not in the case of a logical zero. Lines A and B according to Figure 2 show this relationship. Similar considerations
15 apply to the biphase space code.

For data recovery of such a biphase-coded data signal, the bit clock needs to be recovered on the reception side. To that end, it is known to use a phase-synchronised clock generator (PLL), which is exactly locked to double the bit
20 frequency of the data signal. At substantially high data rates, however, it is difficult to maintain the requisite accurate phase relationship between the clock frequency and the biphase data, which is necessary for reliable data decoding.

25 It is therefore an object of the invention to provide a method with which clock recovery for a biphase-coded data signal is possible even at substantially high data rates.

This object is achieved, on the basis of a method according to the precharacterising clause of the main claim, by the
30 characterising features thereof. Advantageous refinements, in particular concerning a particularly simple arrangement



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for carrying out this method, are given in the dependent claims.

According to the invention, operation is carried out with an uncorrelated clock and, by means of the sampled values
5 and by establishing the bit limits, the original data bits are regenerated from which the bit clock can then be derived in a straightforward way. Particularly accurate clock recovery, which is not susceptible to data jitter and to clock inaccuracies, is obtained when the phase-locked
10 oscillator delivering the sampling frequency is synchronised with the biphasic data recovered in this way.

The method according to the invention can be used for both biphasic-mark-coded and biphasic-space-coded data signals.

The invention will be explained in more detail below with
15 the aid of schematic drawings with reference to an exemplary embodiment for a biphasic-mark-coded signal.

Figure 1 shows the block diagram of an arrangement according to the invention for carrying out the method according to the invention, and Figure 2 shows the
20 associated signal waveforms.

The biphasic-mark-coded data signal B, which is derived from the NRZ data signal A and is to be regenerated, is delivered on the reception side to a sampling circuit 1, downstream of which a detector 2 is arranged. The sampling
25 frequency C for the sampling circuit 1, and the clock frequency for the detector 2, are delivered by a phase-locked oscillator 3 whose output frequency is selected to be 2.5 times as great as the bit frequency of the data signal B. Using the sampling signal C of the oscillator 3,
30 the biphasic data signal B is sampled in the sampling circuit 1, and the sampled values D obtained in this way

are delivered to the detector 2. In order to obtain as many sampled values as possible, sampling is carried out in the sampling circuit 1 with both the positive and negative edges of the sampling signal C. With 2.5 times the bit frequency as the sampling frequency, in theory five sampled values per data bit are obtained. Subject to effects such as data jitter and clock accuracy of the biphase data B, however, four or six sampled values D may also be obtained for one data bit. This is established in the detector 2. In this way, the bit limits E can be established in the detector from the successive sampled values D, since, according to the biphase mark code, a transition between zero and one implies either a change between the data bits of the data signal B or a change in the bit middle.

Therefore, if the detector 2 establishes a change of the logical state one and zero in the tolerance range of from 4 to 6 sampled values, then this implies a logical zero in the regenerated data signal F, whereas if a change of the sampled values D is established in a substantially short interval, for example after just two logical ones, then this implies a one in the regenerated data signal F. It is then possible to regenerate the associated bit-clock frequency G in a straightforward way from the thus regenerated data bits F of the original signal A. -Both the data bits and the bit clock of the original data signal A are hence regenerated. The detector 2 may be configured with a very high tolerance and, in the exemplary embodiment, it is merely necessary for it to reliably recognise the bits with 4, 5 or 6 sampled values. The detector is therefore tolerant with respect to data jitter and clock accuracy. The data and clock recovery will be even more accurate if the oscillator 3 is synchronised with the bit clock G recovered in this way, as is schematically indicated by the active connection 4 in Figure 1.

The serially regenerated data bits F, with the associated bit clock G, can subsequently be converted into parallel data in the known way by means of a serial/parallel converter 5, and the byte clock obtained thereby can

5 likewise be used for synchronising the oscillator 3, in the scope of the active connection 6 according to Figure 1, in order to synchronise the sampling clock accurately with the biphase data.

CLAIMS:

1. Method for data and clock recovery in a biphas-coded data signal,
characterised in that
5 the data signal is sampled using a sampling frequency which is greater than double the bit frequency of the data signal, the bit limits of the data signal are determined from the sampled values obtained in this way
and the data bits and the associated bit clock of the data
10 signal are then regenerated therefrom.
2. Method according to Claim 1.
characterised in that
the sampling frequency is selected to be 2.5 times as great
15 as the bit frequency.
3. Method according to Claim 1 or 2.
characterised in that
the clock generator generating the sampling frequency is
20 synchronised using the regenerated bit clock.
4. Method according to one of the preceding claims,
characterised in that
the regenerated serial data signal is parallel-converted
25 and the clock generator is synchronised using the byte clock obtained in this case.
5. Arrangement for carrying out the method according to one of claims 1 to 4,
30 characterised by a sampling circuit (1), a phase-synchronised oscillator (3) generating the sampling frequency (C) with a sampling frequency of at least 2.5 times the bit frequency, a downstream detector (2), which is clocked with the sampling frequency (C) of the phase-

locked oscillator (3) and in which the bit limits (E) of the data signal are determined from the transitions of the sampled values (D) between the logical states (zero, one), and the data bits (F) and the associated bit clock (G) are
5 then regenerated therefrom.