

SUBSTRATE FOR RADIOFREQUENCY APPLICATIONS AND ASSOCIATED
FABRICATION PROCESS

5 **FIELD OF THE INVENTION**

 The present invention relates to the field of integrated
radiofrequency devices. It in particular relates to a substrate
suitable for said devices and to an associated fabrication
10 process.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

15 In most applications involving the transmission or
reception of radiofrequency signals (10 MHz to 100 GHz), device
fabrication requires a substrate that meets an increasingly
demanding set of specifications, in particular resulting from
the evolution of mobile telephony standards (2G, 3G, LTE, LTE
20 Advanced, LTE Advanced PRO, 5G etc.). The properties of the
materials of the substrate must in particular guarantee:

- low insertion losses (low attenuation of the signal) and
a good linearity (low distortion of the signal, cause of
harmonics), typically achieved via an effective
25 resistivity, over a wide frequency range, higher than
1000 ohms.cm;
- temperature stability of these figures of merit, in
particular in the operating range of the devices [-40°C;
150°C];
- 30 - a low capacitive coupling between the active layer and
the carrier substrate, typically achieved by virtue of a
dielectric permittivity equal to or lower than that of
silicon ($\epsilon_{\text{silicon}} = 11$).

Moreover, to meet the need for high volumes, the substrate must be compatible with the semiconductor industry, and in particular with silicon CMOS fabrication lines. Of course, it must in addition have a competitive cost in order to be adopted in mass-market applications, in particular in the field of telecommunications (cellular networks and telephony, Wi-Fi connectivity, Bluetooth).

Radiofrequency (RF) devices, such as antenna adapters and switches, power amplifiers, low-noise amplifiers or even passive (R, L, C) components may be produced on various types of substrates.

For example silicon-on-sapphire (SOS) substrates are known, this type of substrate allowing components produced in microelectronic technologies in the silicon surface layer to benefit from the insulating properties of the sapphire substrate, which are independent of temperature, from its thermal conductivity, which is higher than 20 W/m.K, and from its permittivity, which is lower than 11. For example, antenna switches and power amplifiers fabricated on this type of substrate have very good figures of merit but are mainly used for niche applications because of the very high overall cost of this solution.

Substrates based on high-resistivity silicon comprising a carrier layer, a trapping layer (of a few hundred nanometres to a few microns in thickness) placed on the carrier substrate, a dielectric layer placed on the trapping layer, and a semiconductor layer placed on the dielectric layer are also known. The carrier substrate usually has a resistivity higher than 1 kOhm.cm. The trapping layer may comprise undoped polysilicon. The combination of a carrier substrate made of high-resistivity silicon and a trapping layer according to the prior art allows the parasitic conduction layer usually present under the buried oxide layer in HR SOI substrates (silicon-on-

insulator substrates with a carrier substrate made of high-resistivity silicon) to be removed. The reader will find a review of the performance of RF devices fabricated on a known prior-art high-resistivity semiconductor substrate in "Silicon-on-insulator (SOI) Technology, manufacture and applications", sections 10.7 and 10.8, Oleg Kononchuk and Bich-Yen Nguyen, published by Woodhead Publishing.

Nevertheless, a polysilicon trapping layer has the drawback of undergoing partial recrystallization in high-temperature heat-treatment steps, this contributing to decreasing the density of traps in the layer. The degradation of the performance of the RF device related to this decrease in trap density may be unacceptable for certain applications. Moreover, it is not easy with these substrates to guarantee stability in RF performance over the entire temperature range of use, in particular above 100°C: their resistivity drops on account of the generation of thermal carriers in the carrier substrate and device/substrate coupling becomes a major contributor to signal attenuation and distortion.

To improve the performance of these substrates, it could be envisioned to increase the thickness of the trapping layer (beyond a few microns), in order to increase the number of available traps and to increase the distance between the carrier substrate and the devices, thus limiting the impact of the thermal carriers generated in the carrier substrate. This option nevertheless has the drawback of increasing the stress on and the bow of the substrates, which become difficult or even impossible to process in standard microelectronic equipment.

Other carrier substrates, such as substrates made of aluminium nitride or silicon carbide, meet the specifications in terms of RF properties but they are not directly compatible with standard semiconductor-industry technology. Their use as a carrier substrate of a transferred final device layer is

envisionable; nevertheless, the cost of these specific materials combined with that of circuit-transfer technologies is still too high for mass adoption of these solutions.

OBJECT OF THE INVENTION

Embodiments of the invention seek to provide a substrate suitable for radiofrequency applications, which may remedy all or some of the drawbacks of the prior art.

BRIEF DESCRIPTION OF THE INVENTION

An aspect of the invention provides a substrate for radiofrequency microelectronic devices comprising a carrier substrate, an intermediate layer, a useful layer arranged on the intermediate layer, characterized in that the carrier substrate is made of a semiconductor material and in that the substrate comprises a sintered composite layer which is arranged on the carrier substrate and is formed from a powder mixture of at least a first dielectric material and a second dielectric material different from the first, the nature of the first material, the nature of the second material, and the proportion of said materials in the powder mixture being selected to provide the sintered composite layer with a thermal expansion coefficient matching that of the carrier substrate within plus or minus 30%, said sintered composite layer having a thickness of between 5 microns and 100 microns, the intermediate layer being arranged on the sintered composite layer.

According to advantageous features of the invention, taken alone or in combination:

- the thermal expansion coefficient of the sintered composite layer is matched with that of the carrier substrate, to plus or minus 10%, or even to plus or minus 5%;
- the carrier substrate has a resistivity higher than 500 ohm.cm;
- the carrier substrate is made of silicon;

- the first and second dielectrics are chosen from silicon oxide, silicon nitride, aluminium nitride, alumina, and mullite;
- the substrate comprises a protective layer placed between the carrier substrate and the sintered composite layer;
- the substrate comprises an intermediate layer placed on the sintered composite layer;
- the intermediate layer is a dielectric layer formed from a material chosen from a silicon oxide, a silicon nitride, a silicon oxynitride, and an aluminium nitride;
- the substrate comprises a useful layer placed on the intermediate layer;
- the useful layer is composed of a material chosen from the semiconductors, insulators or conductors, or even the piezoelectrics.

Another aspect of the invention provides a radiofrequency-microelectronic-device structure comprising:

- a substrate such as above;
- a layer of microelectronic devices arranged on said substrate.

According to example embodiments, the microelectronic device is an antenna adapter or switch or a power amplifier or a low-noise amplifier or a passive component or other circuit operating at high frequency or a radiofrequency MEMS component or even a radiofrequency filter.

Another aspect of the invention provides a method for producing a substrate for radiofrequency microelectronic devices, comprising the following steps:

- a) Providing a carrier substrate made of a semiconductor material having a first surface;
- b) Depositing a layer, which is formed of a powder mixture of at least a first dielectric material and a second dielectric material different from the first, on the first surface of the carrier substrate;
- c) Sintering the layer formed from the powder mixture in order to obtain a sintered composite layer secured to the first surface of the carrier substrate and having a thickness of between 5 microns and 100 microns; the first material, the second material and the proportion of said materials in the powder mixture being selected to provide the sintered composite layer a thermal expansion coefficient matching that of the carrier substrate within more or less 30%;
- d) Assembling a useful layer and the carrier substrate so as to arrange the sintered composite layer between the useful layer and the carrier substrate, an intermediate layer being arranged between the useful layer and the sintered composite layer.

According to advantageous features of the invention, taken alone or in combination:

- the first side of the carrier substrate comprises a protective layer, prior to the deposition of the layer formed from the mixture of powders in step b);
- the protective layer is formed by at least one material chosen from silicon nitride, silicon oxynitride, and silicon oxide;
- the mixture of powders takes the form of a viscous paste, and the layer formed by said mixture is deposited, in step b), by spin coating;

- the deposition of the layer formed by the mixture of powders is followed by a low-temperature heat treatment in order to remove at least one liquid component from the viscous paste;
- the process comprises, after step c), a step d) of bonding a useful layer and the carrier substrate so as to place the sintered composite layer between the useful layer and the carrier substrate;

- an intermediate layer is placed between the useful layer and the sintered composite layer;
- the useful layer provided for bonding step d) is a donor substrate composed of a material chosen from the semiconductors, insulators or conductors, or even the piezoelectrics;
- the process comprises a step e) of thinning the donor substrate to the thickness desired for the useful layer for the fabrication of the radiofrequency microelectronic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will become apparent from the following detailed description of the invention, which description is given with reference to the appended figures, in which:

- Figure 1a shows a substrate according to the invention;
- Table 1 gives the properties of materials from which the sintered composite layer of a substrate according to the invention is liable to be composed;
- Figure 1b shows a graph showing the temperature at which the bow of a substrate (made of silicon of 750 microns thickness) reaches 150 microns, as a function of the thermal expansion coefficient of the composite layer (5 microns thickness) placed on this substrate and for various Young's moduli of said composite layer;
- Figures 2a, 2b, 3a and 3b show substrates according to the invention;
- Figure 4 shows a radiofrequency-microelectronic-device structure according to the invention;

- Figures 5a to 5e show a process for fabricating a substrate according to the invention.

5

DETAILED DESCRIPTION OF THE INVENTION

In the description, the same references in the figures might be used for elements of the same type. The figures are schematic representations which, for the sake of legibility, are not to scale. In particular, the thicknesses of the layers along the z-axis are not to scale with respect to their lateral dimensions along the x- and y-axes; and the relative thicknesses of the layers with respect to one another are not necessarily respected in the figures.

15

The invention relates to a substrate 10 suitable for the fabrication of radiofrequency microelectronic devices, comprising a carrier substrate 1 made of a semiconductor (Figure 1a). Advantageously, the carrier substrate 1 is formed from a single-crystal silicon.

20

The substrate 10 according to the invention also comprises a sintered composite layer 2 placed on the carrier substrate 1 and formed from powders of at least two different dielectrics (Figure 1a). By sintered layer what is meant is a layer resulting from the consolidation of a mixture of powders: this consolidation is obtained by input of thermal energy and optionally mechanical energy, but without melting at least one of the pulverulent materials of the mixture. The sintered nature of the composite layer may therefore be detected by structural analysis of said layer (for example by scanning electron microscopy). The particles or grains of the dielectric powders appear welded together and the density of the composite layer

30

depends on the degree of compaction of the mixture during the input of energy for the consolidation.

The particles forming the powder of each of the dielectrics of the sintered composite layer 2 have dimensions that follow a typically Gaussian distribution. In the remainder of the description, the mean size of the particles will be likened to the equivalent mean diameter of the particles of a given material. The mean size of the particles may typically vary between about 1 micron and 10 microns.

Preferably, the at least two dielectrics composing the sintered composite layer 2 (called the first and second dielectrics) are chosen from silicon oxide, silicon nitride, aluminium nitride, alumina, and mullite (Table 1), in particular because of the high resistivity of these materials and their compatibility with high-temperature treatments.

The sintered composite layer 2 optionally might comprise three or more different dielectrics.

The sintered composite layer 2 furthermore has a thickness greater than 5 microns, or even greater than 10 microns. The thickness of the sintered composite layer 2 is chosen depending on the type of radiofrequency microelectronic devices intended to be produced on the substrate 10.

In general, it will have a thickness comprised between 10 microns and 100 microns in order to prevent or at least limit the penetration of the electromagnetic field generated by the RF devices into the carrier substrate 1: thus, the interaction of this electromagnetic field with free carriers (for example thermal carriers) liable to appear in the carrier substrate 1 is also limited.

To limit the penetration of the electromagnetic field, the first and second dielectrics will possibly preferably be chosen in order to best decrease the equivalent permittivity of the sintered composite layer 2. A low permittivity (typically

lower than 11, the permittivity of silicon) will permit the implementation of smaller thicknesses of composite layer 2.

If the penetration of the electromagnetic field is confined to the sintered composite layer 2, the carrier substrate 1 will be able to have a standard resistivity (typically a few tens of ohms.cm). If the electromagnetic field is liable to penetrate relatively deeply into the carrier substrate 1, the resistivity of said carrier substrate 1 will advantageously be chosen to be higher than 500 ohm.cm, or even than 1 kohm.cm.

The sintered composite layer 2 also has a thermal expansion coefficient (CTE) that is matched with that of the carrier substrate 1. The thermal expansion coefficient of the composite layer 2 is defined by the mean of the thermal expansion coefficients of the constituent dielectrics of said layer 2, weighted by their volume fraction in the composite layer 2. By "matched with the thermal expansion coefficient of the carrier substrate 1", what is meant is as close as possible to said thermal expansion coefficient. According to the invention, the CTE of the sintered composite layer 2 is to within plus or minus 30% of the value of the CTE of the carrier substrate 1. Advantageously, it is to within plus or minus 10% of the value of the CTE of the carrier substrate 1, or even plus or minus 5%, or even closer than plus or minus 3% or plus or minus 1%.

By way of example, a sintered composite layer 2 formed from powders of silicon oxide (SiO_2) and alumina (Al_2O_3), in proportions of 1 volume of Al_2O_3 to 2.7 volumes of SiO_2 , has a thermal expansion coefficient ($\text{CTE } 2.67 \times 10^{-6} / ^\circ\text{K}$) that is matched to the thermal expansion coefficient of a carrier substrate 1 made of silicon ($2.6 \times 10^{-6} / ^\circ\text{K}$), the difference, in this case, being smaller than 3%.

Advantageously, the CTE of the composite layer 2 is chosen so that the substrate 10, equipped with the composite layer 2, has a thickness larger than 5 microns, and so that its bow does not exceed about 150 microns during the microelectronic processes used to produce the constituent layers of the substrate 10 and components in and on the substrate 10. It will be recalled that said microelectronic processes will possibly in particular comprise heat treatments at high temperatures, ranging from 900°C to 1150°C for example.

By way of illustration, the graph in Figure 1b shows the temperature at which the bow of a substrate 10 (the carrier substrate 1 being made of silicon, of 750 microns thickness and of 300 mm diameter) reaches 150 microns, as a function of the thermal expansion coefficient of the composite layer 2 (5 microns thickness) placed on this substrate and for various Young's moduli of said composite layer 2.

For example, for a maximum treatment temperature of 900°C, if the composite layer 2 has an equivalent Young's modulus (defined as the mean of the Young's moduli of the constituent dielectrics of said layer 2, weighted by their volume fraction) of about 70 GPa, the CTE of the composite layer 2 must differ by at most +/- 30% from the value of the CTE of the carrier substrate 1, to remain below the solid curve (i.e. to keep the bow of the substrate 10 below 150 microns).

According to another example, for a maximum treatment temperature of 1100°C, if the composite layer 2 has an equivalent Young's modulus of about 150 GPa, the CTE of the composite layer 2 must differ by at most +/- 11% from the value of the CTE of the carrier substrate 1, to remain below the dashed curve corresponding to "E = 150 GPa" (i.e. to keep the bow of the substrate 10 below 150 microns).

According to one variant, the substrate 10 may comprise a protective layer 3 placed between the carrier substrate 1 and the sintered composite layer 2. As illustrated in Figures 2a and 2b, the substrate 10 comprises in this case a protective layer 3 placed on its first side 1a, and potentially on the second side 1b and on the edge faces of said carrier substrate 1 (Figure 2b). As will be seen in the description of the fabrication process of the substrate 10, the protective layer 3 makes it possible to avoid or at least limit the diffusion of impurities contained in the sintered composite layer 2, or present during the production of said layer 2, into the carrier substrate 1.

For the fabrication of microelectronic devices on the substrate 10, a useful layer 5 is usually required; it is named "useful" because the devices will subsequently be produced in or on this layer 5.

The substrate 10 according to the invention may thus comprise a useful layer 5 placed on the sintered composite layer 2. The useful layer 5 will possibly be composed of a material chosen from the semiconductors (including silicon, silicon-germanium, germanium, silicon carbide, etc.), insulators or conductors, or even the piezoelectrics (including lithium niobate, lithium tantalate, etc.).

According to one advantageous embodiment, the substrate 10 comprises an intermediate layer 4 placed on the sintered composite layer 2 (Figure 3a) and which may optionally completely encapsulate said composite layer (Figure 3b). The intermediate layer 4 will possibly be a dielectric layer formed from a material chosen from a silicon oxide, a silicon nitride, a silicon oxynitride, and an aluminium nitride, etc.

The useful layer 5 is then placed on the intermediate layer 4. The function of the intermediate layer 4 may in particular be to electrically insulate the useful layer 5 and

the composite layer 2 from each other, and/or to form a barrier to diffusion preventing contamination of the useful layer 5 by impurities present in the sintered composite layer 2.

5 The substrate 10 according to the invention comprises a sintered composite layer 2 having the properties of a dielectric and a thermal expansion coefficient that is matched to that of the subjacent carrier substrate 1. The thickness of the composite layer 2 may be chosen depending on the RF microelectronic devices
10 intended to be produced on the substrate 10, so as to prevent (or greatly limit) the penetration of electromagnetic waves into the carrier substrate 1. Since the thermal expansion coefficient of the composite layer 2 is matched with that of the carrier substrate 1, there is no need to limit the thickness of the
15 sintered composite layer 2 for reasons of the stresses and bow induced in the substrate 10.

As described above, the thermal expansion coefficient may be chosen so that, during the heat treatments applied to the substrate 10 to produce the useful layer 5 or the microelectronic
20 devices 20 (typically between 900° and 1150°C), the amplitude of the bow of said substrate is kept below a threshold compatible with standard steps and standard microelectronic equipment; in particular, a bow lower than 150 microns will be targeted for a substrate of 300 mm diameter.

25

The sintered composite layer 2, because of its dielectric character and its suitable thickness, thus provides the substrate 10 with the properties required to guarantee:

30 - low insertion losses (low attenuation of the signal) and a good linearity (low distortion of the signal, cause of harmonics);

- temperature stability of its figures of merit, in particular in the operating range of the devices $[-40^{\circ}\text{C}; 150^{\circ}\text{C}]$;
- a low capacitive coupling between the useful layer and the carrier substrate, typically achieved by virtue of a dielectric permittivity equal to or lower than that of silicon ($\epsilon_{\text{silicon}} = 11$).

The invention also relates to a process for fabricating a substrate suitable for radiofrequency microelectronic devices, as presented in Figures 5a to 5e.

The process firstly comprises a step a) of providing a carrier substrate 1 made of semiconductor. The carrier substrate 1 has a front side, called the first side 1a and a back side, called the second side 1b (Figure 5a).

The process then comprises a step b) comprising depositing a layer 2' formed from a mixture of powders of at least a first dielectric and a second dielectric different from the first, on the first side 1a of the carrier substrate 1.

Optionally, the first side 1a of the carrier substrate 1 comprises a protective layer 3 produced prior to the deposition of the layer 2' of mixture of powders; the protective layer 3 may, as illustrated in Figure 5b, completely encapsulate the carrier substrate 1, i.e. cover its back side 1b and its edge face. The protective layer 3 is formed by at least one material chosen from silicon nitride, a silicon oxynitride and a silicon oxide, and may be produced using various known chemical-deposition techniques. It makes it possible to avoid or at least to limit the diffusion of impurities contained in the layer 2' into the carrier substrate 1.

According to a first variant embodiment, the mixture of powders takes the form of a viscous paste.

Such a paste is customarily obtained by adding a liquid compound, of solvent type (in particular alcohol, for example ethanol), to the dry mixture of powders. Typically, the powders used contain particles the average size of which is comprised between about 1 and 10 microns. To form composite layers 2 of 5 to 10 microns thickness, the smallest sizes of particles will be preferred.

Alternatively, the mixture of powders may be incorporated into a silicon-based polymer matrix (polymer-derived ceramics or PDCs) that is able to be converted into ceramic at high temperature. It will be noted that in the case of a layer 2' with a PDC matrix, the sintered composite layer 2 that will subsequently be obtained will comprise the first and second dielectric of the mixture of powders, but also silicon originating from the conversion of the matrix into ceramic. Advantageously, a content of less than 30% silicon and in the composite layer 2 will be targeted. Since interstices are localized and not continuous in the composite layer 2, the presence of silicon in said interstices does not affect the dielectric character of the composite layer 2.

The layer 2' formed by said mixture in step b) is preferentially deposited by spin coating or dip coating or screen-printing through a mask.

The viscosity of the paste is adjusted via the ratio of the powders/liquid compound (solvent and/or polymer). It is chosen in order to allow a uniform deposition of the layer 2', at thicknesses larger than 5 microns, or even larger than 10 microns, and of up to about 100 microns.

The deposition of the layer 2' is followed by a heat treatment at low temperatures (for example between 150°C and 400°C) allowing the solvent(s) to be removed from the layer 2'

and any degassing subsequently in the process, in particular after the bonding step (described below), to be avoided.

5 According to a second variant embodiment, the mixture of powders takes the form of a dry pulverulent and is deposited in a layer 2' on the first side 1a of the carrier substrate 1. This layer 2' may be shaped by compression moulding or hot isostatic pressing. In both cases, a compressive stress is applied to the
10 layer 2' to firmly attach the particles of the powders of the mixture to one another and to the first side 1a. A specific tool is needed to hold the pulverulent mixture on the substrate and to apply a uniform compressive stress to the entire surface of said substrate 1.

15 The fabrication process according to the invention comprises a step c) comprising sintering the layer 2' formed from the mixture of powders, to obtain a sintered composite layer
20 2 that is firmly attached to the first side 1a of the carrier substrate 1 (Figure 5c).

 The sintering is customarily performed at high temperatures, typically above 1000°C, for a duration that may range from a few hours to around 24 hours. The sintering
25 temperature nevertheless remains below the melting point of at least one of the powders contained in the layer 2'. Under the effect of the heat, the particles of the powders are welded together, thereby achieving cohesion of the resulting composite layer 2. The composite layer 2 is also firmly attached to the
30 first side 1a of the carrier substrate 1.

 Optionally, the sintering may in addition be carried out under mechanical stress, which makes it possible to further compact the composite layer 2.

The sintered composite layer 2 is thus composed of particles of the first and second dielectric. Between the particles, depending on the degree of compaction, there may be more or fewer empty interstices (or interstices containing the ceramic resulting from a PDC matrix). Depending on the particle size distribution, the volume fraction of these interstices could reach about 50%, and will preferentially be kept below 25%, or even below 15%, in order to provide the composite layer 2 with a good mechanical strength. It will be noted that the interstices increase the density of traps (for mobile electric charges), this possibly being advantageous with regard to maintaining the high resistivity of the substrate (trapping layer).

The thickness of the layer 2' deposited in step b) is chosen so as to obtain the thickness desired for the sintered composite layer 2. Specifically, depending on the type of layer 2' deposited (in form of a paste with solvent and/or polymer or in dry form), the decrease in thickness during the sintering step will be greater or lesser. Depending on the circumstances, a decrease in volume of the layer 2' of about 10 to 30% may take place.

At the end of the sintering step, the sintered composite layer 2 according to the invention must have a thickness larger than 5 microns.

In addition, according to the present invention, the nature of the first dielectric, the nature of the second dielectric and the proportion of said dielectrics in the mixture of powders is chosen to give the sintered composite layer 2 a thermal expansion coefficient that is matched with that of the carrier substrate 2, to within better than plus or minus 30%.

Advantageously, as illustrated in Figure 5c, the first side 1a of the carrier substrate 1 comprises a protective layer 3, prior to the deposition of the layer formed from the mixture of powders in step b). The protective layer 3 is formed by at least one material chosen from silicon nitride, silicon oxynitride, and silicon oxide.

The fabrication process furthermore comprises, after step c), a step d) of bonding a useful layer 5 and the carrier substrate 1 so as to place the sintered composite layer 2 between the useful layer 5 and the carrier substrate 1. The useful layer 5 will possibly be composed of a material chosen from the semiconductors, insulators or conductors, or even the piezoelectrics. It will possibly for example be made of silicon, of silicon-germanium, of germanium, of a III-V material, of lithium niobate, of lithium tantalate, of aluminium nitride, of PZT, etc.

Preferentially, an intermediate layer 4 is deposited on the composite layer 2, prior to the bonding step d). By way of example, its thickness will possibly vary between a few nanometres and a few microns. Advantageously, the intermediate layer 4 is formed from a material chosen from silicon oxide, silicon nitride, a silicon oxynitride, and aluminium nitride. It will possibly be deposited by various known chemical-deposition techniques.

On the one hand, this intermediate layer 4 encapsulates the sintered composite layer 2, avoiding or at least limiting the risk of cross-contamination between the various layers of the substrate 10 according to the invention; on the other hand, the intermediate layer 4 may be advantageous with a view to

achieving a bond with the useful layer 5, as it will allow the surface of said intermediate layer 4 to be prepared in a conventional way, and not in a way specific to the composition of the sintered composite layer 2.

5

Advantageously, the bonding step is a step of direct bonding, by molecular adhesion, of the two surfaces brought into contact: i.e. of the first side 5a of the useful layer 5 and of the free side of the composite layer 2. The principle of molecular adhesion, which is well known in the prior art, will not be described in further detail here.

Alternatively, the bonding could be achieved by addition of a layer of adhesive material, or by any other bonding technique suitable for the intended application.

15 In most bonding processes, the substrates to be assembled are required to have a good surface finish (cleanliness, low roughness, etc.).

According to one variant, the useful layer 5 provided for bonding step d) is a donor substrate 5' composed of a material chosen from the semiconductors, insulators or conductors, or even the piezoelectrics (Figure 5d).

The fabrication process then comprises a step e) of thinning the donor substrate 5', from its back side 5b', to the thickness desired for the useful layer 5 for the fabrication of the radiofrequency microelectronic devices.

By way of example, the thinning step, step e), may be based on thin-film transfer processes known to those skilled in the art, among which:

- 30 - the SmartCut™ process, which is based on implantation of light hydrogen and/or helium ions into a donor substrate (before the bonding step); a detaching step (after the bonding step) then allows a thin surface layer (the useful layer) to be separated from the donor substrate, level with

the weakened plane defined by the implantation depth of the ions. Finishing steps, possibly including high-temperature heat treatments, lastly give the useful layer 5 the required surface and crystal quality. This process is particularly

- the SmartCut process followed by a step of epitaxy, in particular allowing thicker useful layers, for example of a few tens of nanometres to 20 μm thickness, to be obtained.
- mechanical, chemical and/or chemical-mechanical thinning processes; they consist in thinning the donor substrate from its back side to the thickness desired for the useful layer, for example by grinding and polishing (chemical-mechanical polishing or CMP). These processes are particularly suitable for the transfer of what are referred to as thick layers, for example layers of a thickness of a few microns to several tens of microns, or indeed of as much as a few hundred microns.

As mentioned above, the step e) of thinning will possibly comprise heat treatments for finishing the side 5b of the useful layer 5. The substrate 10 resists heat treatments well, even heat treatments at high temperatures (900°C to 1100°C, or even 1200°C), in particular because the sintered composite layer 2 has a thermal expansion coefficient that is matched with that of the carrier substrate 1, thus limiting the associated stress and bow (curvature) of the substrate 10.

The invention also relates to a radiofrequency-microelectronic-device structure 100 comprising:

- a substrate 10 such as described above;

- a layer 20 of microelectronic devices, which layer is produced on said substrate 10 (Figure 4) and in particular on the side 5b of the useful layer 5.

5 The microelectronic device will possibly be an antenna adapter or switch or a power amplifier or a low-noise amplifier or a passive component or other circuit operating at high frequency or a radiofrequency MEMS component or a radiofrequency filter.

10

 Of course, the invention is not limited to the described embodiments and examples and variant embodiments thereof may be envisaged which do not depart from the scope of the invention
15 such as defined by the claims.

CLAIMS

1. Substrate for radio-frequency microelectronic devices,
comprising:

- a carrier substrate,
- an intermediate layer,
- a useful layer arranged on the intermediate layer,

characterized in that the carrier substrate is made of semiconductor material and in that the substrate comprises a sintered composite layer which is arranged on the carrier substrate and is formed from a powder mixture of at least a first dielectric material and a second dielectric material different from the first, the nature of the first material, the nature of the second material, and the proportion of said materials in the powder mixture being selected to provide the sintered composite layer with a thermal expansion coefficient matching that of the carrier substrate within plus or minus 30%, said sintered composite layer having a thickness of between 5 microns and 100 microns, the intermediate layer being arranged on the sintered composite layer.

2. Substrate for radio-frequency microelectronic devices according to the preceding claim, wherein the sintered composite layer has a thickness of between 10 microns and 100 microns.

3. Substrate for radio-frequency microelectronic devices according to either of the preceding claims, wherein the resistivity of the carrier substrate is higher than 500 ohm.cm.

4. Substrate for radio-frequency microelectronic devices according to any of the preceding claims, wherein the first carrier substrate is silicon.

5. Substrate for radio-frequency microelectronic devices according to any of the preceding claims, wherein the first and second dielectric materials are selected from silicon oxide, silicon nitride, aluminum nitride, alumina, mullite.

5

6. Substrate for radio-frequency microelectronic devices according to any of the preceding claims, comprising a protective layer arranged between the carrier substrate and the sintered composite layer.

10

7. Substrate for radio-frequency microelectronic devices according to any of the preceding claims, wherein the intermediate layer is a dielectric layer formed of a material selected from a silicon oxide, a silicon nitride, a silicon oxynitride, an aluminum nitride.

15

8. Substrate for radio-frequency microelectronic devices according to any of the preceding claims, wherein the useful layer is composed of a material selected from semiconductor, insulating or conductive materials, or even piezoelectric materials.

20

9. Structure of radio-frequency microelectronic devices comprising:

25

- a substrate according to the preceding claim;

- a layer of microelectronic devices arranged on said substrate.

30

10. Structure of radio-frequency microelectronic devices according to the preceding claim, wherein the microelectronic device is an antenna switch or adapter or a power amplifier or a low noise amplifier or a passive component or other circuit operating at high frequency or an MEMS radio-frequency component or a radio-frequency filter.

35

11. Method for producing a substrate for radio-frequency microelectronic devices, characterized in that it comprises the following steps:

5 a) providing a carrier substrate made of a semiconductor material having a first surface;

10 b) depositing a layer, which is formed of a powder mixture of at least a first dielectric material and a second dielectric material different from the first, on the first surface of the carrier substrate;

15 c) sintering the layer formed of the powder mixture to obtain a sintered composite layer secured to the first surface of the carrier substrate and having a thickness of between 5 microns and 100 microns; the first material, the second material and the proportion of said materials in the powder mixture being selected to provide the sintered composite layer with a thermal expansion coefficient matching that of the carrier substrate
20 within more or less 30%;

25 d) assembling a useful layer and the carrier substrate so as to arrange the sintered composite layer between the useful layer and the carrier substrate, an intermediate layer being arranged between the useful layer and the sintered composite layer.

30 12. Method for producing a substrate for radio-frequency microelectronic devices according to the preceding claim, wherein the first surface of the carrier substrate comprises a protective layer, prior to the deposition of the layer formed of the powder mixture from step b).

35 13. Method for producing a substrate for radio-frequency microelectronic devices according to the preceding claim, wherein the protective layer is formed by at least one material

selected from silicon nitride, silicon oxynitride, silicon oxide.

5 14. Method for producing a substrate for radio-frequency microelectronic devices according to any of the three preceding claims, wherein the powder mixture is in the form of a viscous paste, and the deposition of the layer formed by said mixture in step b) is carried out by spin coating.

10 15. Method for producing a substrate for radio-frequency microelectronic devices according to the preceding claim, wherein the deposition of the layer formed by the powder mixture is followed by a low-temperature heat treatment to remove at least one liquid component from the viscous paste.

15 16. Method for producing a substrate for radio-frequency microelectronic devices according to one of the two preceding claims, wherein the useful layer provided for the assembly step d) is a donor substrate composed of a material selected from
20 semiconductor, insulating or conductive materials, or even piezoelectric materials.

25 17. Method for producing a substrate for radio-frequency microelectronic devices according to the preceding claim, comprising a step e) of thinning the donor substrate to the desired thickness of the useful layer for the production of radio-frequency microelectronic devices.