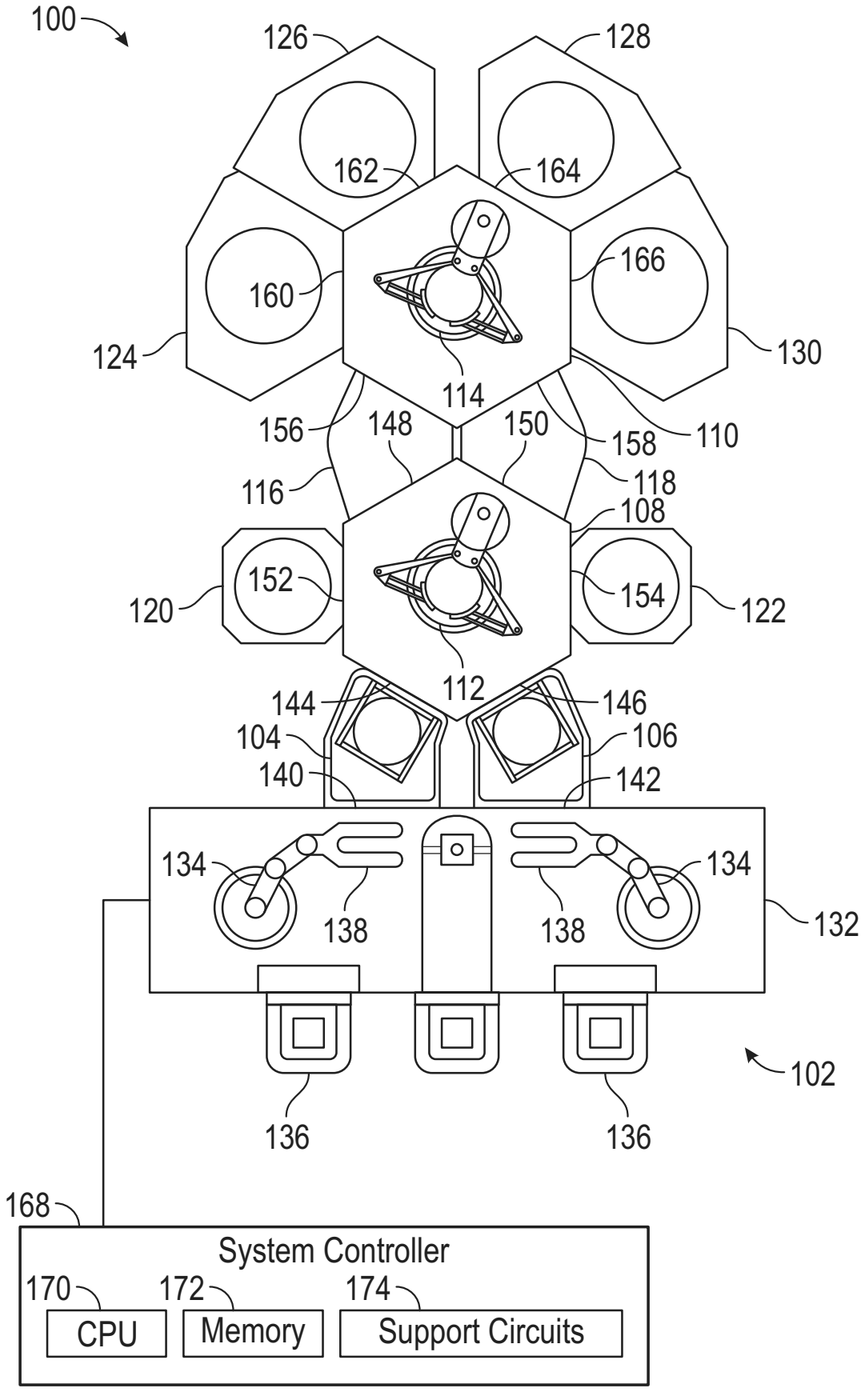

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CPU
Memory
Support Circuits

FIG. 1

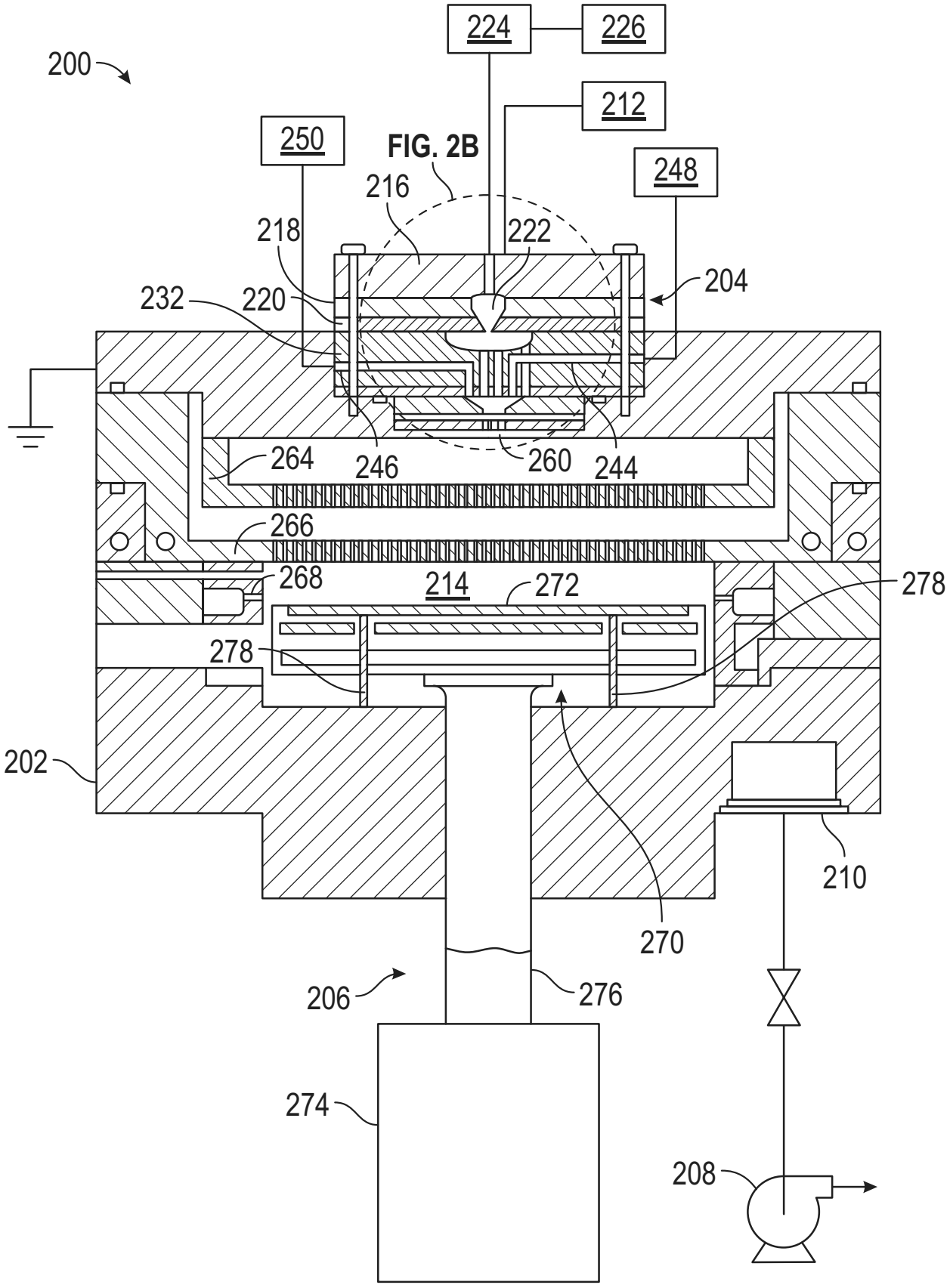

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FIG. 2A

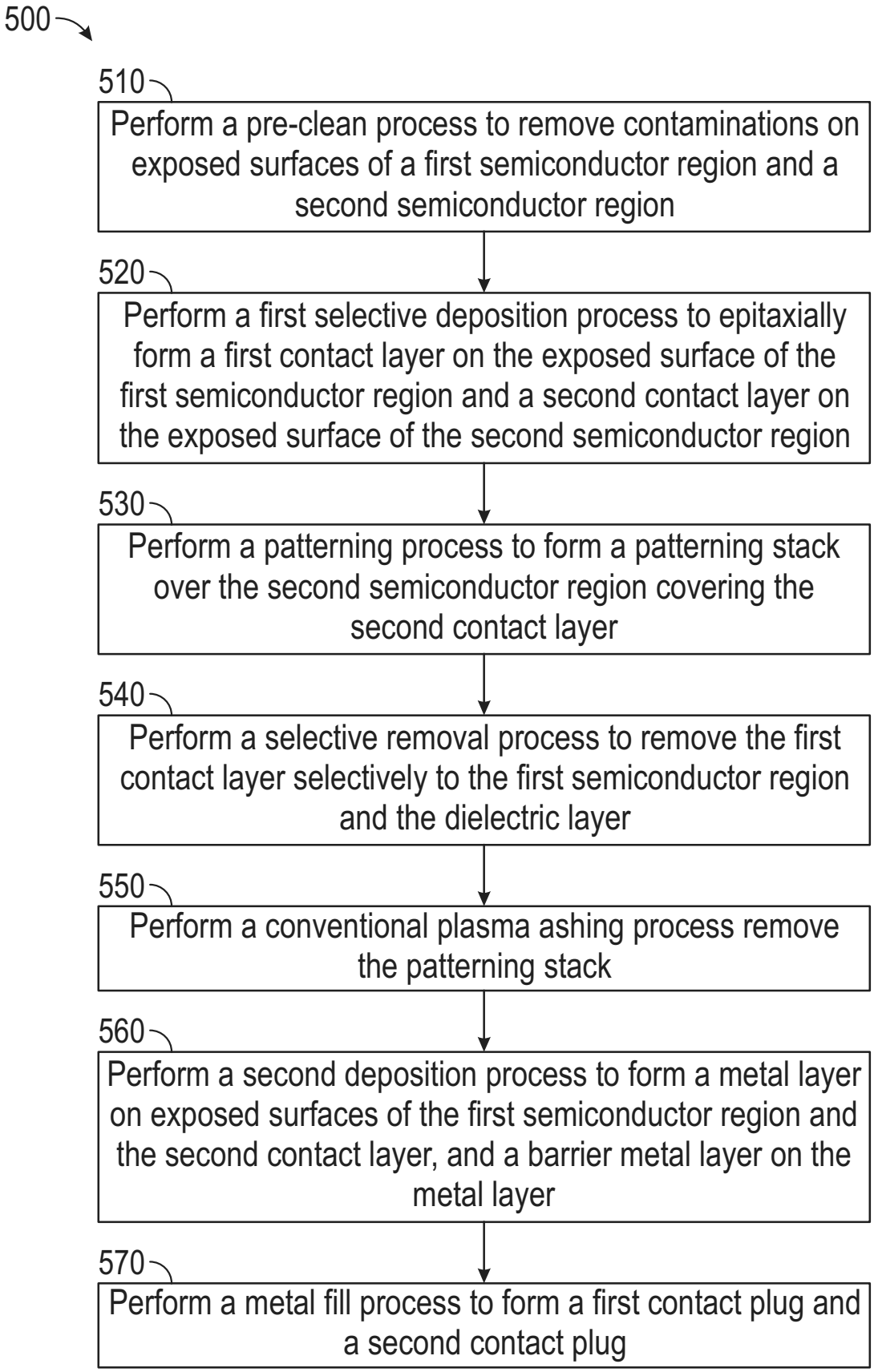

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Perform a pre-clean process to remove contaminations on exposed surfaces of a first semiconductor region and a second semiconductor region
520
Perform a first selective deposition process to epitaxially form a first contact layer on the exposed surface of the first semiconductor region and a second contact layer on the exposed surface of the second semiconductor region
530
Perform a patterning process to form a patterning stack over the second semiconductor region covering the second contact layer
540
Perform a selective removal process to remove the first contact layer selectively to the first semiconductor region and the dielectric layer
550
Perform a conventional plasma ashing process remove the patterning stack
560
Perform a second deposition process to form a metal layer on exposed surfaces of the first semiconductor region and the second contact layer, and a barrier metal layer on the metal layer
570
Perform a metal fill process to form a first contact plug and a second contact plug

FIG. 5

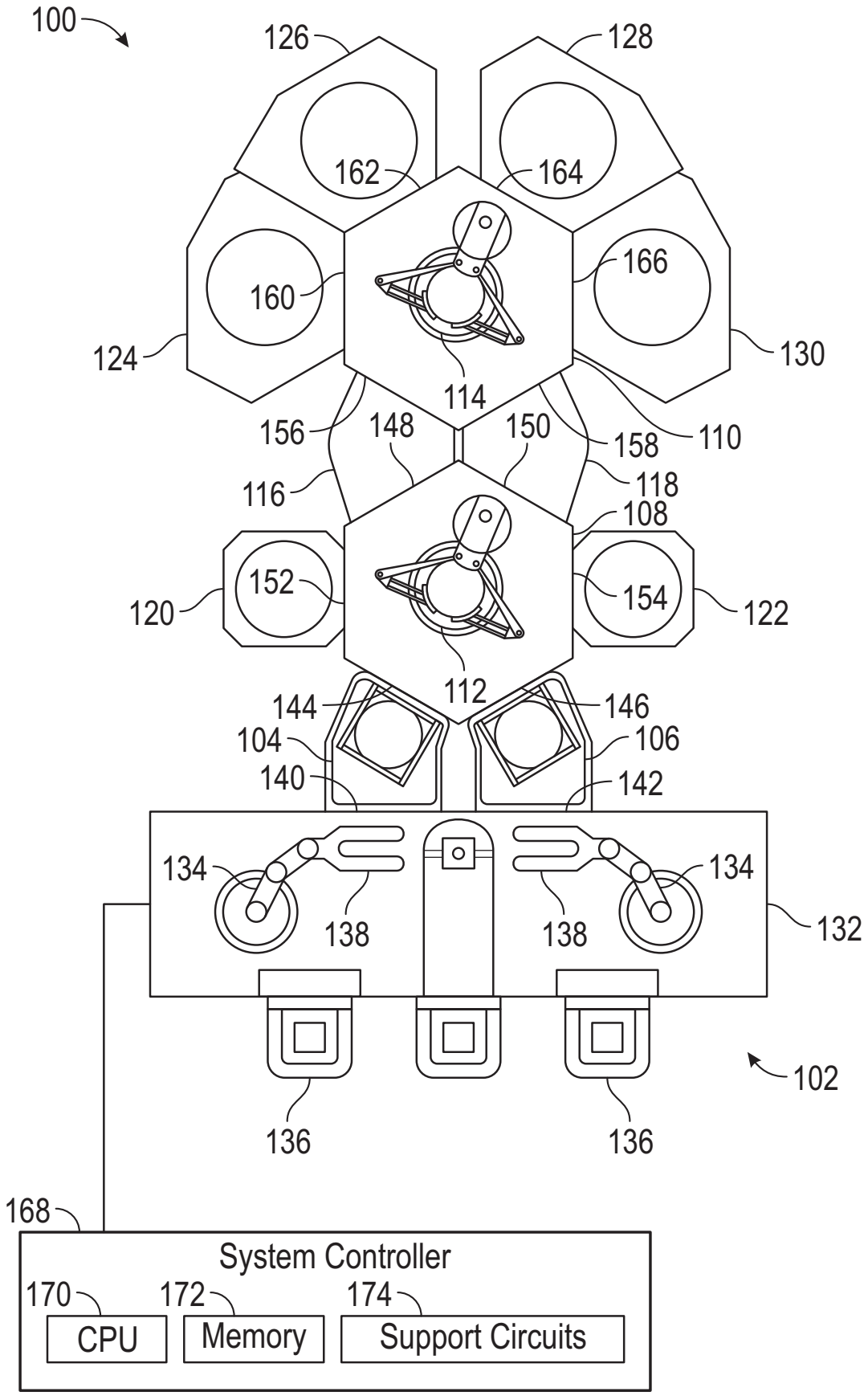

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Memory
Support Circuits

FIG. 1

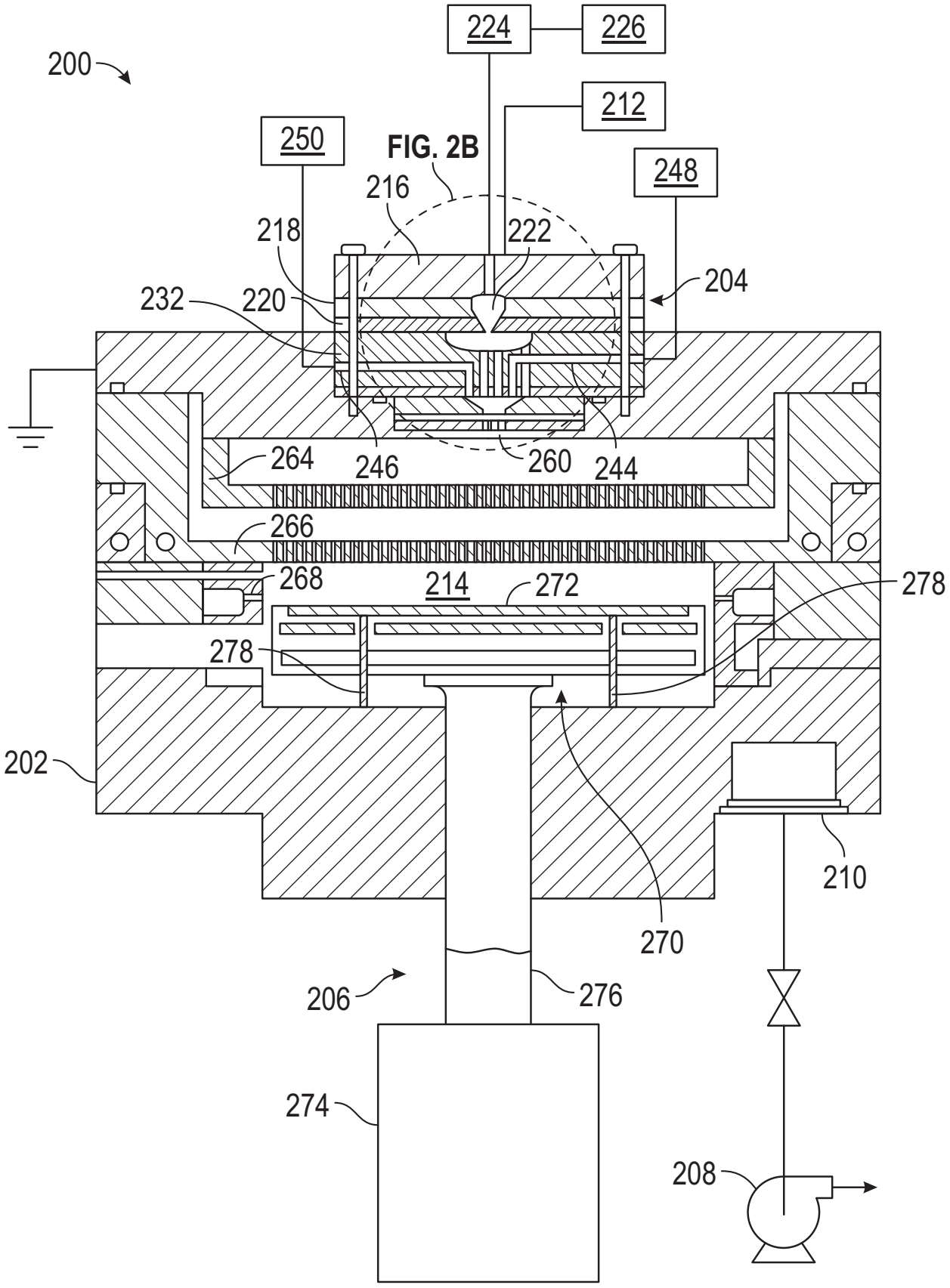

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FIG. 2B

FIG. 2A

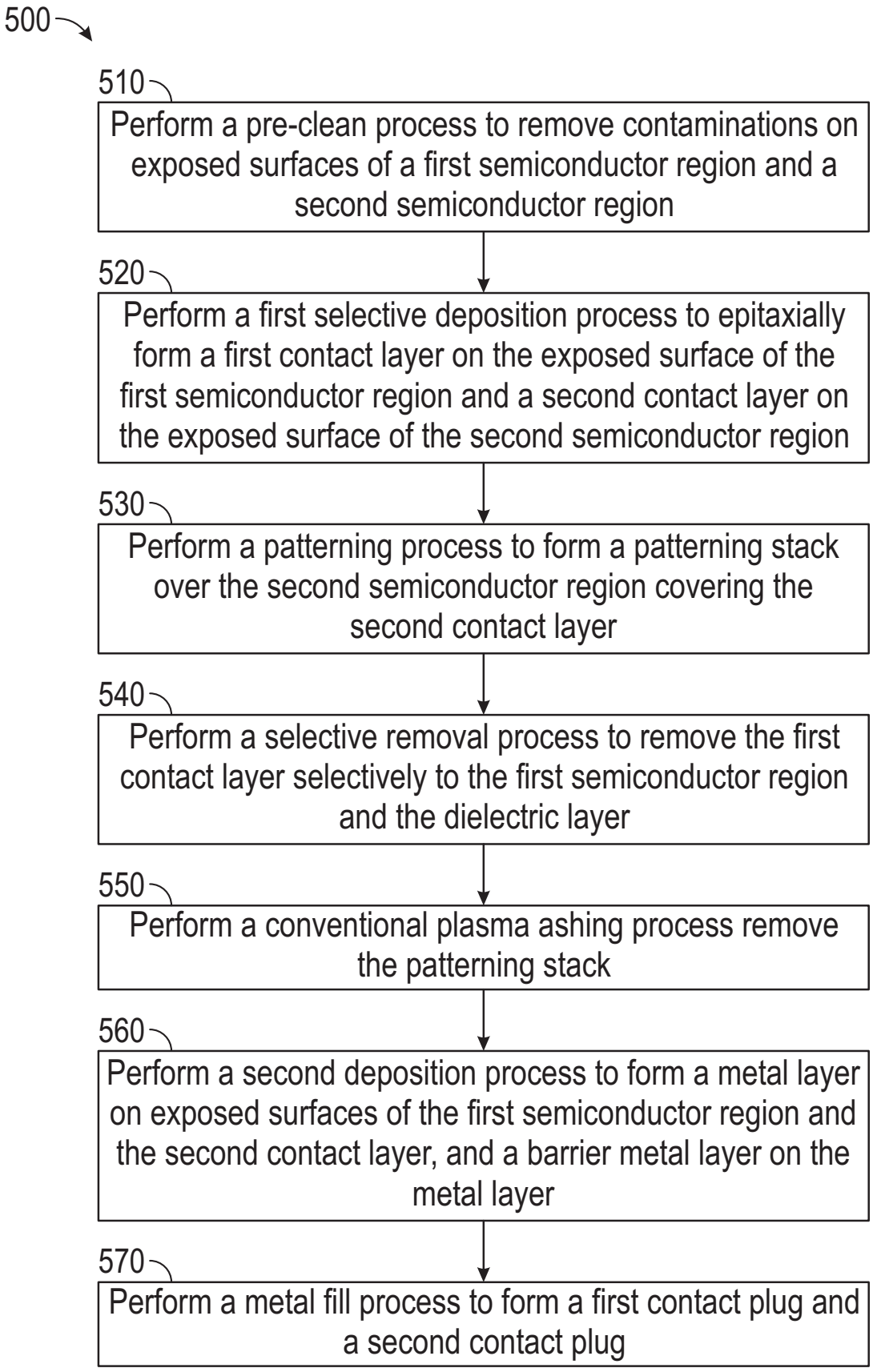

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510
Perform a pre-clean process to remove contaminations on exposed surfaces of a first semiconductor region and a second semiconductor region
520
Perform a first selective deposition process to epitaxially form a first contact layer on the exposed surface of the first semiconductor region and a second contact layer on the exposed surface of the second semiconductor region
530
Perform a patterning process to form a patterning stack over the second semiconductor region covering the second contact layer
540
Perform a selective removal process to remove the first contact layer selectively to the first semiconductor region and the dielectric layer
550
Perform a conventional plasma ashing process remove the patterning stack
560
Perform a second deposition process to form a metal layer on exposed surfaces of the first semiconductor region and the second contact layer, and a barrier metal layer on the metal layer
570
Perform a metal fill process to form a first contact plug and a second contact plug

FIG. 5