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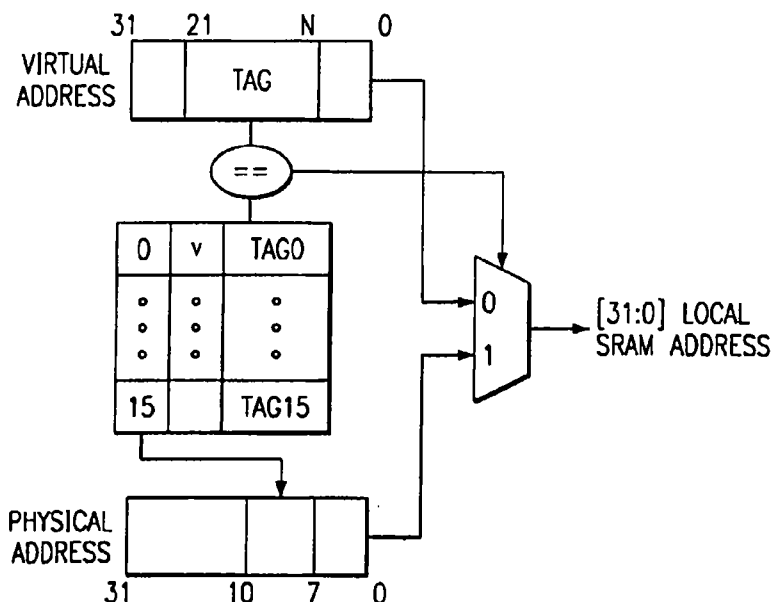
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(54) Title: SYSTEMS AND METHODS USING A SYSTEM-ON-A-CHIP WITH SOFT CACHE



(57) Abstract: A soft cache system compares tag bits of a virtual address (the bits from N-21) with tag fields of a plurality of soft cache register entries (TAG 0-TAG 15), each entry associated with an index (0-15) to a corresponding cache lines in virtual memory. A cache line size for the cache line is programmable. When the tag bits of the virtual address (the bits from N-21) match the tag field of one of the soft cache entries, the index (0-15) from that entry is selected for generating a physical address. The physical address is generated using the selected index as an offset field (the bits from 7-10) to a corresponding soft cache space in memory.

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