

DATA PATH CELL ON AN SeOI SUBSTRATE WITH A BURIED BACK
CONTROL GATE BENEATH THE INSULATING LAYER

ABSTRACT

The invention relates, according to a first aspect, to a data path cell specifically adapted to its environment for use in an integrated circuit produced on a semiconductor-on-insulator substrate comprising a thin layer of semiconductor material separated from a bulk substrate by an insulating layer, the cell comprising an array of field-effect transistors, each transistor having, in the thin layer, a source region (S_7), a drain region (D_7) and a channel region (C_7) which is bounded by the source and drain regions, and further including a front gate control region (GA_7) formed above the channel region, characterized in that at least one transistor (T_7) has a back gate control region (GN_2) formed in the bulk substrate beneath the channel region, the back gate region being able to be biased so as to modify the performance characteristics of the transistor.

FIGURE 3