FIG. 1A

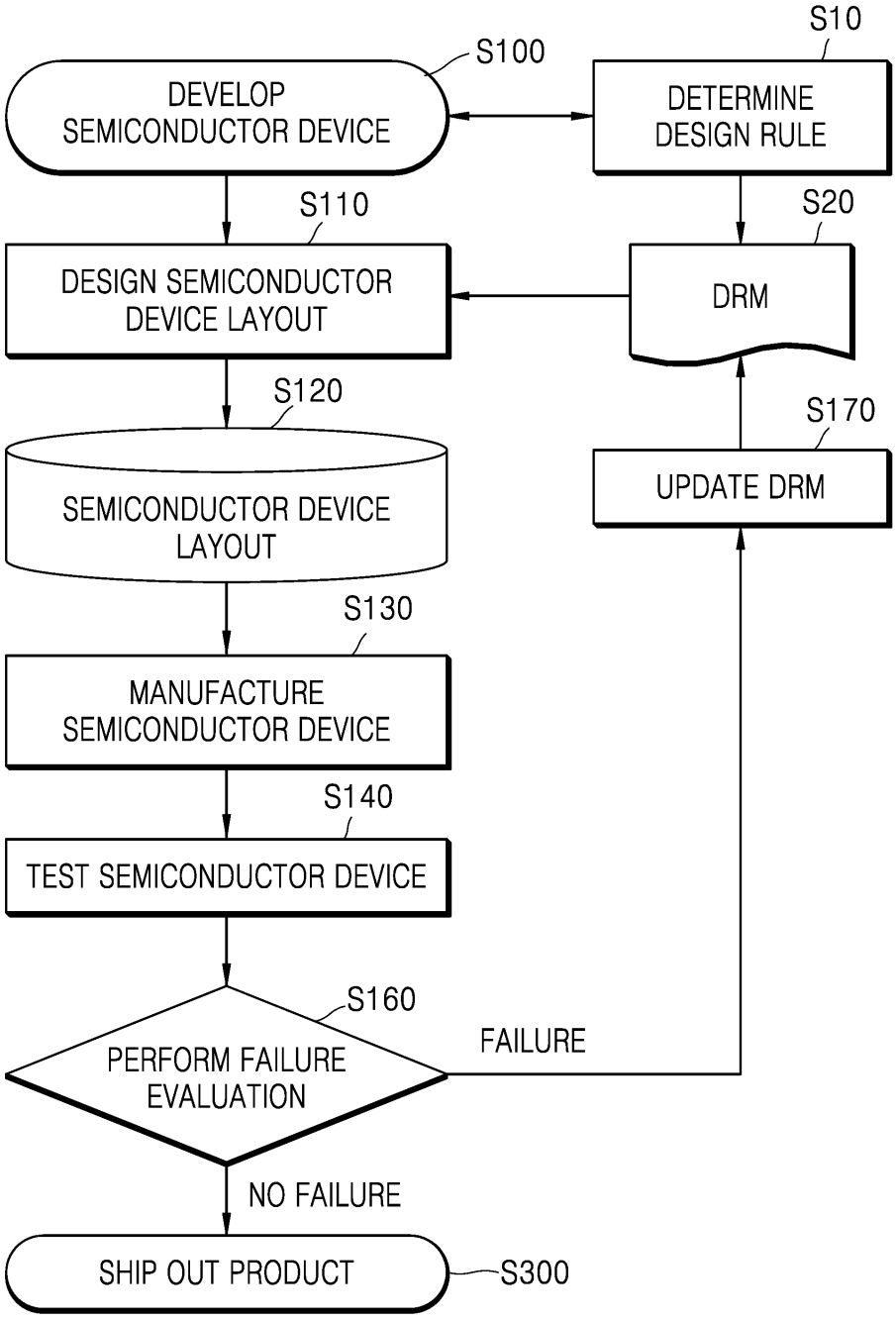

S10
S100
DEVELOP SEMICONDUCTOR DEVICE
DETERMINE DESIGN RULE
S110
S20
DESIGN SEMICONDUCTOR DEVICE LAYOUT
DRM
S120
S170
SEMICONDUCTOR DEVICE LAYOUT
UPDATE DRM
S130
MANUFACTURE SEMICONDUCTOR DEVICE
S140
TEST SEMICONDUCTOR DEVICE
S160
PERFORM FAILURE EVALUATION
FAILURE
NO FAILURE
SHIP OUT PRODUCT
S300

FIG. 1B

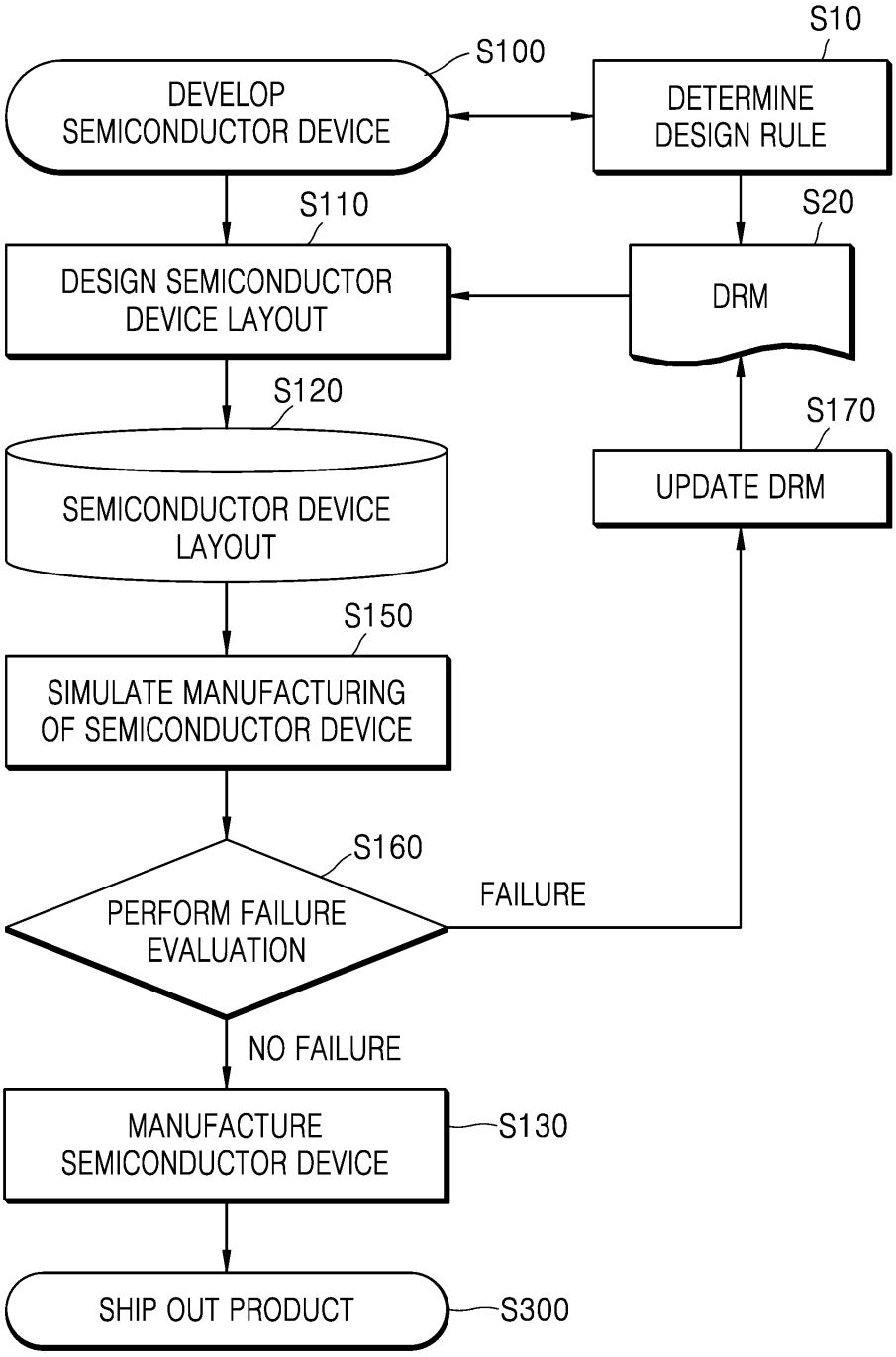

S10
S100
DEVELOP SEMICONDUCTOR DEVICE
DETERMINE DESIGN RULE
S110
S20
DESIGN SEMICONDUCTOR DEVICE LAYOUT
DRM
S120
S170
SEMICONDUCTOR DEVICE LAYOUT
UPDATE DRM
S150
SIMULATE MANUFACTURING OF SEMICONDUCTOR DEVICE
S160
PERFORM FAILURE EVALUATION
FAILURE
NO FAILURE
MANUFACTURE SEMICONDUCTOR DEVICE
S130
SHIP OUT PRODUCT
S300

FIG. 1C

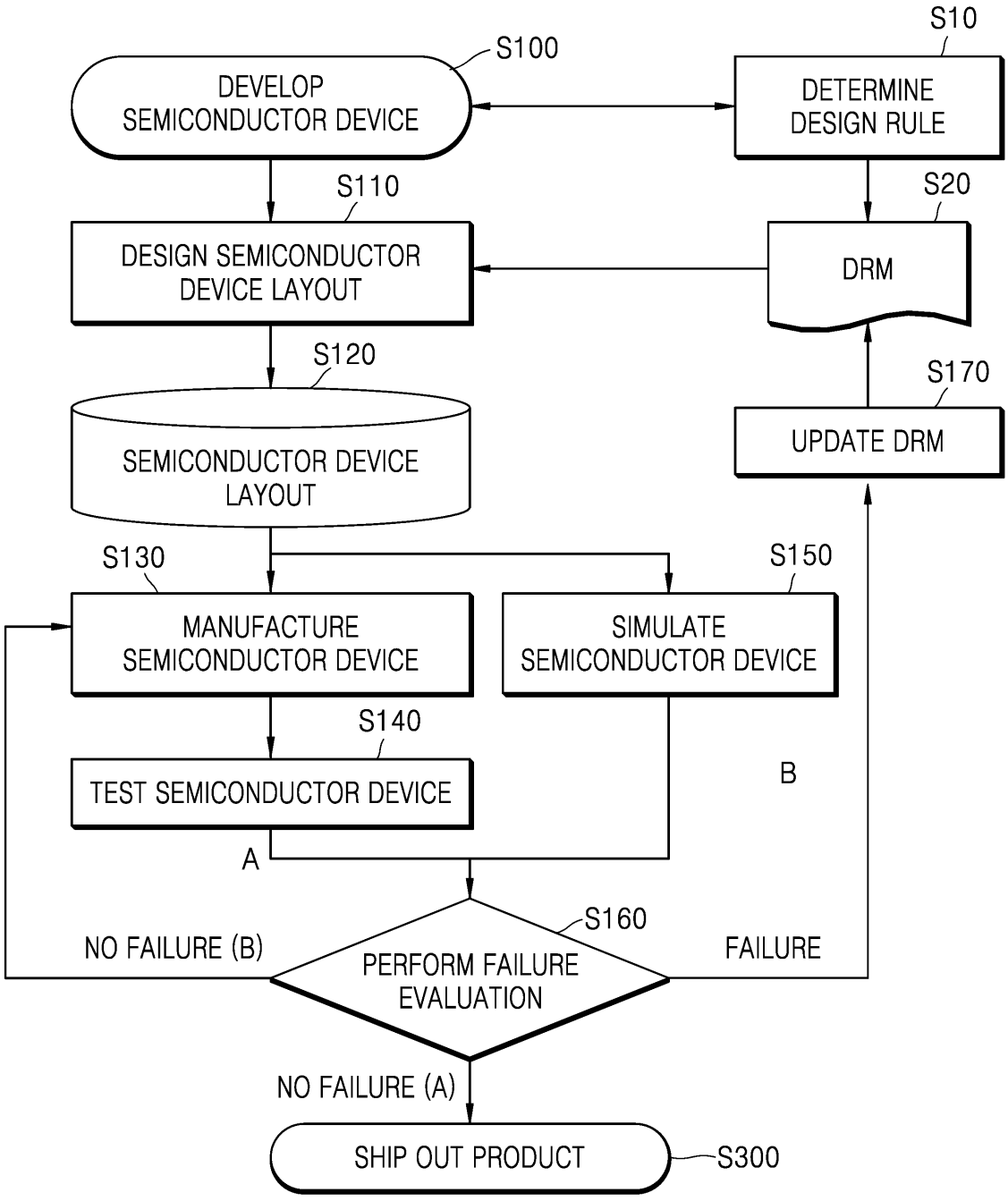

S10
S100
DEVELOP SEMICONDUCTOR DEVICE
DETERMINE DESIGN RULE
S110
S20
DESIGN SEMICONDUCTOR DEVICE LAYOUT
DRM
S120
S170
SEMICONDUCTOR DEVICE LAYOUT
UPDATE DRM
S130
S150
MANUFACTURE SEMICONDUCTOR DEVICE
SIMULATE SEMICONDUCTOR DEVICE
S140
TEST SEMICONDUCTOR DEVICE
B
A
S160
NO FAILURE (B)
PERFORM FAILURE EVALUATION
FAILURE
NO FAILURE (A)
SHIP OUT PRODUCT
S300

FIG. 1D

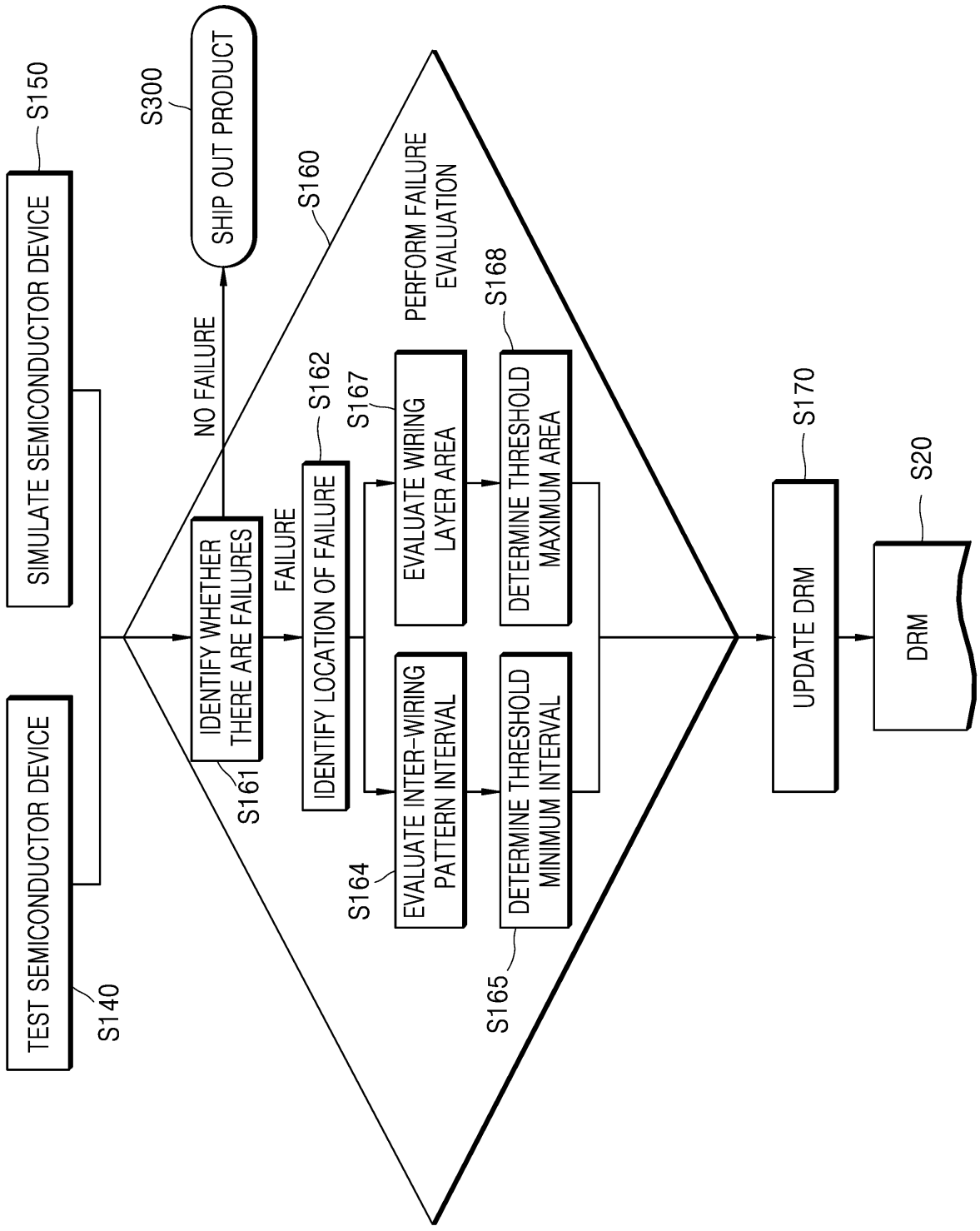

TEST SEMICONDUCTOR DEVICE
SIMULATE SEMICONDUCTOR DEVICE
S140
S150
IDENTIFY WHETHER THERE ARE FAILURES
S161
NO FAILURE
SHIP OUT PRODUCT
S300
FAILURE
IDENTIFY LOCATION OF FAILURE
S162
PERFORM FAILURE EVALUATION
S160
EVALUATE INTER-WIRING PATTERN INTERVAL
S164
EVALUATE WIRING LAYER AREA
S167
DETERMINE THRESHOLD MINIMUM INTERVAL
S165
DETERMINE THRESHOLD MAXIMUM AREA
S168
UPDATE DRM
S170
DRM
S20

FIG. 2

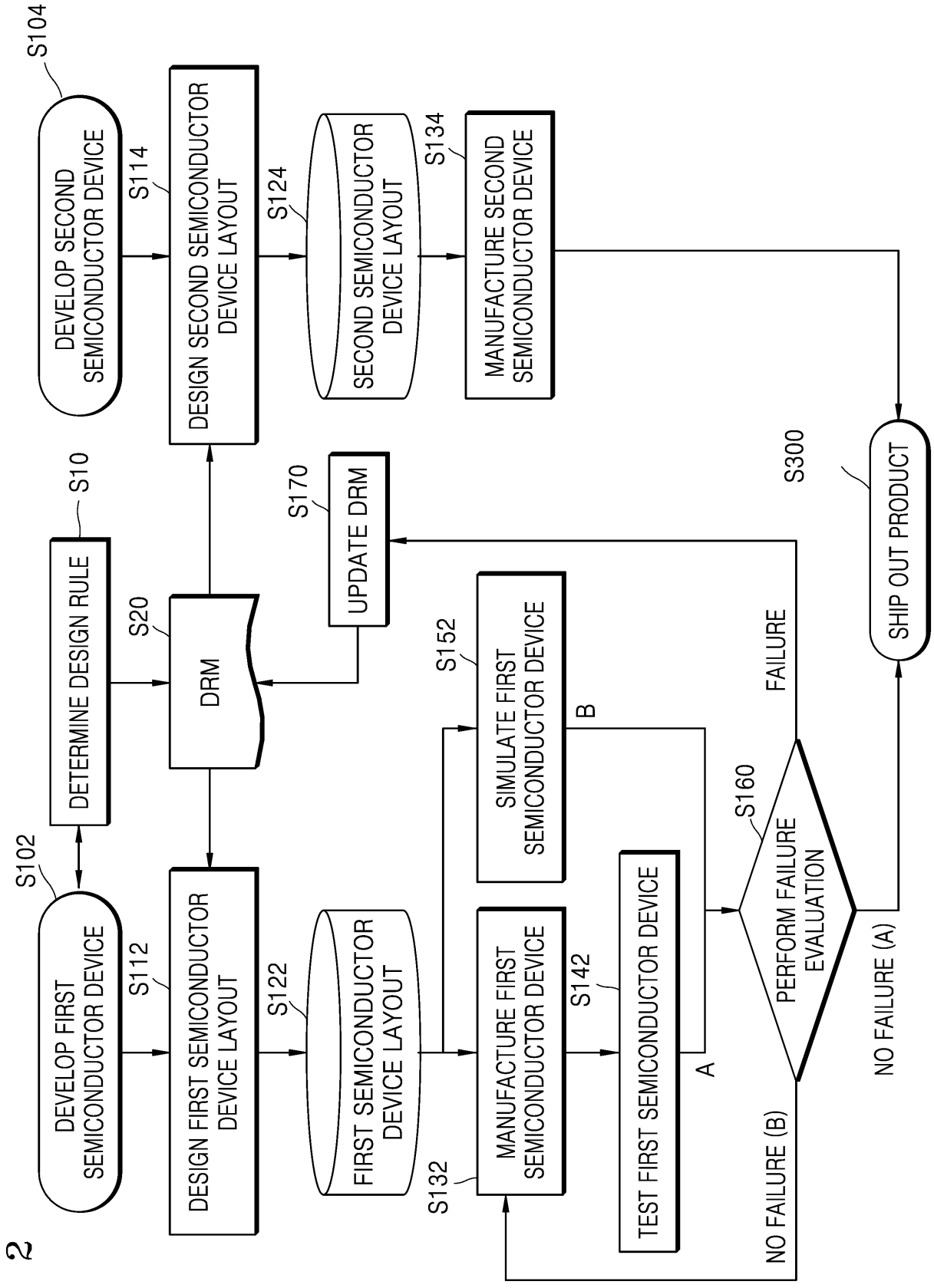

S104
DEVELOP SECOND SEMICONDUCTOR DEVICE
S114
DESIGN SECOND SEMICONDUCTOR DEVICE LAYOUT
S124
SECOND SEMICONDUCTOR DEVICE LAYOUT
S134
MANUFACTURE SECOND SEMICONDUCTOR DEVICE
S10
DETERMINE DESIGN RULE
S20
DRM
S170
UPDATE DRM
S300
SHIP OUT PRODUCT
S102
DEVELOP FIRST SEMICONDUCTOR DEVICE
S112
DESIGN FIRST SEMICONDUCTOR DEVICE LAYOUT
S122
FIRST SEMICONDUCTOR DEVICE LAYOUT
S152
SIMULATE FIRST SEMICONDUCTOR DEVICE
B
S132
MANUFACTURE FIRST SEMICONDUCTOR DEVICE
S142
TEST FIRST SEMICONDUCTOR DEVICE
A
S160
PERFORM FAILURE EVALUATION
FAILURE
NO FAILURE (A)
NO FAILURE (B)

FIG. 3

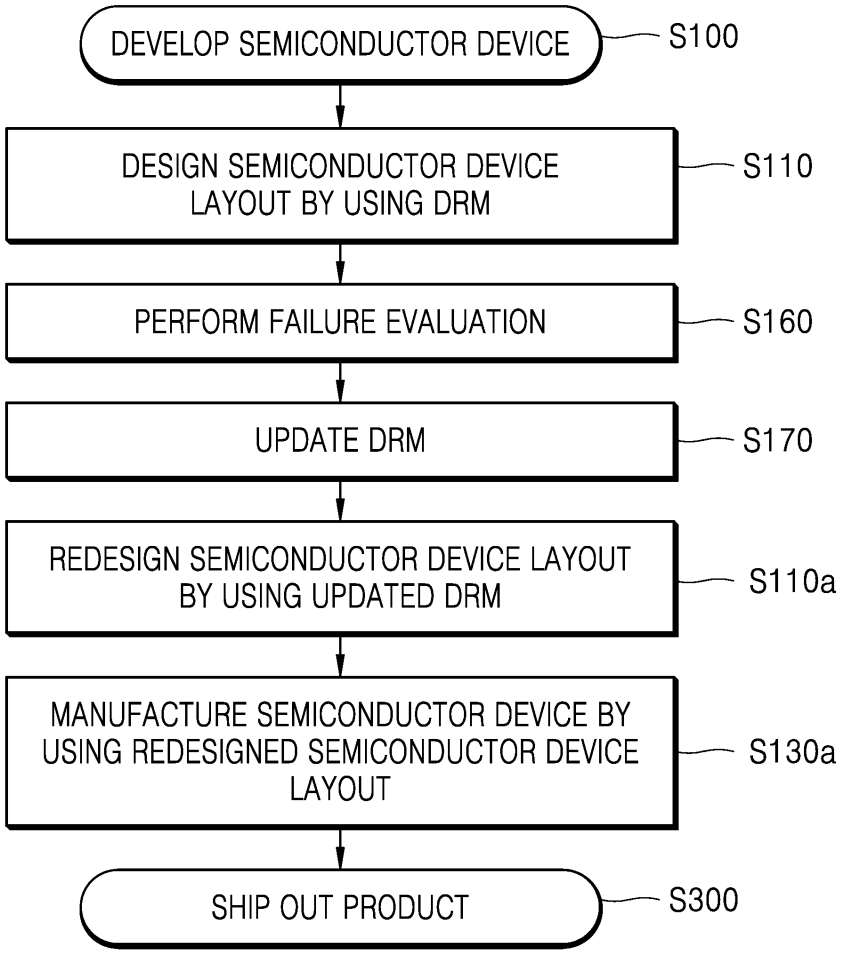

DEVELOP SEMICONDUCTOR DEVICE
S100
DESIGN SEMICONDUCTOR DEVICE LAYOUT BY USING DRM
S110
PERFORM FAILURE EVALUATION
S160
UPDATE DRM
S170
REDESIGN SEMICONDUCTOR DEVICE LAYOUT BY USING UPDATED DRM
S110a
MANUFACTURE SEMICONDUCTOR DEVICE BY USING REDESIGNED SEMICONDUCTOR DEVICE LAYOUT
S130a
SHIP OUT PRODUCT
S300

FIG. 4A

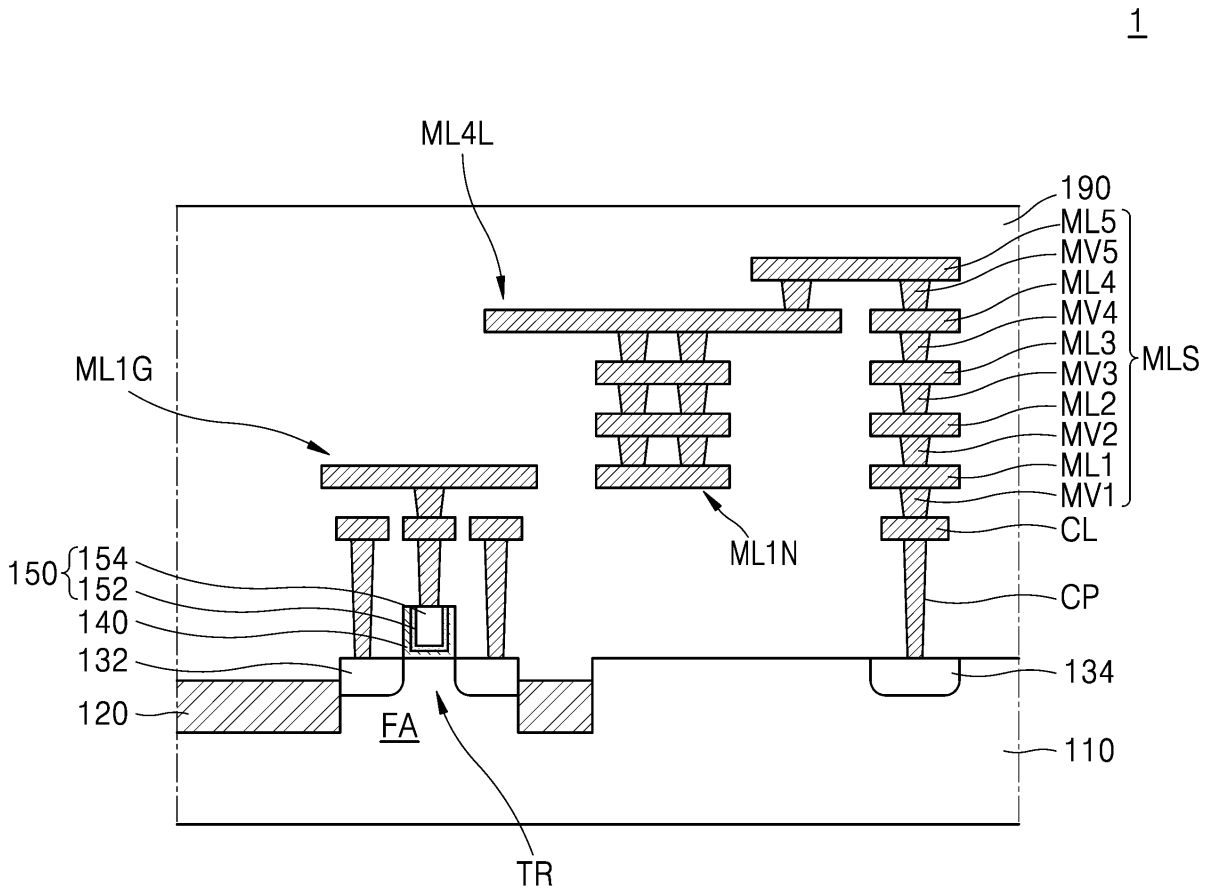

1
ML4L
190
ML5
MV5
ML4
MV4
ML3
MV3
ML2
MV2
ML1
MV1
MLS
ML1G
ML1N
CL
150
154
152
140
132
120
CP
134
FA
110
TR

FIG. 4B

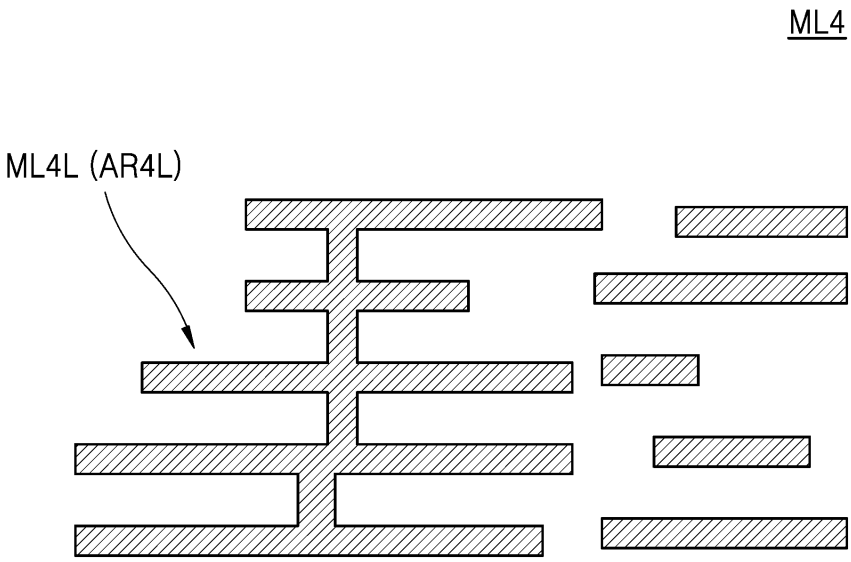


FIG. 5A

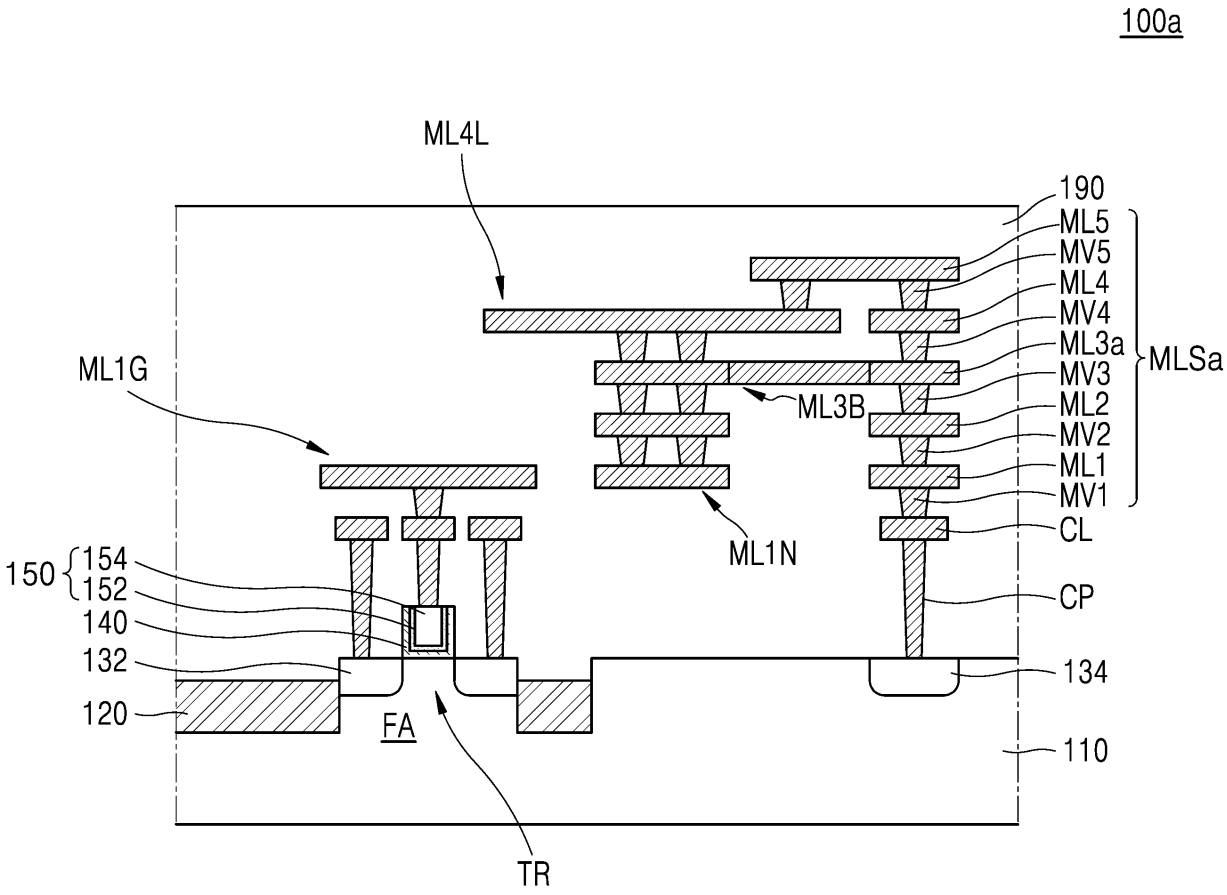

100a
ML4L
190
ML5
MV5
ML4
MV4
ML3a
MV3
ML2
MV2
ML1
MV1
MLSa
ML1G
ML3B
ML1N
CL
150
154
152
140
132
120
CP
134
FA
110
TR

FIG. 5B

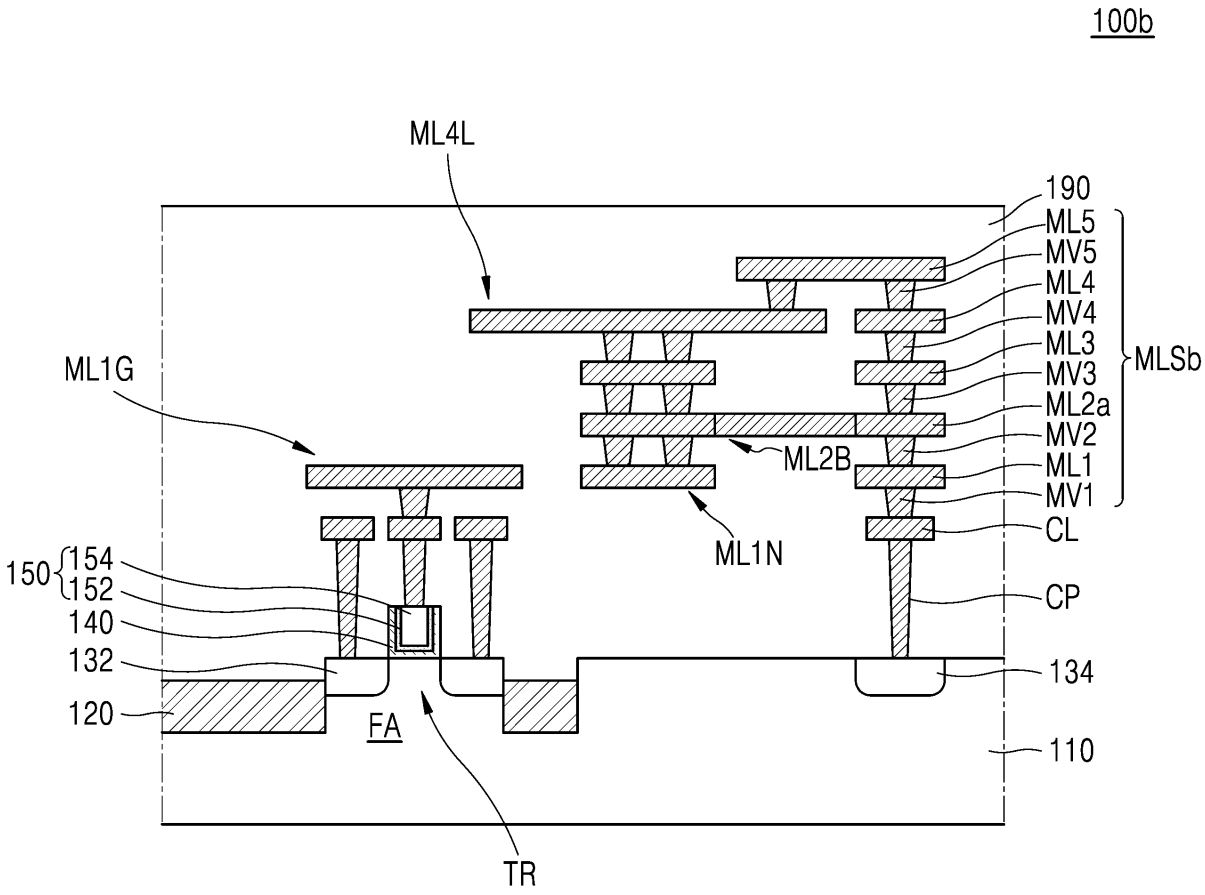

100b
ML4L
190
ML5
MV5
ML4
MV4
ML3
MV3
ML2a
MV2
ML1
MV1
MLSb
ML1G
ML2B
ML1N
CL
150
154
152
140
132
120
CP
134
FA
110
TR

FIG. 5C

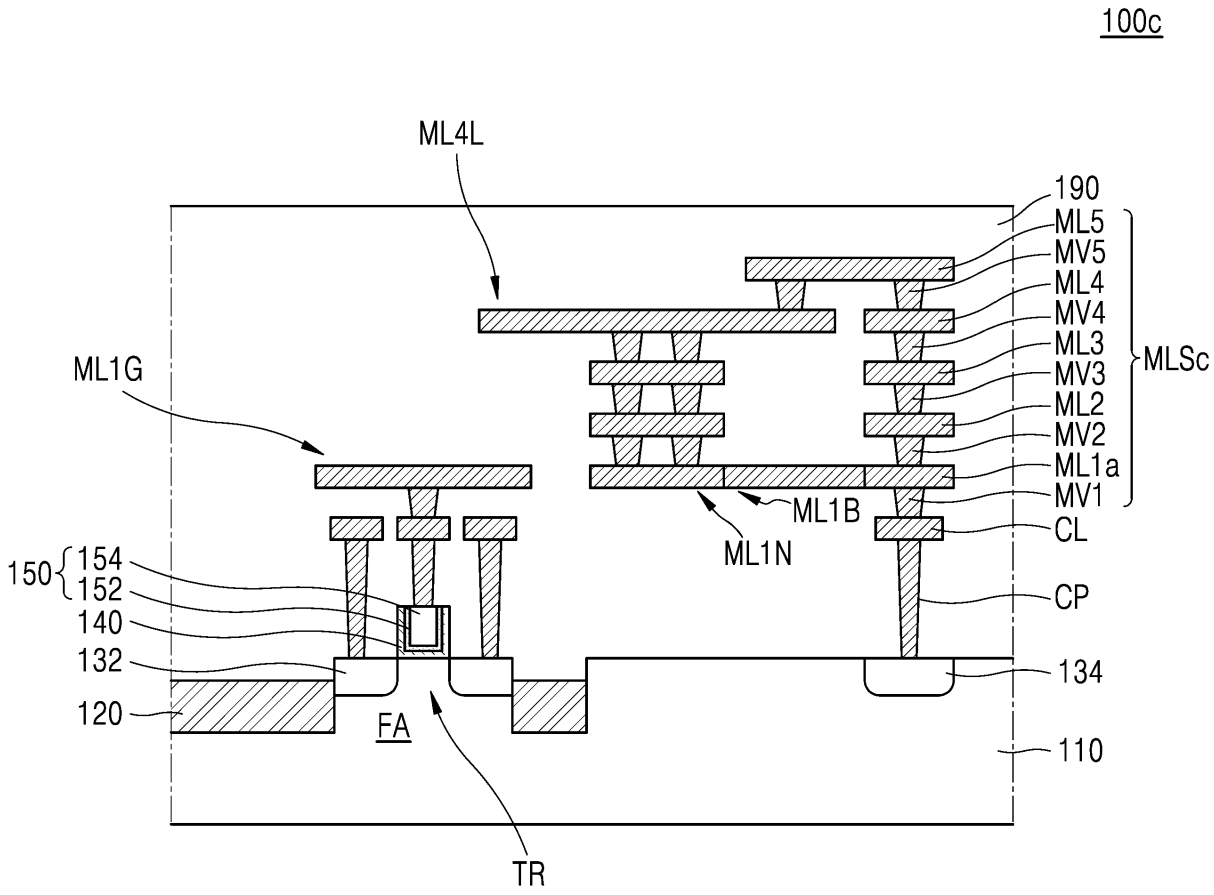

100c
ML4L
190
ML5
MV5
ML4
MV4
ML3
MV3
ML2
MV2
ML1a
MV1
MLSc
ML1G
ML1B
ML1N
CL
150
154
152
140
132
120
CP
134
FA
110
TR

FIG. 5D

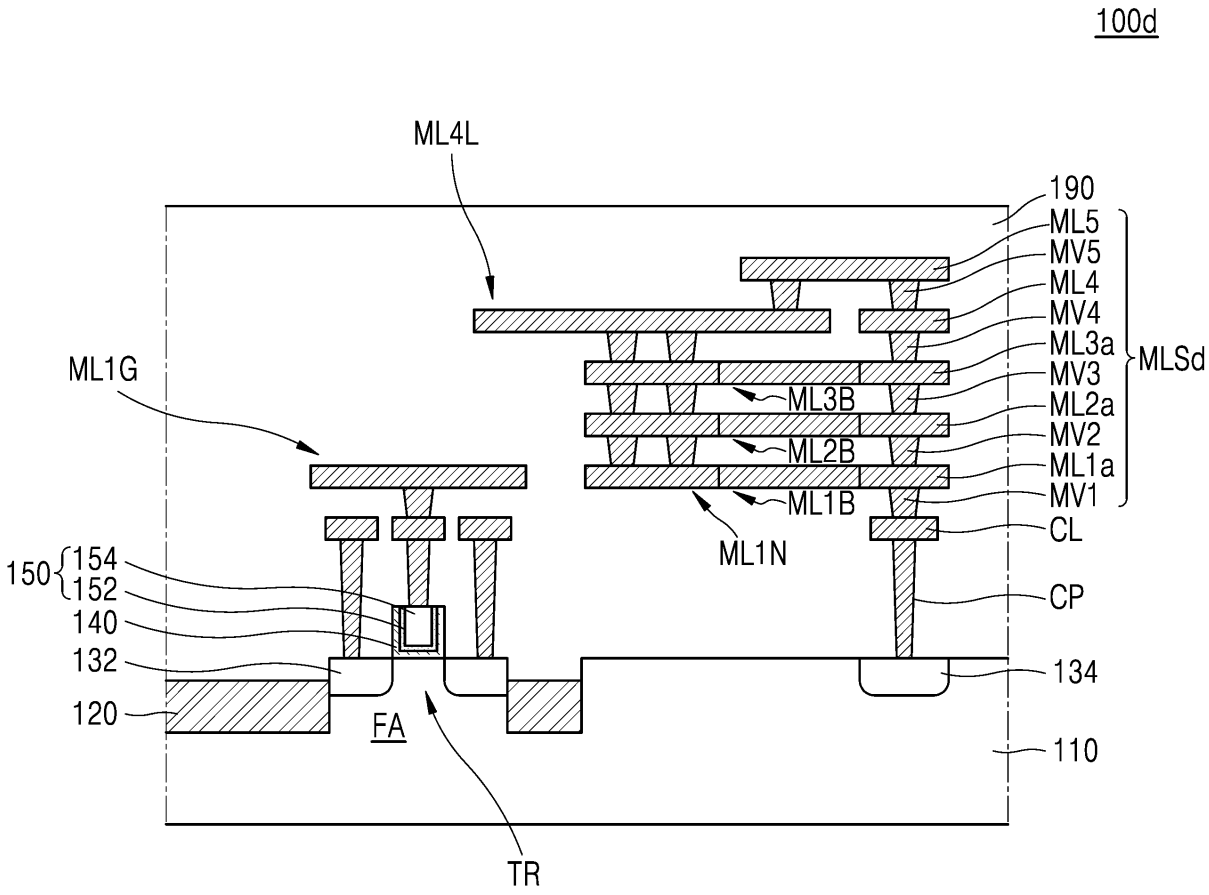

100d
ML4L
190
ML5
MV5
ML4
MV4
ML3a
MV3
ML2a
MV2
ML1a
MV1
MLSd
ML1G
ML3B
ML2B
ML1B
ML1N
CL
150
154
152
140
132
120
CP
134
FA
110
TR

FIG. 6

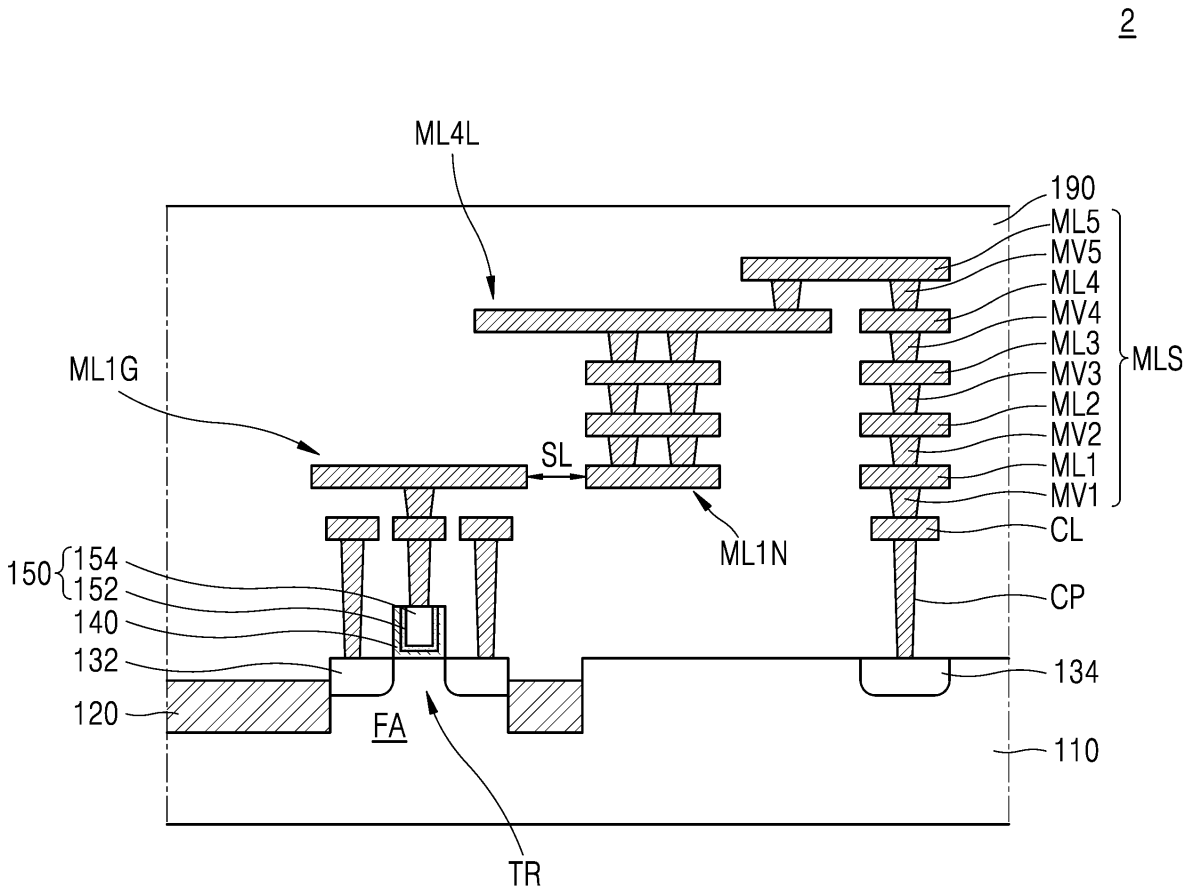

2
ML4L
190
ML5
MV5
ML4
MV4
ML3
MV3
ML2
MV2
ML1
MV1
MLS
ML1G
SL
ML1N
CL
150
154
152
140
132
120
CP
134
FA
110
TR

FIG. 7

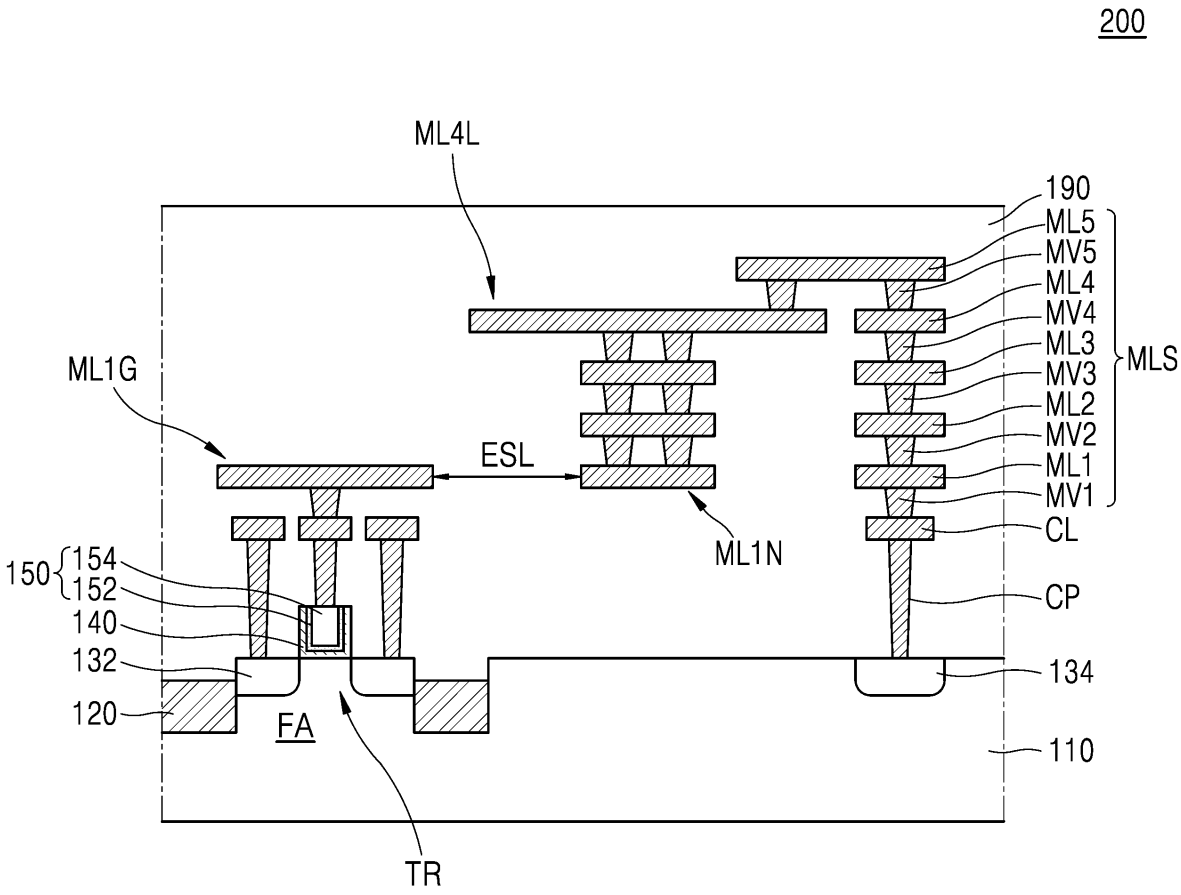

200
ML4L
190
ML5
MV5
ML4
MV4
ML3
MV3
ML2
MV2
ML1
MV1
MLS
ML1G
ESL
ML1N
CL
150
154
152
140
132
120
CP
134
FA
110
TR

FIG. 8

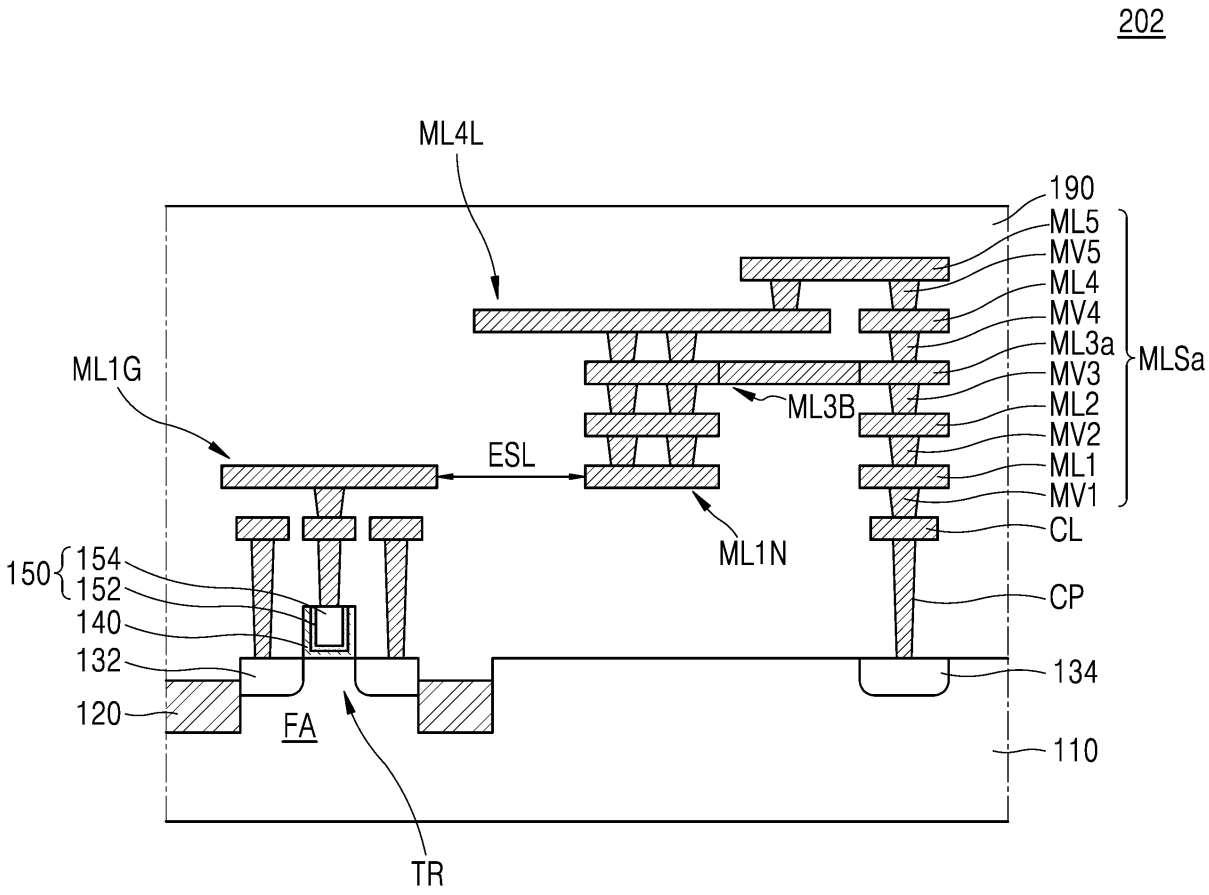

202
ML4L
190
ML5
MV5
ML4
MV4
ML3a
MV3
ML2
MV2
ML1
MV1
MLSa
ML1G
ML3B
ESL
ML1N
CL
150
154
152
CP
140
132
134
120
FA
110
TR

FIG. 9A

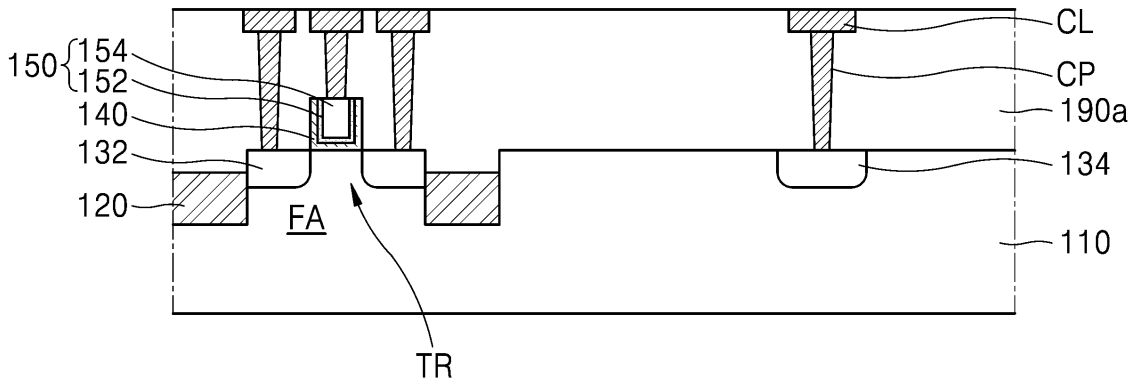


FIG. 9B

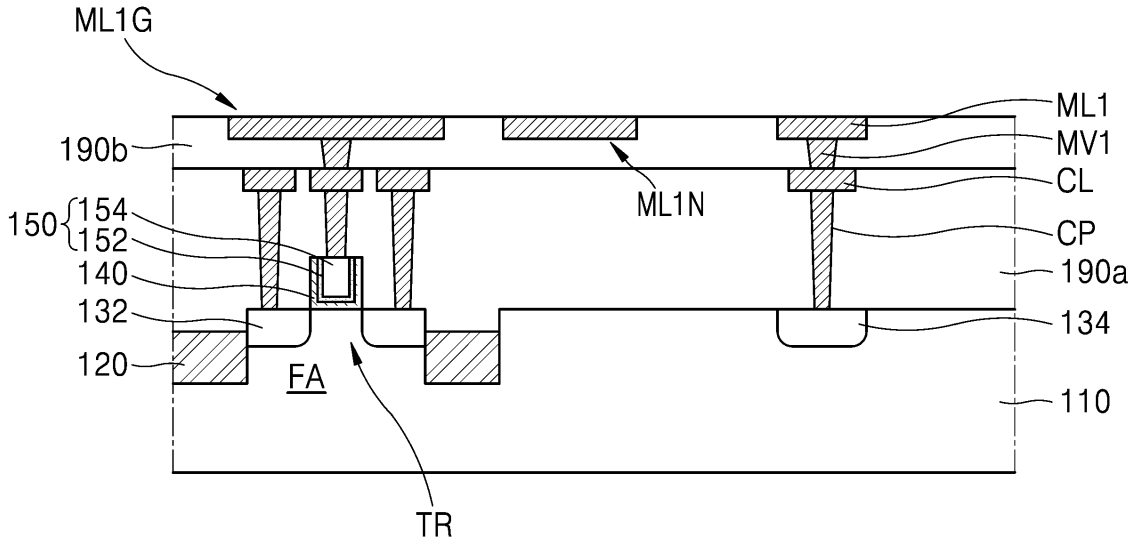

ML1G
ML1
MV1
190b
ML1N
CL
150
154
152
CP
140
190a
132
134
120
FA
110
TR

FIG. 9C

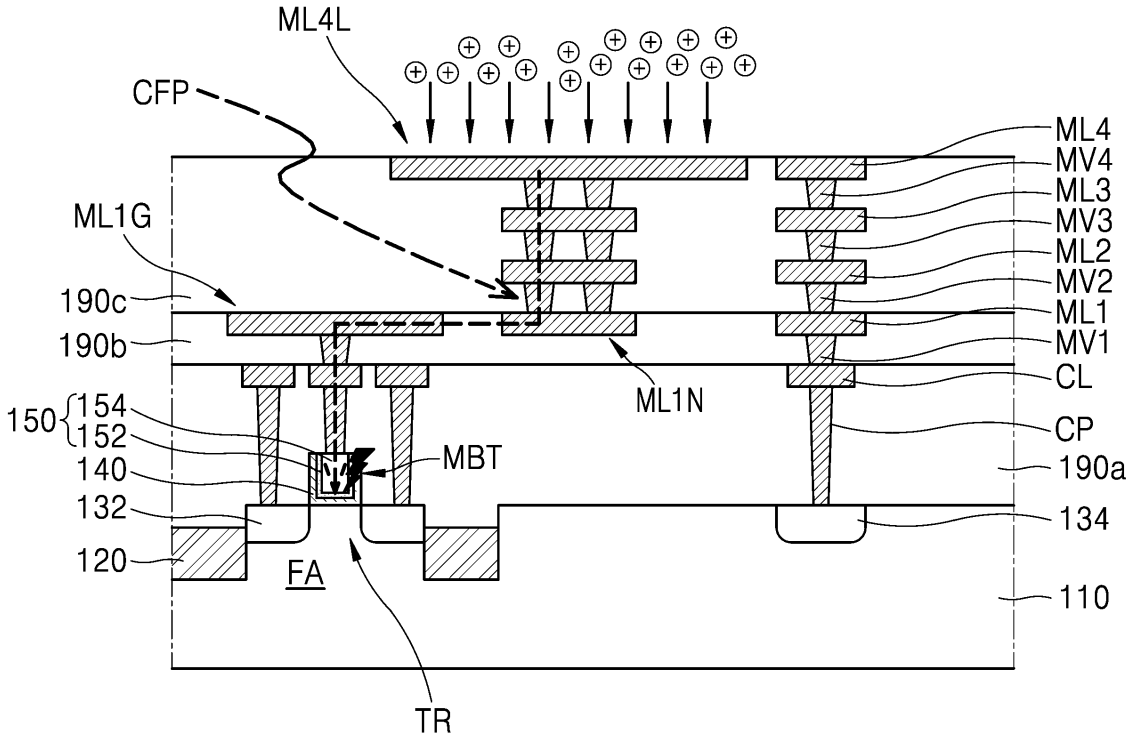

ML4L
CFP
ML1G
190c
190b
150
154
152
140
132
120
MBT
FA
TR
ML1N
ML4
MV4
ML3
MV3
ML2
MV2
ML1
MV1
CL
CP
190a
134
110

FIG. 10

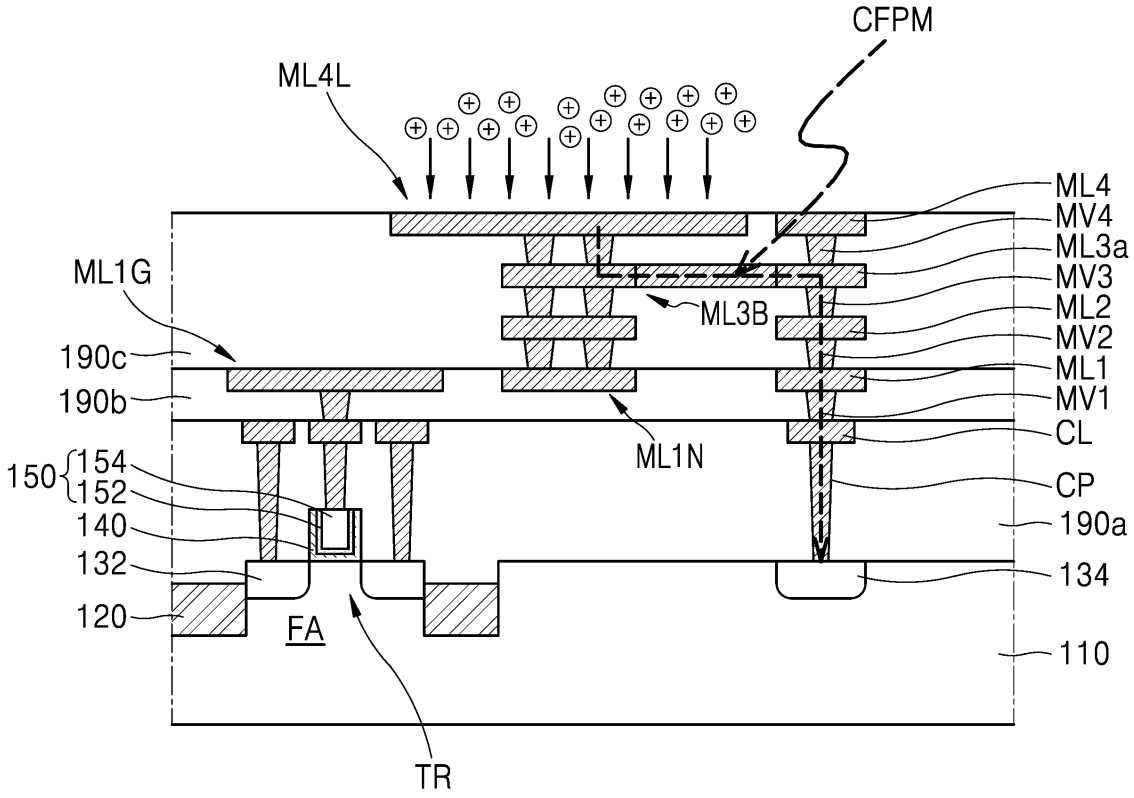

CFPM
ML4L
ML4
MV4
ML3a
MV3
ML2
MV2
ML1
MV1
CL
CP
190a
134
110
ML1G
ML3B
190c
190b
ML1N
150
154
152
140
132
120
FA
TR

FIG. 11

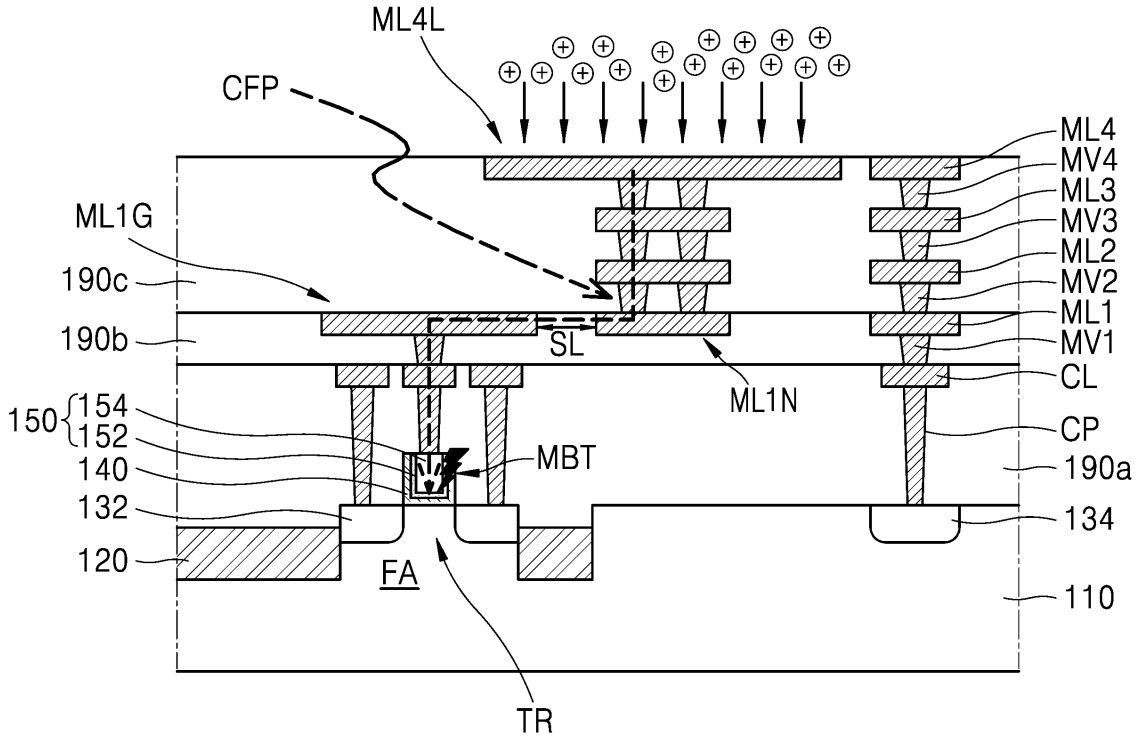
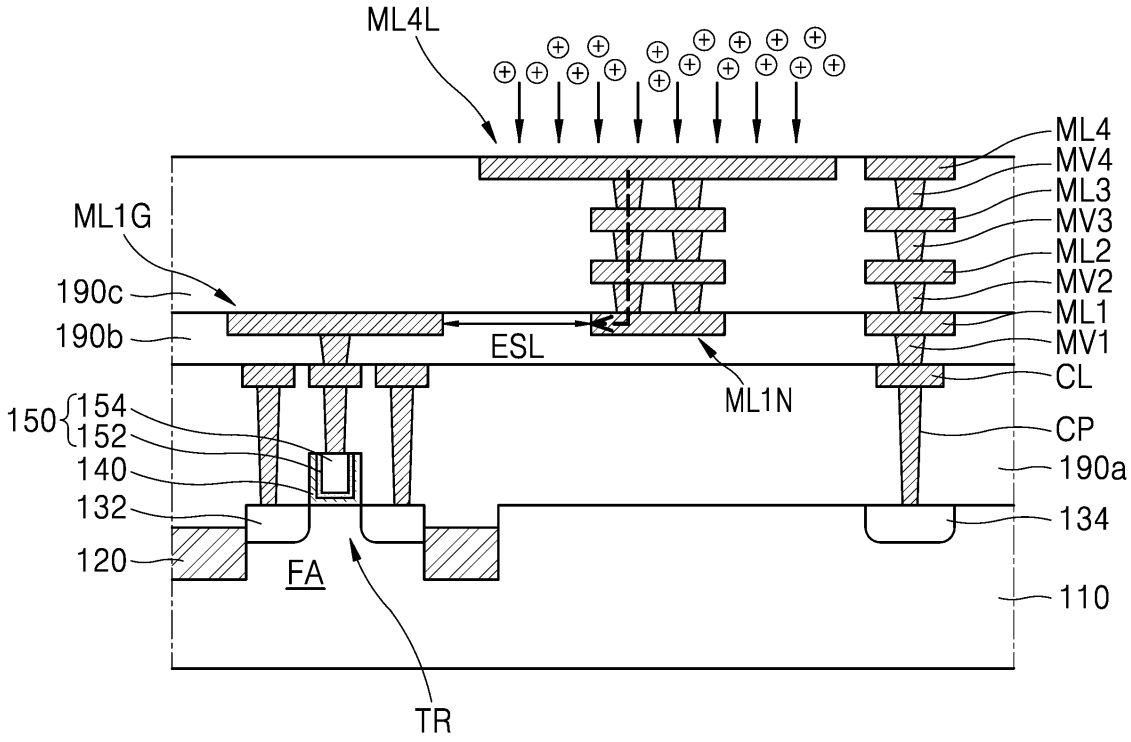

ML4L
CFP
ML4
MV4
ML3
MV3
ML2
MV2
ML1
MV1
CL
CP
190a
134
110
ML1G
190c
190b
SL
ML1N
150
154
152
140
132
120
MBT
FA
TR

FIG. 12


ML4L
ML4
MV4
ML3
MV3
ML2
MV2
ML1
MV1
CL
CP
190a
134
110
ML1G
190c
190b
ESL
ML1N
150
154
152
140
132
120
FA
TR