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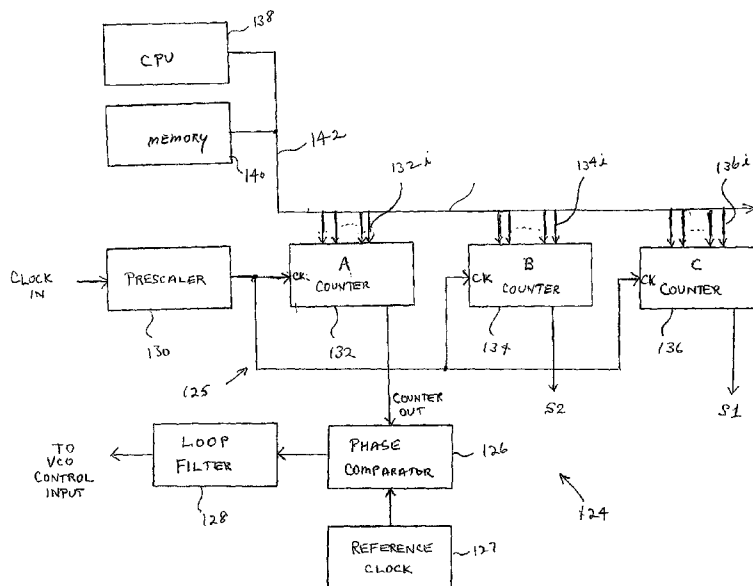
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(54) Title: **WIRELESS COMMUNICATION DEVICE WITH PHASE-LOCKED LOOP OSCILLATOR**



(57) Abstract: A frequency generating circuit utilizes a quad modulus prescaler in which two control signals are used to select the prescaler modulus. The modulus control signals are generated by a multistage counter in which two independent counting stages (B, C) are used to generate the first and second modulus control signals (S1, S2). The first modulus control signal is at a first logic level when the associated counter is at a non-zero value and is at a second logic level when the associated counter reaches zero. The second modulus control signal is generated by a second counter and has a first logic value when the second counter is in a non-zero state and a second logic value when the second counter reaches zero.

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