

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 February 2001 (08.02.2001)

PCT

(10) International Publication Number
WO 01/09939 A1

- (51) International Patent Classification⁷: H01L 21/44, 21/48, 21/50, 23/12, 23/053
- (21) International Application Number: PCT/US00/20583
- (22) International Filing Date: 28 July 2000 (28.07.2000)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
09/365,356 30 July 1999 (30.07.1999) US
- (71) Applicant: MICRON TECHNOLOGY, INC. [US/US];
8000 South Federal Way, Boise, ID 83707 (US).
- (72) Inventor: JIANG, Tongbi; 12036 W. Patrina Drive, Boise,
ID 83713 (US).
- (74) Agents: ARTERBERRY, Steve et al.; Dorsey & Whitney
LLP, Suite 3400, 1420 Fifth Avenue, Seattle, WA 98101
(US).
- (81) Designated States (*national*): AE, AL, AM, AT, AU, AZ,
BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK,
DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL,
IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU,
LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT,
RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA,
UG, UZ, VN, YU, ZA, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian
patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European
patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,
IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG,
CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).
- Published:
— With international search report.
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND STRUCTURE FOR MANUFACTURING IMPROVED YIELD SEMICONDUCTOR PACKAGED DEVICES

(57) Abstract: A semiconductor package structure for a ball grid array type package using a plurality of pieces of adhesive elastomer film to attach a semiconductor die to a substrate having conductive traces in order to alleviate thermal mismatch stress between the semiconductor die and the printed circuit board to which the packaged device is soldered, while maintaining the reliability of the packaged device itself.

WO 01/09939 A1