H1529 PC

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 January 2005 (27.01.2005)

PCT

(10) International Publication Number
WO 2005/008758 A1

(51) International Patent Classification[7]: H01L 21/285

(21) International Application Number: PCT/US2004/021661

(22) International Filing Date: 6 July 2004 (06.07.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/615,086 7 July 2003 (07.07.2003) US

(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC.** [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **CHIU, Robert, J.** [US/US]; 1901 Halford Avenue, #6, Santa Clara, CA 95051 (US). **PATTON, Jeffrey, P.** [US/US]; 2250 Monroe St, #366, Santa Clara, CA 95050 (US). **BESSER, Paul, R.** [US/US]; 1087 Yorktown Drive, Sunnyvale, CA 94087 (US). **NGO, Minh, Van** [US/US]; 40986 Canyon Heights Drive, Fremont, CA 94539 (US).

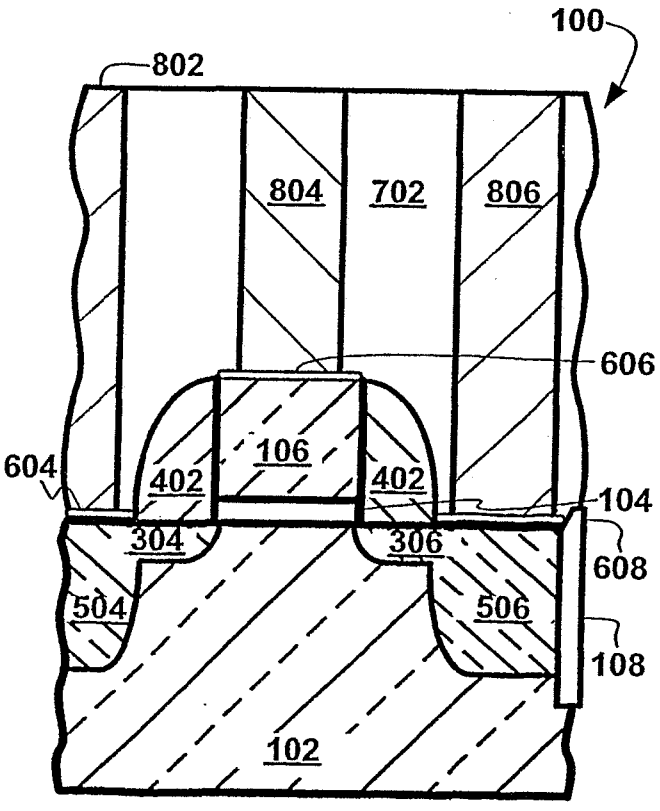
(74) Agent: **COLLOPY, Daniel, R.**; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: ULTRA-UNIFORM SILICIDES IN INTEGRATED CIRCUIT TECHNOLOGY



(57) Abstract: A method (900) of forming and a structure of an integrated circuit (100) are provided. A gate dielectric (104) is formed on a semiconductor substrate (102), and a gate (106) is formed over a gate dielectric (104) on the semiconductor substrate (102). Source/drain junctions (504/506) are formed in the semiconductor substrate (102). Ultra-uniform silicides (604/608) are formed on the source/drain junctions (504/506), and a dielectric layer (702) is deposited above the semiconductor substrate (102). Contacts (802/806/804) are then formed in the dielectric layer (702) to the ultra-uniform silicides (604/608/606).

WO 2005/008758 A1

European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.