

CAPACITOR AND DRAM DEVICE INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application claims the benefit of and priority to Korean Patent Application No. 10-2020-0121326, filed on 21 September 2020 in the Korean Intellectual Property Office, and entitled: “Capacitor and a Dram Device Including the Same,” is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] Embodiments relate to a capacitor and a dynamic random-access memory (DRAM) device including the same.

BACKGROUND

[0003] In a DRAM device, unit memory cell may include one transistor and one capacitor, and the capacitor may have a high capacitance.

SUMMARY

[0004] The embodiments may be realized by providing a capacitor including a lower electrode; a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and an upper electrode on the dielectric layer structure, wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase.

[0005] The embodiments may be realized by providing a capacitor including a lower electrode; a dielectric layer structure on the lower electrode, the dielectric layer structure

including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and an upper electrode on the dielectric layer structure, wherein the dielectric layer structure has a thickness of about 20 Å to about 60 Å, and the first zirconium oxide layer, the hafnium oxide layer, and the second zirconium oxide layer are each crystalline.

[0006] The embodiments may be realized by providing a dynamic random-access memory (DRAM) device including a substrate; a cell transistor on the substrate, the cell transistor including a gate structure, a first impurity region, and a second impurity region; a bit line structure electrically connected to the first impurity region; and a capacitor on the bit line structure, the capacitor being electrically connected to the second impurity region, wherein the capacitor includes a lower electrode; a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and an upper electrode on the dielectric layer structure, wherein the dielectric layer structure has a thickness of about 20 Å to about 60 Å, and wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Features will be apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

[0008] FIGS. 1 to 3 are cross-sectional views of a capacitor in accordance with example embodiments;

[0009] FIG. 4 is a cross-sectional view of a capacitor in accordance with example embodiments;

[0010] FIG. 5 is a graph showing capacitance according to applied voltage of the capacitor;

[0011] FIG. 6 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments;

[0012] FIG. 7 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments;

[0013] FIG. 8 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments;

[0014] FIG. 9 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments;

[0015] FIG. 10 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments;

[0016] FIG. 11 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments;

[0017] FIGS. 12 to 14 are cross-sectional views of stages in a method of manufacturing a capacitor in accordance with example embodiments; and

[0018] FIG. 15 is a cross-sectional view of a DRAM device having a capacitor in accordance with example embodiments.

DETAILED DESCRIPTION

[0019] FIGS. 1 to 3 are cross-sectional views of a capacitor in accordance with example embodiments. FIG. 4 is a cross-sectional view of a capacitor in accordance with example embodiments.

[0020] The capacitor shown in FIGS. 1 to 3 includes a lower electrode having a pillar shape. The capacitor shown FIG. 4 includes a lower electrode having a cylindrical (e.g., hollow cylindrical) shape.

[0021] FIG. 1 is a vertical cross-sectional view of the capacitor. FIG. 2 is a horizontal cross-sectional view taken along line I-I of FIG. 1. FIG.3 is an enlarged cross-sectional view of portion A of FIG. 1.

[0022] Referring to FIGS. 1 to 4, the capacitor 180 may include a lower electrode 110, a dielectric layer structure 140, and an upper electrode 150 stacked.

[0023] In an implementation, the capacitor 180 may be on a lower structure 102 on a substrate 100. In an implementation, the lower structure 102 may include a transistor, a contact plug, a conductive line, an insulating interlayer, or the like.

[0024] Each of the lower electrode 110 and the upper electrode 150 may include metal, metal nitride, or conductive oxide. In an implementation, each of the lower electrode 110 and the upper electrode 150 may independently include, e.g., titanium nitride (TiN), titanium (Ti), tantalum (Ta), tantalum nitride (Ta₂N₃), ruthenium (Ru), tungsten, tungsten nitride, Nb, NbN, indium tin oxide (ITO), Ta-doped SnO₂, Nb-doped SnO₂, Sb-doped SnO₂, V-doped SnO₂, or the like. In an implementation, a material of the lower electrode 110 may be the same as a material of the upper electrode 150. In an implementation, materials of the lower electrode 110 and the upper electrode 150 may be different from each other. As used herein, the term “or” is not an exclusive term, e.g., “A or B” would include A, B, or A and B.

[0025] The lower electrode 110 may have various three-dimensional structures.

[0026] In an implementation, the lower electrode 110 may have a three-dimensional structure such as a cylinder shape or a pillar shape. As shown in FIGS. 1 to 3, the lower electrode 110 may have the pillar shape. As shown in FIG. 4, the lower electrode 110 may have the cylindrical (e.g., hollow cylindrical) shape.

[0027] In an implementation, the lower electrode 110 may have a two-dimensional shape such as a plate shape. In this case, the capacitor may have a shape similar to the enlarged

view shown in FIG. 3. A capacitance of the capacitor 180 may be determined by a surface area of the lower electrode 110, and the lower electrode 110 may have various modified structures for increasing of the capacitance.

[0028] The dielectric layer structure 140 may be between the lower electrode 110 and the upper electrode 150. The dielectric layer structure 140 may contact (e.g., directly contact) a surface of the lower electrode 110 to cover the surface of the lower electrode 110. The dielectric layer structure 140 may be conformally formed on the surface of the lower electrode 110. When the lower electrode 110 has the two-dimensional shape such as the plate shape, the dielectric layer structure 140 may be on an upper surface of the lower electrode 110 to have a two-dimensional shape. When the lower electrode 110 has a pillar shape or a cylinder shape, the dielectric layer structure 140 may be formed along the surface of the lower electrode 110 to have the three-dimensional shape.

[0029] For the capacitor 180 having a high capacitance, the dielectric layer structure 140 may be designed to have a high dielectric constant. In an implementation, the dielectric layer structure 140 may have a thickness of an equivalent oxide layer of about 5 Å or less, e.g., about 3.7 Å or less.

[0030] The dielectric layer structure 140 may include a plurality of stacked dielectric layers. In an implementation, the dielectric layer structure 140 may have a thickness of about 20 Å to about 60 Å. Maintaining the thickness of the dielectric layer structure 140 at about 20 Å or greater may help prevent an increase in leakage currents in the capacitor. Maintaining the thickness of the dielectric layer structure 140 at about 60 Å or less may help ensure that the capacitor has a high target capacitance. In an implementation, the dielectric layer structure 140 having a thickness of about 20 Å to about 60 Å may be suitable for a capacitor in a highly integrated semiconductor device. Hereinafter, a thickness of a layer means a

thickness of the layer in a vertical direction from a surface of a structure under the layer (e.g., a thickness in an outward direction).

[0031] The dielectric layer structure 140 may include a main dielectric layer and a sub-dielectric layer. The main dielectric layer may be a ferroelectric material having a ferroelectric property or an anti-ferroelectric property according to an electric field. A dielectric constant of the ferroelectric material may be highly increased within a switching voltage range, which is a voltage range that may be converted from the ferroelectric property to the anti-ferroelectric property or from the anti-ferroelectric property to the ferroelectric property. In this case, when the switching voltage range matches an operating voltage range of the capacitor or is within the operating voltage range of the capacitor, the dielectric constant of the dielectric layer structure may be highly increased. Thus, the capacitor may have a high capacitance in the operating voltage range.

[0032] In a highly integrated semiconductor device (e.g., a DRAM device), the semiconductor device may have a low operating voltage range, e.g., an operating voltage range of about -1 V to about 1 V. In an implementation, the highly integrated DRAM device may have the low operating voltage range of about -0.7 V to about 0.7 V. Thus, the dielectric layer structure 140 of the capacitor 180 may be boosted with a high dielectric constant in the operating voltage range of about -1 V to about 1 V.

[0033] The dielectric layer structure 140 may include a sandwich or layered structure having a hafnium oxide layer 122 and zirconium oxide layers 120 and 124 directly contacting upper and lower surfaces, respectively, of the hafnium oxide layer 122. In an implementation, the dielectric layer structure 140 may include a first stacked structure in which a first zirconium oxide layer 120/a hafnium oxide layer 122/a second zirconium oxide layer 124 are sequentially stacked. The first zirconium oxide layer 120, the hafnium

oxide layer 122, and the second zirconium oxide layer 124 included in the first stacked structure may each be crystallized or crystalline layers.

[0034] The main dielectric layer of the dielectric layer structure 140 may be the hafnium oxide layer 122. A (e.g., crystalline) hafnium oxide layer having a tetragonal crystal phase or an orthorhombic crystal phase may be the ferroelectric material having the ferroelectric property or the anti-ferroelectric property according to the electric field. The hafnium oxide layer having the tetragonal crystal phase or the orthorhombic crystal phase may have a high dielectric constant of 70 or more.

[0035] In an implementation, the dielectric constant of the dielectric layer structure 140 may be increased by using the hafnium oxide layer having the ferroelectric property. Thus, the capacitance of the capacitor may be increased by the hafnium oxide layer having the ferroelectric property. Therefore, the hafnium oxide layer 122 included in the dielectric layer structure 140 may have the tetragonal crystal phase or the orthorhombic crystal phase.

[0036] A hafnium oxide layer having a monoclinic crystal phase or an amorphous hafnium oxide layer may have no ferroelectric property. In an implementation, the hafnium oxide layer 122 included in the dielectric layer structure 140 may not have the monoclinic crystal phase and may not be amorphous. A stacked structure of the dielectric layer structure 140 may be optimized so that the hafnium oxide layer 122 may have a stable tetragonal crystal phase or a stable orthorhombic crystal phase.

[0037] A coercive field of the hafnium oxide layer 122 having the tetragonal crystal phase or the orthorhombic crystal phase may be within the operating voltage range of about -1 V to about 1 V. When the hafnium oxide layer 122 having the tetragonal crystal phase or the orthorhombic crystal phase is used as the main dielectric layer of the dielectric layer structure 140, the capacitor 180 may have a high capacitance within the operating voltage range.

[0038] Hereinafter, the hafnium oxide layer 122 may mean a hafnium oxide layer having the tetragonal crystal phase or the orthorhombic crystal phase.

[0039] The hafnium oxide layer 122 may have a thickness of about 5 Å to about 18 Å. Maintaining the thickness of the hafnium oxide layer at about 5Å or greater may help prevent leakage currents from occurring in the capacitor. Also, it may be easier to form the hafnium oxide layer having a thickness of about 5Å or greater. Maintaining the thickness of the hafnium oxide layer at about 18 Å or less may help ensure that a phase of the hafnium oxide layer is a tetragonal crystal phase or an orthorhombic crystal phase, rather than a monoclinic crystal phase.

[0040] The first and second zirconium oxide layers 120 and 124 may have a small lattice mismatch with the hafnium oxide layer 122. In an implementation, the first and second zirconium oxide layers 120 and 124 may directly contact upper and lower (e.g., inner and outer) surfaces of the hafnium oxide layer 122, respectively. Thus, a stacked structure including the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer may have a low residual stress.

[0041] If the hafnium oxide layer 122 were to directly contact the lower electrode 110 and the upper electrode 150, a lattice mismatch between the hafnium oxide layer 122 and the lower electrode 110 and a lattice mismatch between the hafnium oxide layer 122 and the upper electrode 150 may be high. Thus, a residual stress of the hafnium oxide layer 122 could be very high. In an implementation, the hafnium oxide layer may not directly contact the lower electrode 110 and the upper electrode 150.

[0042] If the residual stress of the dielectric layer structure were to be high after the dielectric layers included in the dielectric layer structure are crystallized, an electric field for changing a direction of polarization of the dielectric layers (e.g., hafnium oxide layer 122) may be increased. Accordingly, the coercive field of the dielectric layers may be increased,

and thus the electric field required for have the same polarization (P) in the dielectric layers having high residual stress may be increased.

[0043] $P = \chi_e \cdot \epsilon_0 \cdot E$, $\chi_e = \epsilon_r - 1$ (ϵ_0 : vacuum dielectric constant, ϵ_r : dielectric constant)

[0044] $C = \epsilon_0 \cdot \epsilon_r \cdot A / t$ (A: capacitor area, t: dielectric material thickness)

[0045] The electric field for having the same polarization may be increased, χ_e may be decreased, and the dielectric constant may be decreased.

[0046] If the residual stress of the dielectric layer structure were to be high, the dielectric constant of the dielectric layer structure may not be boosted at the low operating voltage range, e.g., about -1 V to about 1 V. Also, the dielectric constant of the dielectric layer structure 140 could be boosted at an operating voltage lower than -1 V and an operating voltage higher than 1 V. Thus, in order to have a high capacitance at the low operating voltage range of about -1 V to about 1 V, the residual stress of the dielectric layer structure 140 may be low.

[0047] The first and second zirconium oxide layers 120 and 124 may be crystalline. In an implementation, the first and second zirconium oxide layers 120 and 124 may have a stable tetragonal crystal phase. In an implementation, the first and second zirconium oxide layers 120 and 124 directly contacting the hafnium oxide layer 122 may be crystalline. In an implementation, the first and second zirconium oxide layers 120 and 124 may induce crystallization of the hafnium oxide layer 122 so that the hafnium oxide layer 122 may have a stable tetragonal crystal phase or an orthorhombic crystal phase during the process for forming the dielectric layer structure 140 and subsequent anneal process.

[0048] In an implementation, the first and second zirconium oxide layers 120 and 124 may have the same thickness. In an implementation, the first and second zirconium oxide layers 120 and 124 may have different thicknesses.

[0049] Each of the first and second zirconium oxide layers 120 and 124 may independently have a thickness of about 5 Å to about 30 Å. Maintaining the thickness of each of the first and second zirconium oxide layers 120 and 124 at about 5 Å or greater may help ensure that the first and second zirconium oxide layers 120 and 124 induce crystallization of the hafnium oxide layer 122 so that the hafnium oxide layer 122 may have a stable tetragonal crystal phase or an orthorhombic crystal phase. Maintaining the thickness of each of the first and second zirconium oxide layers 120 and 124 at about 30 Å or less may help ensure that the capacitor has a high target capacitance.

[0050] FIG. 5 is a graph showing capacitance according to applied voltage of the capacitor.

[0051] As shown in FIG. 5, a capacitance of the capacitor 180 in which the lower electrode 110, the dielectric layer structure 140, and the upper electrode 150 are stacked may have a hysteresis characteristic. The capacitance may be maximized within a voltage range of about -1 V to about 1 V.

[0052] In an implementation, the dielectric layer structure may include the first stacked structure in which the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer 124 are sequentially stacked, and the dielectric layer structure may further include at least one additional layer on or under the first stacked structure.

[0053] Each of the embodiments described below is the same as the capacitor described with reference to FIGS. 1 to 4, except for the dielectric layer structure. Thus, only the dielectric layer structure is mainly described.

[0054] FIG. 6 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments.

[0055] Referring to FIG. 6, the capacitor 180a may include a stack of the lower electrode 110/a dielectric layer structure 140a/ the upper electrode 150.

[0056] The dielectric layer structure 140a may include an interface layer 130 and the first stacked structure in which the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer 124 are stacked. In an implementation, the interface layer 130 may be additionally formed between the lower electrode 110 and the first zirconium oxide layer 120.

[0057] As described above, the dielectric layer structure 140a may have a thickness of about 20 Å to about 60 Å.

[0058] The hafnium oxide layer 122 may have a thickness of about 5 Å to about 18 Å. Each of the first and second zirconium oxide layers 120 and 124 may independently have the thickness of about 5 Å to about 30 Å. A thickness of the interface layer 130 may be controlled so that a sum of the thicknesses of the interface layer 130 and the first stacked structure in which the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer 124 are stacked may be equal to or less than 60 Å. In an implementation, the interface layer 130 may have a thickness less than the thickness of the first zirconium oxide layer 120.

[0059] The interface layer 130 may help prevent direct contact between the lower electrode 110 and the first zirconium oxide layer 120. The interface layer 130 may be a layer having a small lattice mismatch with the first zirconium oxide layer 120.

[0060] In an implementation, the interface layer 130 may include a ZrNbOx layer or a TiNbOx layer. In an implementation, the interface layer 130 may have a structure in which the TiNbOx layer and the ZrNbOx layer are stacked.

[0061] In an implementation, the dielectric layer structure 140a may further include the interface layer 130, and a residual stress of the dielectric layer structure 140a may be decreased. Therefore, the capacitor including the dielectric layer structure 140a may have a high capacitance.

[0062] FIG. 7 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments.

[0063] Referring to FIG. 7, the capacitor 180b may include a stack of the lower electrode 110/a dielectric layer structure 140b/ the upper electrode 150.

[0064] The dielectric layer structure 140b may include the first stacked structure 125, an insert layer 132, and a third zirconium oxide layer 134. In an implementation, the insert layer 132 and the third zirconium oxide layer 134 may be further formed on the second zirconium oxide layer 124.

[0065] The dielectric layer structure 140b may have a thickness of about 20 Å to about 60 Å. The hafnium oxide layer 122 may have the thickness of about 5 Å to about 18 Å. Each of the first and second zirconium oxide layers 120 and 124 may independently have the thickness of about 5 Å to about 30 Å. Thicknesses of the insert layer 132 and the third zirconium oxide layer 134 may be controlled, respectively, so that a sum of the thicknesses of the first stacked structure in which the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer 124 are stacked, the insert layer 132 and the third zirconium oxide layer 134 may be equal to or less than 60 Å.

[0066] The insert layer 132 may be between the second and third zirconium oxide layers 124 and 134. In an implementation, the second zirconium oxide layer 124 may be a crystallized layer, and the third zirconium oxide layer 134 may be an amorphous layer. The insert layer 132 may be an amorphous layer. In an implementation, the insert layer 132 may be amorphous, and the third zirconium oxide layer 134 may be formed on the insert layer 132 to be amorphous.

[0067] The insert layer 132 may include a metal oxide. In an implementation, the insert layer 132 may include an oxide of Al, Ta, Nb, Mo, W, Ru, V, Y, Sc, or Gd. In an

implementation, the insert layer 132 may have a thickness less than a thickness of each of the second and third zirconium oxide layers 124 and 134.

[0068] An amorphous zirconium oxide layer may have a superior surface roughness compared to a crystalline zirconium oxide layer. Thus, in the capacitor 180b having the dielectric layer structure 140b according to the present embodiment, a concentration of an electric field due to a poor surface roughness of a dielectric layer may be decreased. Thus, leakage currents of the capacitor 180b may be decreased.

[0069] FIG. 8 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments.

[0070] Referring to FIG. 8, the capacitor 180c may include a stack of the lower electrode 110/a dielectric layer structure 140c / the upper electrode 150.

[0071] The dielectric layer structure 140c may include the interface layer 130, the first stacked structure 125, the insert layer 132, and the third zirconium oxide layer 134. In an implementation, the interface layer 130 may be between the lower electrode 110 and the first zirconium oxide layer 120. The insert layer 132 and the third zirconium oxide layer 134 may be further formed on the second zirconium oxide layer 124.

[0072] The dielectric layer structure 140c may have a thickness of about 20 Å to about 60 Å. The hafnium oxide layer 122 may have the thickness of about 5 Å to about 18 Å. Each of the first and second zirconium oxide layers 120 and 124 may independently have the thickness of about 5 Å to about 30 Å. Thicknesses of the interface layer 130, the insert layer 132 and the third zirconium oxide layer 134 may be controlled, respectively, so that a sum of the thicknesses of the interface layer 130, the first stacked structure in which the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer 124 are stacked, the insert layer 132 and the third zirconium oxide layer 134 may be equal to or less than 60 Å.

[0073] A material of the interface layer 130 may be the same as the material of the interface layer illustrated with reference to FIG. 6. A material of the insert layer 132 may be the same as the material of the insert layer illustrated with reference to FIG. 7.

[0074] The dielectric layer structure 140c may have a low residual stress. In an implementation, the capacitor having the dielectric layer structure 140c may have a high capacitance, and leakage currents of the capacitor may be decreased.

[0075] FIG. 9 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments.

[0076] Referring to FIG. 9, the capacitor 180d may include a stack of the lower electrode 110/a dielectric layer structure 140d/ the upper electrode 150.

[0077] The dielectric layer structure 140d may include the interface layer 130, a first insert layer 132a, the first stacked structure 125, a second insert layer 132b, and the third zirconium oxide layer 134. In an implementation, the capacitor may further include the first insert layer 132a between the interface layer 130 and the first stacked structure 125 in the structure of the capacitor shown in FIG. 8. A material of the first insert layer 132a may be the same as the material of the insert layer illustrated with reference to FIG. 7. The first insert layer 132a may prevent materials in the first stacked structure 125 from diffusing toward the lower electrode 110.

[0078] In an implementation, the second insert layer may not be formed.

[0079] FIG. 10 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments.

[0080] Referring to FIG. 10, the capacitor 180e may include a stack of the lower electrode 110/a dielectric layer structure 140e/ the upper electrode 150.

[0081] The dielectric layer structure 140e may include the first insert layer 132a, the interface layer 130, the first stacked structure 125, the second insert layer 132b, and the

third zirconium oxide layer 134. In an implementation, the capacitor may further include the first insert layer 132a between the lower electrode 110 and the interface layer 130 in the structure of the capacitor shown in FIG. 8. A material of the first insert layer 132a may be the same as the material of the insert layer illustrated with reference to FIG. 7.

[0082] In an implementation, the second insert layer may not be formed.

[0083] In an implementation, the dielectric layer structure may further include an insert layer between the interface layer 130 and the first stacked structure 125 in the dielectric layer structure shown in FIG. 10. In an implementation, a stacked structure including an insert layer/an interface layer/an insert layer may be between the lower electrode 110 and the first stacked structure 125.

[0084] FIG. 11 is an enlarged cross-sectional view of a capacitor in accordance with example embodiments.

[0085] Referring to FIG. 11, the capacitor 180f may include a stack of the lower electrode 110/a dielectric layer structure 140f/ the upper electrode 150.

[0086] The dielectric layer structure 140f may include the first insert layer 132a, the first stacked structure 125, the second insert layer 132b, and the third zirconium oxide layer 134. In an implementation, the dielectric layer structure 140f may not include an interface layer, and may further include the first insert layer 132a between the lower electrode 110 and the first stacked structure 125 in the dielectric layer structure shown in FIG. 10. A material of the first insert layer 132a may be the same as the material of the insert layer illustrated with reference to FIG. 7. In an implementation, the second insert layer may not be formed.

[0087] FIGS. 12 to 14 are cross-sectional views of stages in a method of manufacturing a capacitor in accordance with example embodiments.

[0088] Hereinafter, an example of a method of manufacturing a capacitor including a lower electrode having a pillar shape is described.

[0089] Referring to FIG. 12, a mold layer 104 may be formed on a substrate. A portion of the mold layer 104 may be etched to form a hole. The hole may be formed at a portion for forming a lower electrode.

[0090] In an implementation, before forming the mold layer 104, a lower structure 102 may be further formed on the substrate 100. The lower structure 102 may include lower circuits including a transistor, a contact plug, and a conductive line and an insulating interlayer covering the lower circuits.

[0091] A lower electrode layer may be formed on the mold layer 104 to fill the hole. The lower electrode layer may be planarized until an upper surface of the mold layer 104 may be exposed to form a lower electrode 110 in the hole.

[0092] In an implementation, the lower electrode layer may be deposited by a deposition process such as a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, or an atomic layer deposition (ALD) process. The planarization process may include a chemical mechanical polishing (CMP) process or an etch back process.

[0093] In an implementation, the lower electrode layer may be formed on the lower structure 102. The lower electrode layer may be patterned by a photolithography process to form the lower electrode 110. In this case, the mold layer may not be formed on the lower structure 102.

[0094] Referring to FIG. 13, the mold layer 104 may be removed. Thus, a surface of the lower electrode 110 having a pillar shape may be exposed.

[0095] A first zirconium oxide layer 120 may be conformally formed on surfaces of the lower electrode 110 and the lower structure 102 to have a uniform thickness. A hafnium oxide layer 122 may be formed on the first zirconium oxide layer 120. A second zirconium oxide layer 124 may be formed on the hafnium oxide layer 122. Thus, a first stacked structure in which the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the

second zirconium oxide layer 124 are stacked may be formed on the lower electrode 110 and the lower structure 102.

[0096] The hafnium oxide layer 122 may be formed to have a tetragonal crystal phase or an orthorhombic crystal phase. Each of the first and second zirconium oxide layers 120 and 124 may be formed to have a crystalline phase. In an implementation, each of the first and second zirconium oxide layers 120 and 124 may have a tetragonal crystal phase, which is a stable phase.

[0097] The dielectric layer structure 140 may have a thickness of about 20 Å to about 60 Å. Each of the first and second zirconium oxide layers 120 and 124 may independently have a thickness of about 5 Å to about 30 Å. The hafnium oxide layer 122 may have a thickness of about 5 Å to about 18 Å.

[0098] In an implementation, each of the first zirconium oxide layer 120, the hafnium oxide layer 122, and the second zirconium oxide layer 124 may be formed by an atomic layer deposition (ALD) process. The deposition process of each of the first zirconium oxide layer 120, the hafnium oxide layer 122, and the second zirconium oxide layer 124 may be performed at a relatively low temperature, e.g., of about 200 °C to about 450 °C. Performing the deposition process of each of the first zirconium oxide layer 120, hafnium oxide layer 122, and second zirconium oxide layer 124 at about 200°C or greater may help ensure that each of precursors may be thermally decomposed, and the layers may be suitably deposited. Performing the deposition process of each of the first zirconium oxide layer 120, the hafnium oxide layer 122, and the second zirconium oxide layer 124 at about 450 °C or less may help ensure that the layers grow stably. In an implementation, the deposition process of each of the first zirconium oxide layer 120, the hafnium oxide layer 122, and the second zirconium oxide layer 124 may be performed at a temperature of about 200 °C to about 320 °C.

[0099] In an implementation, in the deposition process of each of the first zirconium oxide layer 120, the hafnium oxide layer 122, and the second zirconium oxide layer 124, an oxidant may include O_3 , H_2O , or O_2 .

[00100] In an implementation, each of the first zirconium oxide layer 120, the hafnium oxide layer 122, and the second zirconium oxide layer 124 may be formed in a deposition apparatus of a batch-type. In an implementation, each of the first zirconium oxide layer 120, the hafnium oxide layer 122, and the second zirconium oxide layer 124 may be formed in a deposition apparatus of single wafer type.

[00101] In an implementation, a deposition chamber for forming the first and second zirconium oxide layers 120 and 124 and a deposition chamber for forming the hafnium oxide layer 122 may be different from each other. In an implementation, a deposition chamber for forming the first and second zirconium oxide layers 120 and 124 and a deposition chamber for forming the hafnium oxide layer 122 may be the same.

[00102] In an implementation, the hafnium oxide layer 122 may be formed between the first and second zirconium oxide layers 120 and 124, and the first stacked structure including the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer stacked may have a low residual stress.

[00103] The hafnium oxide layer 122 may be crystallized at a low temperature, during forming the hafnium oxide layer 122 and the second zirconium oxide layer 124 on the hafnium oxide layer 122. Thus, the hafnium oxide layer 122 may have a tetragonal crystal phase or an orthorhombic crystal phase. In addition, the first and second zirconium oxide layers 120 and 124 may be also crystallized during forming the first and second zirconium oxide layers 120 and 124 and the hafnium oxide layer 122. Thus, the first and second zirconium oxide layers 120 and 124 may have a stable tetragonal crystal phase.

[00104] In an implementation, before forming the first zirconium oxide layer 120, an interface layer (refer to FIG. 6, 130) may be further formed on surfaces of the lower electrode 110 and the lower structure 102 to have a uniform thickness. In an implementation, the interface layer 130 may be formed by an atomic layer deposition process. The deposition process of the interface layer 130 may be performed at a low temperature of about 200 °C to about 450 °C. In an implementation, the deposition process of the interface layer 130 may be performed at a temperature of about 200 °C to about 320 °C. In this case, the capacitor as shown in FIG. 6 may be formed by subsequent processes.

[00105] In an implementation, an insert layer (refer to FIG. 7, 132) and a third zirconium oxide layer (refer to FIG. 7, 134) may be further formed on the second zirconium oxide layer 124. The insert layer 132 may include a metal oxide. In an implementation, the insert layer 132 may include an oxide of Al, Ta, Nb, Mo, W, Ru, V, Y, Sc, or Gd. In an implementation, the insert layer 132 may be formed to have a thickness less than a thickness of each of the second and third zirconium oxide layers 124 and 134. In an implementation, the insert layer 132 and the third zirconium oxide layer 134 may be formed by an atomic layer deposition process. The deposition processes of the insert layer 132 and the third zirconium oxide layer 134 may be performed at a low temperature of about 200 °C to about 450 °C. In an implementation, the deposition processes of the insert layer 132 and the third zirconium oxide layer 134 may be performed at a temperature of about 200 °C to about 320 °C. In this case, the capacitor as shown in FIG. 7 may be formed by subsequent processes.

[00106] In an implementation, before forming the first zirconium oxide layer 120, an interface layer (refer to FIG. 8, 130) may be further formed on surfaces of the lower electrode 110 and the lower structure 102 to have a uniform thickness. An insert layer

(refer to FIG. 8, 132) and a third zirconium oxide layer (refer to FIG. 8, 134) may be further formed on the second zirconium oxide layer 124. In this case, the capacitor as shown in FIG. 8 may be formed by subsequent processes.

[00107] One of the capacitors shown in FIGS. 9 to 11 may be formed by additionally performing the processes of forming an interface layer and/or insert layers and subsequent processes.

[00108] Referring to FIG. 14, an upper electrode 150 may be formed on the second zirconium oxide layer 124.

[00109] In an implementation, the upper electrode 150 may be formed of a material the same as a material of the lower electrode 110. In an implementation, the upper electrode 150 may be formed of a material different from a material of the lower electrode 110.

[00110] In an implementation, the upper electrode 150 may be formed by a deposition process such as a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, and atomic layer deposition (ALD) process.

[00111] In an implementation, after forming the upper electrode 150, an anneal process may be further performed. When the anneal process is performed, the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer 124 included in the dielectric layer structure 140 may be additionally or further crystallized. In an implementation, the anneal process may be performed at a temperature higher than temperatures of deposition processes for forming the dielectric layer structure 140.

[00112] As described above, the hafnium oxide layer 122 included in the dielectric layer structure 140 may have the tetragonal crystal phase or the orthorhombic crystal phase. The zirconium oxide layers 120 and 124 may be formed on the upper and lower (e.g., inner and outer) surfaces of the hafnium oxide layer 122, respectively, so that residual stress of

the dielectric layer structure 140 may be decreased. Thus, the dielectric layer structure 140 may have a low coercive field, and a capacitance of the capacitor may be highly increased within a range of about -1V to about 1V, which is an operating voltage range of the capacitor including the dielectric layer structure 140.

[00113] FIG. 15 is a cross-sectional view of a DRAM device having a capacitor in accordance with example embodiments.

[00114] Although the DRAM device is only shown in FIG. 15, the capacitor may be used in all memory devices using the capacitor as a data storage unit.

[00115] Referring to FIG. 15, the DRAM device may include a cell transistor, a capacitor, and a bit line formed on a substrate. The DRAM device may include a unit cell including one cell transistor and one capacitor.

[00116] The substrate 200 may include an active region and a field region. The field region may be a region in which an isolation layer 220 is formed in an isolation trench included in the substrate 200. The active region may be a region of the substrate other than the field region.

[00117] A gate trench 202 extending in a first direction parallel to an upper surface of the substrate 200 may be formed at an upper portion of the substrate 200. A gate structure 210 may be formed in the gate trench 202.

[00118] In an implementation, the gate structure 210 may include a gate insulation layer 204, a gate electrode 206, and a capping insulation pattern 208. A plurality of gate structures 210 may be arranged in a second direction parallel to the upper surface of the substrate 200 and perpendicular to the first direction.

[00119] The gate insulation layer 204 may include silicon oxide. The gate electrode 206 may include a metal material or polysilicon. The capping insulation pattern 208 may include silicon nitride.

[00120] Impurity regions 230 serving as source/drain regions may be formed at the active region of the substrate 100 between the gate structures 210.

[00121] In an implementation, the impurity regions 230 may include a first impurity region 230a electrically connected to a bit line structure 260 and a second impurity region 230b electrically connected to a capacitor 180.

[00122] A pad insulation pattern 240, a first etch stop pattern 242, and a first conductive pattern 246 may be formed on the active region, the isolation layer 220, and the gate structure 210. The pad insulation pattern 240 may include an oxide such as silicon oxide, and the first etch stop pattern 242 may include a nitride such as silicon nitride. The first conductive pattern 246 may include polysilicon doped with impurities.

[00123] A recess portion may pass through a stacked structure including the pad insulation pattern 240, the first etch stop pattern 242, and the first conductive pattern 246. The recess portion may be disposed at a portion of the substrate 100 between the gate structures. An upper surface of the first impurity region 230a may be exposed by a bottom of the recess portion.

[00124] A second conductive pattern 248 may be formed to fill the recess portion. The second conductive pattern 248 may include, e.g., polysilicon doped with impurities. In an implementation, the second conductive pattern 248 may contact the first impurity region 230a.

[00125] A third conductive pattern 250 may be stacked on the first conductive pattern 246 and the second conductive pattern 248. The third conductive pattern 250 may include, e.g., polysilicon doped with impurities. As the first to third conductive patterns 246, 248, and 250 include substantially the same material, the first to third conductive patterns 246, 248, and 250 may be merged into one pattern. A barrier metal pattern 252, a metal pattern 254, and a hard mask pattern 256 may be stacked on the third conductive pattern 250.

[00126] A stacked structure including the first conductive pattern 246, the second conductive pattern 248, the third conductive pattern 250, the barrier metal pattern 252, the metal pattern 254, and the hard mask pattern 256 may serve as a bit line structure 260.

[00127] In an implementation, the second conductive pattern 248 may serve a bit line contact, and the first conductive pattern 246, the third conductive pattern 250, the barrier metal pattern 252 and the metal pattern 254 may serve as a bit line. The bit line structure 260 may extend in the second direction. A plurality of bit line structures 260 may be arranged in the first direction.

[00128] In an implementation, a spacer may be formed on sidewalls of the bit line structure 260.

[00129] In an implementation, a first insulating interlayer may be formed to fill a portion between the bit line structures 260.

[00130] A contact plug 270 may be formed through the first insulating interlayer, the first etch stop pattern 242 and the pad insulation pattern 240. The contact plug 270 may contact the second impurity region 230b. The contact plug 270 may be between the bit line structures 260.

[00131] A capacitor 180 may be formed on the contact plug 270.

[00132] The capacitor 180 may include a lower electrode 110, a dielectric layer structure 140, and an upper electrode 150. The dielectric layer structure 140 may include a stack of the first zirconium oxide layer 120/ the hafnium oxide layer 122/ the second zirconium oxide layer 124.

[00133] The capacitor 180 may have a structure the same as a structure of the capacitor as illustrated with reference to FIG. 1. In an implementation, the capacitor may have a structure the same as a structure of one of the capacitors illustrated with reference to FIGS. 6 to 8.

[00134] A plate electrode 160 may be further formed on the upper electrode 150. The plate electrode 160 may include polysilicon doped with impurities.

[00135] The DRAM device may be operated in the operating voltage range of about -1V to about 1V. In the capacitor, a dielectric constant of the dielectric layer structure may be highly boosted in the operating voltage range of about -1 V to about 1 V, and thus a capacitance of the capacitor may be greatly increased. The DRAM device may have excellent electrical characteristics.

[00136] By way of summation and review, as a DRAM device is highly integrated, it may be difficult for the capacitor included in the DRAM to have high capacitance and low leakage currents.

[00137] One or more embodiments may provide a capacitor having a high capacitance.

[00138] One or more embodiments may provide a DRAM device including a capacitor having a high capacitance.

[00139] In example embodiments, the dielectric layer structure included in the capacitor may have a ferroelectric property within an operating voltage range, e.g., the operating voltage range of about -1 V to about 1 V. The capacitor may have a high capacitance within the operating voltage range.

[00140] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it

will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A capacitor, comprising:
 - a lower electrode;
 - a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and
 - an upper electrode on the dielectric layer structure,
 - wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase.
2. The capacitor as claimed in claim 1, wherein the first zirconium oxide layer and the second zirconium oxide layer are each crystalline.
3. The capacitor as claimed in claim 2, wherein the first zirconium oxide layer and the second zirconium oxide layer have an orthorhombic crystal phase.
4. The capacitor as claimed in any one of claims 1 to 3, wherein the hafnium oxide layer has a thickness of about 5 Å to about 18 Å.
5. The capacitor as claimed in any one of claims 1 to 4, wherein each of the first zirconium oxide layer and the second zirconium oxide layer independently has a thickness of about 5 Å to about 30 Å.

6. The capacitor as claimed in any one of claims 1 to 5, wherein the dielectric layer structure has a thickness of about 20 Å to about 60 Å.

7. The capacitor as claimed in any one of claims 1 to 6, wherein the dielectric layer structure further includes an interface layer, the interface layer being between the first zirconium oxide layer and the lower electrode.

8. The capacitor as claimed in claim 7, wherein the interface layer includes a ZrNbOx layer, a TiNbOx layer, or a stacked structure of the TiNbOx layer and the ZrNbOx layer.

9. The capacitor as claimed in any one of claims 1 to 8, wherein the dielectric layer structure further includes an insert layer and a third zirconium oxide layer, the insert layer including an oxide of Al, Ta, Nb, Mo, W, Ru, V, Y, Sc, or Gd.

10. The capacitor as claimed in claim 9, wherein the insert layer and the third zirconium oxide layer are amorphous.

11. The capacitor as claimed in any one of claims 1 to 10, wherein the lower electrode includes a metal, a metal nitride, or a conductive oxide.

12. A capacitor, comprising:
a lower electrode;

a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and

an upper electrode on the dielectric layer structure,

wherein:

the dielectric layer structure has a thickness of about 20 Å to about 60 Å, and

the first zirconium oxide layer, the hafnium oxide layer, and the second zirconium oxide layer are each crystalline.

13. The capacitor as claimed in claim 12, wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase.

14. The capacitor as claimed in claim 12 or claim 13, wherein the first zirconium oxide layer and the second zirconium oxide layer each have a tetragonal crystal phase.

15. The capacitor as claimed in any one of claims 12 to 14, wherein the hafnium oxide layer has a thickness of about 5 Å to about 18 Å.

16. The capacitor as claimed in any one of claims 12 to 15, wherein each of the first zirconium oxide layer and the second zirconium oxide layer independently has a thickness of about 5 Å to about 30 Å.

17. The capacitor as claimed in any one of claims 12 to 16, wherein the dielectric layer structure further includes an interface layer, the interface layer being between the first zirconium oxide layer and the lower electrode.

18. The capacitor as claimed in any one of claims 12 to 17, wherein:
the dielectric layer structure further includes an insert layer and a third zirconium oxide layer, and
the insert layer includes an oxide of Al, Ta, Nb, Mo, W, Ru, V, Y, Sc, or Gd.

19. A dynamic random-access memory (DRAM) device, comprising:
a substrate;
a cell transistor on the substrate, the cell transistor including a gate structure, a first impurity region, and a second impurity region;
a bit line structure electrically connected to the first impurity region; and
a capacitor on the bit line structure, the capacitor being electrically connected to the second impurity region,
wherein the capacitor includes:

a lower electrode;
a dielectric layer structure on the lower electrode, the dielectric layer structure including a first zirconium oxide layer, a hafnium oxide layer, and a second zirconium oxide layer sequentially stacked; and
an upper electrode on the dielectric layer structure,
wherein the dielectric layer structure has a thickness of about 20 Å to about 60 Å,
and
wherein the hafnium oxide layer has a tetragonal crystal phase or an orthorhombic crystal phase.

20. The DRAM device as claimed in claim 19, wherein the first zirconium oxide layer and the second zirconium oxide layer are each crystalline.