

## ABSTRACT

A semiconductor device includes a source layer; a plurality of channel structures; a plurality of gate electrodes; and a common source line. At least one of the plurality of gate electrodes provides a GIDL line. For an erasing operation, an erasing voltage applied to the common source line reaches a target voltage, and, after the erasing voltage reaches the target voltage, a step increment voltage is applied to the erasing voltage, such that the erasing voltage has a voltage level higher than a voltage level of the target voltage. After the step increment voltage has been applied for a desired time period, the voltage level of the erasing voltage is decreased to the target voltage level for the remainder of the erasing operation.

FIG. 4