LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF DRIVING SAME

The present invention relates to liquid crystal display devices and methods of driving the same, in which elements of non-linear characteristic are provided on one of the substrates thereof.

In a known active matrix of elements of the two terminal type, in which there is a column electrode on one of the substrates and a row electrode on the other, a liquid crystal display layer is encapsulated in the space between the substrates, and non-linear characteristic elements are disposed between the liquid crystal layer and the column electrode or between the liquid crystal layer and the row electrode. Such non-linear characteristic elements may be:-

(1) ceramic varistors (D.E. Casfeleberry. IEEE. ED-26, 1979, from page 1123 to page 1128);

(2) amorphous silicon PN diodes (Togashi et al, Television Association Technical Report, ED 782, IPD 86-3, 1984, Japanese Laid Open Application No. 57273/84); and

(3) MIM (Metal Insulator Metal) elements (D.R. Baraff et al., IEEE. ED-28, 1981, from page 736 to page 739 and K. Niwa et al., SID 84 DIGEST, 1984, from page 304 to page 307).

Several driving methods for each active matrix are suggested, but all use the switching function of non-linear elements as shown in Figure 2, thereby controlling the amount of electric charge supplied to the liquid crystal display layers.

In a prior art liquid crystal display device, there is a matrix of row electrodes 601 (Figure 1) and column electrodes 602. At each intersection is a non-linear element 603 and a liquid crystal layer 604 in series. The voltages applied across the non-linear element 603 and the liquid crystal layer 604 are hereinafter referred to as V_{NL} and V_{LC}, respectively.

The non-linear element 603 has a switching characteristic shown in Figure 2, so that a sudden increase in current occurs when the voltage applied exceeds a threshold voltage V_{th}.

In use, the common line driving wave form C (Figure 3) is applied to a column electrode 602 and data line driving wave form D to row electrode 601, thereby driving the display device by time sharing or high duty driving. The hatched portion C-D shows the voltage which is applied to the liquid crystal layer 604, V_{th} being the threshold voltage of the non-linear element 603 at which current increases sharply. The effective voltage applied to the liquid crystal layer is extremely low during non-selected term, thereby improving the ON signal to OFF signal ratio of liquid crystal material to obtain high contrast.

When a display is to be driven by high duty driving modified according to the grey scale, the pulse width of ON signal during the selected term is modulated or controlled in accordance with grey scale data to realise grey scale display. In a conventional data line driving circuit for this purpose (Figure 4), a counter 401 is driven by clock signals f to give binary output signals Q_0, Q_1, Q_2 and Q_3. Figure 5 is a time chart of the conventional

data line driving circuit. The selected time width T corresponds to pulse widths 301 and 302 shown in Figure 3. Therefore there are sixteen clock signals f in one time period T. The counter 401 counts sixteen clock signals f and outputs binary signals after 1, 2, 4 and 8 signals. The output signals Q_0, Q_1, Q_2 and Q_3 are passed to a reference grey scale pulse forming circuit 405 whose output pulses P_0, P_1, P_2 and P_3 are of widths 1/f, 2/f, 4/f and 8/f, respectively (Figure 5), or in the particular case T/16, T/8, T/4 and T/2. A memory 402 stores digital data converted from analogue data relating to grey scale level. The memory has a capacity of four bits with respective binary output signals M_0, M_1, M_2 and M_3. Four AND gates 406 receive pairs of signals M_0 to M_3 from the memory 402 and P_0 to P_3 from the reference grey scale pulse forming circuit 405. The outputs of the AND gates 406 are ORd in OR gate 403 which can thus generate an output signal selected from sixteen different width signals as shown in Figure 5, depending on data stored in the memory 402. Depending on the output signal from the gate 403, a transmission gate 404 controls whether the ON voltage V_{ON} or the OFF voltage V_{OFF} is selected to be output from the transmission gate 404 to the row electrode as data line driving signal D.

When a data line driving signal is output from the driving circuit, the voltage applied to the non-linear element 603 and the liquid crystal layer 604, being the voltage applied to the row electrode 601 and the column electrode 602, is shown in Figure 6. In this case, the grey scale data (M_0, M_1, M_2, M_3) = (0, 1, 0, 1), so that during the ON time t_1, because V_{NL} is

greater than V_{th}, a high current flows through the non-linear element 603 to charge the liquid crystal layer 604, whereby V_{LC} is increased. However, during the OFF time t_2, the liquid crystal layer is not discharged because V_{NL} is reduced below V_{th}. Accordingly, V_{LC} is not substantially reduced. During ON time t_3, V_{NL} is increased again, and V_{LC} increases to the point where V_{NL} is equal to V_{th}. Thus this driving method does not provide an accurate grey scale display using pulse width modulation, when ON times are separated by OFF times due to the charge holding characteristic of the element when V_{LC} is not reduced in OFF time.

It was difficult to display according to grey scale in the active matrix using non-linear elements driven with high duty by the conventional method described above. The object of the present invention is to provide an active matrix using non-linear elements which enables the display according to grey scale by the use of a simple circuit.

In order to attain the object, the present invention provides a plurality of column electrodes and a plurality of row electrodes in the form of a matrix, a liquid crystal display layer disposed between the column electrodes and the row electrodes, switch elements having non-linear volt-ampere characteristics at intersections of the column and row electrodes between the liquid crystal display layer and either the column electrode or the row electrode, a common line driving circuit for generating a voltage to individual column electrodes, and a data line driving circuit for generating a voltage to individual row electrodes, the

row electrode voltage including an ON pulse comprising a pulse width modulated signal based upon a grey scale display indication, the column electrode voltage during a selected time being such that, in combination with an ON pulse on an intersecting row electrode, the relevant switch element triggers to charge the display layer, and during a non-selected time is insufficient to trigger the switch element, the ON pulse being present only during the selected time column electrode voltage, and the start of the pulse width modulated signal being so controlled that the ON pulse is continuous or undivided during that selected time.

The ON pulse may continue until the end of the selected time. Thus, the pulse width modulated signal ON pulse from the data line driving circuit is gathered at the end of selected time, thereby applying voltage which corresponds to the duty of selected signal to the liquid crystal layer, and the grey scale can be displayed with high duty driving by an active matrix liquid crystal display device using a non-linear element. Preferably, the grey scale display indication is in the form of a plurality of binary signals, whose complement is compared to the binary signal output of a clock signal counter to start the ON pulse upon agreement.

In a preferred embodiment, the comparison is made by means of EX-NOR circuits and an AND gate to operate a latch which is re-set at the end of the selected time. Conveniently, there is a four bit binary output grey scale signal and a four bit binary output counter signal.

In an advantageous modification of the invention, at the end of the selected time, a discharge signal of opposite polarity to that previously applied to the respective electrode is applied to the column electrode and to the row electrode, so as to discharge electric charge stored in the liquid crystal layer during the selected time. By discharging the electric charge stored in the liquid crystal display layer at the end of selected time, cross talk of data signals between columns is controlled.

According to another aspect of the present invention, there is provided a method of driving a liquid crystal display device including a plurality of column electrodes and a plurality of row electrodes in the form of a matrix, a liquid crystal display layer disposed between the column electrodes and the row electrodes, and switch elements having non-linear volt-ampere characteristics at inter-sections of the column and row electrodes between the liquid crystal display layer and either the column or row electrode, the method comprising applying a voltage to individual column electrodes, and applying a voltage to individual row electrodes, the row electrode voltage including an ON pulse comprising a pulse width modulated signal based upon a grey scale display indication, the column electrode voltage during a selected time being such that, in combination with an ON pulse on an inter-secting row electrode, the relevant switch element triggers to charge the display layer, and during a non-selected time is insufficient to trigger the switch element, the ON pulse being present only during the

selected time column electrode voltage, and the start of the pulse width modulated signal being so controlled that the ON pulse is continuous or undivided during that selected time.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of the components of a picture element at the intersection of column and row electrodes in a known display device;

Figure 2 shows the characteristic volt-ampere curve of a non-linear element forming one component of the picture element;

Figure 3 shows the wave forms of the voltages applied to the column and row electrodes of the picture element;

Figure 4 shows a known data line driving circuit for generating a voltage to a row electrode which includes a pulse width modulated signal based upon a grey scale display indication;

Figure 5 is a time chart of the pulses in parts of the circuit of Figure 4;

Figure 6 shows the wave form of the pulse width modulated signal derived from the circuit of Figure 4;

Figure 7 is a block diagram of a liquid crystal display device according to the present invention;

Figure 8 is a time chart of the pulses in part of the circuit of Figure 7;

Figure 9 shows the wave forms of two pulse width modulated signals derived from the circuit of Figure 7;

Figure 10 shows the wave forms of the voltages applied to the column and row electrodes of the device according to the present invention;

Figure 11 shows the wave forms of the voltages applied to the column and row electrodes of a modified embodiment of the present invention; and

Figure 12 is a time chart, similar to part of Figure 8, of pulses in parts of the circuit for the modified embodiment of Figure 11.

In a first embodiment of the present invention (Figure 7) a liquid a liquid crystal video display device includes a video display portion 101 comprising a matrix of picture elements. Each picture element comprises a non-linear characteristic element 106 and a liquid crystal layer 107 connected to the non-linear element

in series between column and row electrodes 105 and 104, respectively. The non-linear element 106 is disposed between the column electrode 105 and the layer 107 though it could be between the layer 107 and the row electrode 104. A common line driving circuit 102 has as an output a common line driving signal C to the column electrode 105. As shown in Figure 10, during a selected time T, a large effective voltage is applied to the liquid crystal layer.

During the non-selected time, a small effective voltage is applied to the liquid crystal layer. A data line driving circuit 103 (Figure 7) has as an output a data line driving signal D to the row electrode 104. Signal D includes a pulse width modulation signal during the selected time T, in which the ON pulse is gathered at the end as shown in Figure 10.

The data line driving circuit 103 includes a clock counter 108 which outputs binary signals Q_0, Q_1, Q_2 and Q_3 under the control of input clock signals f. A memory 109 stores the grey scale data as four binary signals M_0, M_1, M_2 and M_3. The output of the memory 109 is, however, the complement of these signals, namely $\bar{M}_0$, $\bar{M}_1$, $\bar{M}_2$, and $\bar{M}_3$. Four EX-NOR gates 113 compare the output signals Q_0, Q_1, Q_2 and Q_3 from the counter 108 and the output signals $\bar{M}_0$, $\bar{M}_1$, $\bar{M}_2$ and $\bar{M}_3$ from the memory 109. and provide outputs upon agreement to an AND gate 110. Thus the gate 110 detects complete agreement of data from the counter 108 and the memory 109 and then provides an output signal to set a resettable latch 111. The resettable latch 111 is reset by signal R at the beginning of the selected time T as shown in

Figure 8. Thus, the circuit generates a signal pulse width modulated in accordance with the code stored in the memory 109. The output signal from the latch 111 is transferred to a transmission gate 112 which controls the selection of ON voltage (V_{ON}) or OFF voltage (V_{OFF}).

The table below indicates the outputs of the counter 108 and the memory 109 for grey scale indications stored in the memory, from which the start of the pulse width modulated signals shown in Figure 8 can be derived.

Q_0	Q_1	Q_2	Q_3	$\bar{M}_0$	$\bar{M}_1$	$\bar{M}_2$	$\bar{M}_3$	M_0	M_1	M_2	M_3	
0	0	0	0	0	0	0	0	1	1	1	1	t_0
1	0	0	0	1	0	0	0	0	1	1	1	t_1
0	1	0	0	0	1	0	0	1	0	1	1	t_2
1	1	0	0	1	1	0	0	0	0	1	1	t_3
0	0	1	0	0	0	1	0	1	1	0	1	t_4
1	0	1	0	1	0	1	0	0	1	0	1	t_5
0	1	1	0	0	1	1	0	1	0	0	1	t_6
1	1	1	0	1	1	1	0	0	0	0	1	t_7
0	0	0	1	0	0	0	1	1	1	1	0	t_8
1	0	0	1	1	0	0	1	0	1	1	0	t_9
0	1	0	1	0	1	0	1	1	0	1	0	t_{10}
1	1	0	1	1	1	0	1	0	0	1	0	t_{11}
0	0	1	1	0	0	1	1	1	1	0	0	t_{12}
1	0	1	1	1	0	1	1	0	1	0	0	t_{13}
0	1	1	1	0	1	1	1	1	0	0	0	t_{14}
1	1	1	1	1	1	1	1	0	0	0	0	t_{15}

In order to accommodate the reset signal R, there are seventeen clock signals f during selected time T as shown in Figure 8.

It will be noted that, even in the case where one of the binary signals held in the memory 109 is 0 between two 1 signals, a continuous ON pulse is obtained by correct selection of the start.

Figure 9 shows the wave form of the voltage applied to the liquid crystal layer 107 (the voltage applied to the row electrode 104 and the column electrode 105) when the data line is driven by the data line driving circuit 103. Figure 9(a) shows the wave form when M_0, M_1, M_2 and M_3 are 0, 1, 1 and 1, respectively. Figure 9(b) shows the wave form when M_0, M_1, M_2 and M_3 are 1, 1, 0 and 0, respectively. In both cases, V_{LC} is applied to the liquid crystal layer by gathering the ON pulse to the latter end portion during the selected time. This is achieved by controlling the start of the ON pulse in accordance with the complement of the stored grey scale indication. V_{LC} corresponds to the voltage applied to a liquid crystal layer during a pulse width modulated signal.

Figure 10 illustrates the driving wave forms of the liquid crystal portion, the axis of time being extended. As can be seen from Figure 10, the ON pulses during the selected time are gathered at the end, signals C (Figure 10(a)) and D (Figure 10(b)) being applied to the column electrode and the row electrode, respectively, thereby forming the differential voltage C-D as shown in Figure 10(c). As illustrated in Figure 9, during

the selected time, the voltage V_{LC} is applied to the liquid crystal layer during a pulse width modulated signal. However, during the non-selected time which follows the selected time, the voltage V_{NL} is very high and the polarity thereof is opposite to that during the selected time because the liquid crystal layer is charged with electric charge during the selected time. As a result, as shown by the curves 1001 and 1002, the wave may be modulated by the adjacent data line driving voltage. The modulated wave causes cross talk defect produced between columns in the display.

Accordingly, in a preferred modified embodiment of the invention (Figure 11), in order to overcome this defect, signals C (Figure 11(a)) and D (Figure 11(b)) are modified. With respect to the signal C (Figure 11(a)) , the pulses 1003 and 1004 are added at the end of the selected time T. These pulses have opposite polarity to those of the foregoing selected time. With respect to the signal D (Figure 11(b)), a pulse 1005 or 1006 of optional OFF voltage level is added at the end of the selected time T. As a result, differential voltage C-D includes pulses 1007 and 1008 which act as discharging signals at the end of the selected time T, so that the electrical charge stored in the liquid crystal layer during the selected time is fully discharged. Preferably, V_{NL} is lower than V_{th}, i.e. $V_{NL} < V_{th}$. Because V_{NL} is low in the following selected time, the cross talk caused by data line driving voltage in the adjacent column in Figure 10(c) can be prevented as shown in Figure 11(c). As an example of the circuit for forming

the modified signal D of Figure 11(b), the pulse of reset signal R is widened (Figure 12) so as to be included at the end of selected time T in Figure 8, in order that a pulse of OFF level be set up during the OFF time at the end of the selected time T.

As described above, in an active matrix liquid crystal display device of non-linear element type according to the present invention the ON pulse width modulated signal generated from the data line driving circuit is gathered at the end of selected time and the voltage corresponding to the duty of the selected signal is applied to the liquid crystal layer, so that accurate grey scale image can be reproduced in the display with high duty driving method.

Further, the cross talk caused by data signal between columns can be controlled by generating the discharging signal for discharging the load held in the liquid crystal layer at the end of the selected time.

The present invention provides an improved liquid crystal video display device in which elements of non-linear characteristic are provided on one of the substrates thereof. In the liquid crystal video display device according to the present invention, the ON pulses of pulse width modulated signal generated from data line driving circuit are gathered at the end of selected time and a signal for discharging charge stored in liquid crystal layers is applied to a row electrode and a column electrode, so that grey scale of image can be displayed with a simplified circuit for a liquid crystal display. In the specification, the ON pulse stands for the pulse for turning on the liquid

crystal display. The OFF pulse stands for the pulse for turning off the liquid crystal display.

C L A I M S

1. A liquid crystal display device including a plurality of column electrodes and a plurality of row electrodes in the form of a matrix, a liquid crystal display layer disposed between the column electrodes and the row electrodes, switch elements having non-linear volt-ampere characteristics at intersections of the column and row electrodes between the liquid crystal display layer and either the column electrode or the row electrode, a common line driving circuit for generating a voltage to individual column electrodes, and a data line driving circuit for generating a voltage to individual row electrodes, the row electrode voltage including an ON pulse comprising a pulse width modulated signal based upon a grey scale display indication, the column electrode voltage during a selected time being such that, in combination with an ON pulse on an intersecting row electrode, the relevant switch element triggers to charge the display layer, and during a non-selected time is insufficient to trigger the switch element, the ON pulse being present only during the selected time column electrode voltage, and the start of the pulse width modulated signal being so controlled that the ON pulse is continuous or undivided during that selected time.

2. A device according to claim 1, wherein the ON pulse continues until the end of the selected time.

3. A device according to claim 1 or 2, wherein the grey scale display indication is in the form of a

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plurality of binary signals, whose complement is compared to the binary signal output of a clock signal counter to start the ON pulse upon agreement.

4. A device according to claim 3, wherein the comparison is made by means of EX-NOR circuits and an AND gate to operate a latch which is re-set at the end of the selected time.

5. A device according to claim 3 or 4, wherein there is a four bit binary output grey scale signal and a four bit binary output counter signal.

6. A device according to any preceding claim, wherein, at the end of the selected time, a discharge signal of opposite polarity to that previously applied to the respective electrode is applied to the column electrode and to the row electrode, so as to discharge electric charge stored in the liquid crystal layer during the selected time.

7. A liquid crystal display device substantially as herein described and shown in Figures 7 to 10 of the accompanying drawings.

8. A liquid crystal display device substantially as herein described and shown in Figures 7 to 10 and as modified in Figure 11 of the accompanying drawings.

9. A method of driving a liquid crystal display device including a plurality of column electrodes and a plurality of row electrodes in the form of a matrix, a liquid crystal display layer disposed between the column electrodes and the row electrodes, and switch elements having non-linear volt-ampere characteristics at inter-sections of the column and row electrodes between the liquid crystal display layer and either the column or

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row electrode, the method comprising applying a voltage to individual column electrodes, and applying a voltage to individual row electrodes, the row electrode voltage including an ON pulse comprising a pulse width modulated signal based upon a grey scale display indication, the column electrode voltage during a selected time being such that, in combination with an ON pulse on an intersecting row electrode, the relevant switch element triggers to charge the display layer, and during a non-selected time is insufficient to trigger the switch element, the ON pulse being present only during the selected time column electrode voltage, and the start of the pulse width modulated signal being so controlled that the ON pulse is continuous or undivided during that selected time.

10. A method according to claim 9, wherein the ON pulse continues until the end of the selected time.

11. A method according to claim 9, wherein, at the end of selected time, a discharge signal of opposite polarity to that previously applied to the respective electrode is applied to the column electrode and to the row electrode, so as to discharge electric charge stored in the liquid crystal layer during the selected time.

12. A method of driving a liquid crystal display device substantially as herein described and illustrated in Figures 7 to 10 of the accompanying drawings.

13. A method of driving a liquid crystal display device substantially as herein described and shown in Figures 7 to 10 and as modified in Figure 11 of the accompanying drawings.

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