

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS/INCORPORATION BY REFERENCE

[0001] The present application makes reference to, claims priority to, and claims the benefit of Korean Patent Application No. 10-2012-0126932, filed on Nov. 9, 2012 in the Korean Intellectual Property Office and titled “SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF”, the contents of which are hereby incorporated herein by reference, in their entirety.

FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002] [Not Applicable]

SEQUENCE LISTING

[0003] [Not Applicable]

MICROFICHE/COPYRIGHT REFERENCE

[0004] [Not Applicable]

BACKGROUND

[0005] Present systems, methods and/or architectures for forming electronic packages having interposers are inadequate. Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such approaches with the present invention as set forth in the remainder of the present application with reference to the drawings.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

[0006] The accompanying drawings are included to provide a further understanding of the present disclosure, and are incorporated in and constitute a part of this specification. The drawings illustrate exemplary embodiments of the present disclosure and, together with the description, serve to explain principles of the present disclosure. In the drawings:

[0007] FIG. 1 illustrates a cross-sectional view of a semiconductor device according to an embodiment;

[0008] FIG. 2 illustrates a cross-sectional view of a semiconductor device according to another embodiment;

[0009] FIGS. 3A to 3F illustrate cross-sectional views sequentially showing a method of manufacturing a semiconductor device according to another embodiment;

[0010] FIGS. 4A to 4D illustrate cross-sectional views of a method of manufacturing a front part of an interposer in a method of manufacturing a semiconductor device according to another embodiment;

[0011] FIGS. 5A to 5E illustrate cross-sectional views of a method of manufacturing a rear part of the interposer in the method of manufacturing the semiconductor device according to another embodiment;

[0012] FIGS. 6A to 6D illustrate cross-sectional views of a method of manufacturing a front part of an interposer in a method of manufacturing a semiconductor device according to another embodiment;

[0013] FIGS. 7A to 7E illustrate cross-sectional views of a method of manufacturing a rear part of the interposer in the method of manufacturing the semiconductor device according to another embodiment;

[0014] FIGS. 8A to 8D illustrate cross-sectional views of a method of manufacturing a front part of an interposer in a method of manufacturing a semiconductor device according to another embodiment;
and

[0015] FIGS. 9A to 9E illustrate cross-sectional views of a method of manufacturing a rear part of the interposer in the method of manufacturing the semiconductor device according to another embodiment.

DETAILED DESCRIPTION OF VARIOUS ASPECTS OF THE INVENTION

[0016] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings. However, the various aspects of the present invention may be embodied in different forms, and thus the provided exemplary embodiments should not be construed as limiting.

[0017] Various embodiments relate to a semiconductor device and a manufacturing method thereof. Generally, after a semiconductor die is mounted on an interposer, one semiconductor device in which the interposer is stacked on the other semiconductor die or substrate is called a 2.5D package. Commonly, 3D packages represent semiconductor devices in which one semiconductor die is stacked on the other semiconductor die or substrate without an interposer.

[0018] However, the above-described 2.5D package should have a plurality of through silicon vias so that electrical signals flow between an upper semiconductor die and a lower semiconductor die or substrate. Thus, in the semiconductor device according to the related art, the through silicon vias as well as circuit patterns should be formed in the interposer. As a result, manufacturing costs may be expensive, and also, the semiconductor device may be increased in thickness.

[0019] An example aspect of the present invention provides a semiconductor device including an interposer having a relatively thin thickness without a through silicon via and a method of manufacturing the same.

[0020] Another example aspect of the present invention provides a semiconductor device in which a redistribution layer having the fine pitch with a submicron unit is capable of being formed since, for example, an interposer is formed on a dummy substrate formed of silicon or glass, and which is capable of being manufactured using various materials and realized in an embedded passive structure and a method of manufacturing the same.

[0021] According to at least one of embodiments, a method of manufacturing a semiconductor device includes: forming an interposer including a redistribution layer and a dielectric layer on a dummy substrate; connecting a semiconductor die to the redistribution layer facing an upper portion of the interposer; encapsulating the semiconductor die by using an encapsulation; removing the dummy

substrate from the interposer; and connecting a bump to the redistribution layer facing a lower portion of the interposer.

[0022] The dummy substrate may, for example, include a silicon or glass. The dielectric layer may, for example, include a silicon oxide layer, a silicon nitride layer, or a polymer layer. A solder may, for example, be formed on the redistribution layer facing the upper portion of the interposer, and the semiconductor die may be connected to the solder.

[0023] After the connection of the semiconductor die, an underfill may, for example, be filled between the semiconductor die and the interposer. After the encapsulating of the semiconductor die, the encapsulant may, for example, be ground to expose a top surface of the semiconductor die. The removing of the dummy substrate may, for example, include grinding and etching the dummy substrate to expose the redistribution layer facing the lower portion of the interposer.

[0024] The connection of the bump may, for example, include: forming an under bump metal on the redistribution layer facing the lower portion of the interposer; and connecting the bump to the under bump metal. The forming of the interposer may, for example, include previously forming an under bump metal on the redistribution layer facing the lower portion of the interposer.

[0025] After the connection of the bump, the bump may, for example, be mounted on a circuit board. An underfill may, for example, be filled between the interposer and the circuit board. A cover may, for example, be attached to the circuit board to cover the semiconductor die.

[0026] The forming of the interposer may, for example, include: forming a seed layer on the dummy substrate; forming and patterning the redistribution layer on the seed layer; forming the dielectric layer outside the redistribution layer; grinding and removing the dummy substrate; and removing the seed layer.

[0027] The forming of the interposer may, for example, include: forming a seed layer on the dummy substrate; forming an under bump metal on the seed layer; forming and patterning the redistribution layer on the under bump metal; forming the dielectric layer outside the redistribution layer; grinding and removing the dummy substrate; and removing the seed layer. The patterning of the under bump metal may, for example, include removing the seed layer formed outside the under bump metal.

[0028] According to another embodiment, a semiconductor device includes: an interposer including a redistribution layer and a dielectric layer; a semiconductor die connected to the redistribution layer facing an upper portion of the interposer; encapsulant encapsulating the semiconductor die; and a bump connected to the redistribution layer facing a lower portion of the interposer.

[0029] The dielectric layer may, for example, include a silicon oxide layer, a silicon nitride layer, or a polymer layer. A solder may, for example, be formed on the redistribution layer facing the upper portion of the interposer, and the semiconductor die may be connected to the solder. An underfill may, for example, be filled between the semiconductor die and the interposer. A top surface of the semiconductor die may, for example, be exposed through the encapsulant.

[0030] An under bump metal may, for example, be disposed between the redistribution layer facing the lower portion of the interposer and the bump. The under bump metal may, for example, be disposed inside the interposer. The bump may, for example, be mounted on a circuit board. An underfill may, for example, be filled between the interposer and the circuit board. A cover may, for example, be attached to the circuit board to cover the semiconductor die.

[0031] Various example embodiments will now be described more fully hereinafter with reference to the accompanying drawings.

[0032] Embodiments may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art.

[0033] In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. As used herein, the term and/or includes any and all combinations of one or more of the associated listed items.

[0034] In the following description, the technical terms are used only for explaining a specific exemplary embodiment while not limiting the present disclosure. The terms of a singular form may include plural forms unless referred to the contrary. The meaning of “include,” “comprise,” “including,” or “comprising,” specifies a property, a region, a fixed number, a step, a process, an

element and/or a component but does not exclude other properties, regions, fixed numbers, steps, processes, elements and/or components.

[0035] Also, though terms like a first and a second are used to describe various members, components, regions, layers, and/or portions in various embodiments of the present invention, the members, components, regions, layers, and/or portions are not limited to these terms. These terms are used only to differentiate one member, component, region, layer, or portion from another one. Therefore, a member, a component, a region, a layer, or a portion referred to as a first member, a first component, a first region, a first layer, or a first portion in an embodiment can be referred to as a second member, a second component, a second region, a second layer, or a second portion in another embodiment.

[0036] Also, the terms “semiconductor die” used in this specification may, for example, include a semiconductor chip having an active circuit or a passive circuit, a semiconductor wafer, or its equivalent. Also, in this specification, a dummy substrate may, for example, include silicon, glass, or its equivalent. Also, in this specification, a dielectric layer may, for example, include silicon, glass, or its equivalent.

[0037] FIG. 1 illustrates a cross-sectional view of a semiconductor device according to an embodiment.

[0038] Referring to FIG. 1, a semiconductor device 100 according to an embodiment includes an interposer 110, a semiconductor die 120, an underfill 130, an encapsulant 140, and a bump 150.

[0039] The interposer 110 includes a redistribution layer 111 and a dielectric layer 112. For example, the interposer 110 may include a redistribution layer 111 having a multi-layered structure, and the redistribution layer 111 may be protected by the dielectric layer 112. The redistribution layer 111 disposed on each of bottom and top surfaces is directly exposed through the dielectric layer 112. Also, the redistribution layer 111 disposed on each of the bottom and top surface of the dielectric layer 112 may, for example, have a relatively large width so that the bump is easily formed later. As described above, the portion of the redistribution layer 111 having the relatively large width may, for example, be defined as a pad or land.

[0040] Here, the redistribution layer 111 may, for example, be formed of one selected from copper, aluminum, and their equivalents. Also, the dielectric layer 112 may, for example, be formed of one selected from a silicon oxide layer, a silicon nitride layer, a polymer layer, and their equivalents. However, the present disclosure is not limited to these materials. As an example, when the silicon oxide layer or the silicon nitride layer is used as the dielectric layer 112, the redistribution layer 111 may, for example, have a fine pitch with a submicron unit. In some cases, a passive device may be embedded. This may, for example, be done because the redistribution layer 111 and the dielectric layer 112 may be patterned by using a line width embodied in a semiconductor fabrication (FAB) process when the dielectric layer 112 includes the silicon oxide layer or the silicon nitride layer. As previously known, the line width embodied in a package process may be significantly greater than that embodiment in the semiconductor FAB process. Furthermore, since the interposer 110 might not need through silicon vias, unlike a related art, the interposer 110 may have a thin thickness and be manufactured with low costs.

[0041] The semiconductor die 120 may, for example, include a common memory, a graphics processing unit (GPU), a central processing unit (CPU), or its equivalent. However, the present disclosure is not limited to these kinds. The semiconductor die 120 includes a connection terminal 121 electrically connectable to the interposer 110. As illustrated, the connection terminal 121 may, for example, include a copper pillar 121a and a solder cap 121b disposed on an end of the copper pillar 121a. The connection terminal 121 may, for example, include a common solder bump. Also, a solder 122 may be previously disposed between the connection terminal 121 and the interposer 110, i.e., on a top surface of the redistribution layer 111 facing an upper portion of the interposer 110 to easily connect the interposer 110 to the connection terminal 121. As a result, the semiconductor die 120 may be electrically connected to the redistribution layer 111 facing the upper portion of the interposer 110.

[0042] The underfill 130 is filled between the interposer 110 and the semiconductor die 120. More particularly, the underfill 130 may be disposed between the interposer 110 and the semiconductor die 120 and also surround a side surface of a lower portion of the semiconductor die 120. The underfill 130 may, for example, improve physical/mechanical coupling between the interposer 110 and the semiconductor die 120. In addition, the underfill 130 may prevent the interposer 110 and the

semiconductor die 120 from being separated from each other by a stress due to, for example, a difference in the respective coefficients of thermal expansion between the interposer 110 and the semiconductor die 120.

[0043] The encapsulant 140 surrounds the semiconductor die 120 disposed above the interposer 110 to protect the semiconductor die against external environments. More particularly, the encapsulant 140 surrounds surfaces of the semiconductor die 120 and the underfill 130. However, a top surface of the semiconductor die 120 may be exposed to the outside from the encapsulant 140 to improve heat dissipation performance of the semiconductor die 120.

[0044] Here, a side surface of the encapsulant 140 may be flush with a side surface of the interposer 110. Also, a top surface of the encapsulant 140 may be flush with the top surface of the semiconductor die 120. As a result, the semiconductor device 100 according to the current embodiment may have a compact structure.

[0045] The bump 150 is connected to the redistribution layer 111 facing a lower portion of the interposer 110. More particularly, a bump metal 113 is disposed on the redistribution layer 111 exposed through a bottom surface of the interposer 110, and then the bump 150 is connected to the bump metal 113. The bump 150 may, for example, have a relatively small size when compared to that of a common solder ball. Thus, the bump 150 may be defined as a micro bump. For example, the bump 150 may have a diameter of about 100 μm or less. However, the present disclosure is not limited to this diameter. In some cases, the diameter of the bump 150 may be larger than that of the above-mentioned. On the other hand, a solder ball that will be described below may have a diameter of about 200 μm to about 400 μm .

[0046] Therefore, the semiconductor device 100 according to the current embodiment may be, for example, manufactured in a flip chip shape. Thus, the semiconductor device 100 having the flip chip shape may, for example, be mounted on a circuit board for common semiconductor device or semiconductor package. Alternatively, the semiconductor device 100 according to the current embodiment may be mounted on a mother board or a main board.

[0047] Therefore, the current embodiment may, for example, provide the semiconductor device 100 (flip chip device) having the interposer 110 having a relatively thin thickness without through silicon

vias. Also, since, for example, the current embodiment uses the silicon oxide layer or the silicon nitride layer, which are formed of a nonorganic material, the redistribution layer 111 having the fine pitch with the submicron unit may be provided. Also, the current embodiment may, for example, provide the semiconductor device 100 including the interposer 110 which may be realized in an embedded passive structure.

[0048] FIG. 2 illustrates a cross-sectional view of a semiconductor device according to another embodiment.

[0049] Referring to FIG. 2, a semiconductor device 200 according to another embodiment includes the above-described device 100 (hereinafter, referred to as a flip chip device), a circuit board 210, an underfill 220, a cover 230, a thermal conductive adhesive 240, and a solder ball 250.

[0050] As described above, the flip chip device 100 has the bottom surface on which the bump 150 is disposed. The bump 150 is mounted on the circuit board 210.

[0051] The circuit board 210 includes a circuit pattern 211 and an insulation layer 212. Furthermore, a passive device 260 may, for example, be mounted on the circuit board 210. Also, as described above, the bump 150 of the flip chip device 100 is electrically connected to the circuit pattern 211 of the circuit board 210.

[0052] The underfill 220 is filled between the interposer 100 and the circuit board 210. That is, the underfill 220 surrounds the bump 150 as well as side surfaces of the interposer 110 of the flip chip device 100 and the encapsulant 140. Thus, it may prevent the flip chip device 100 and the circuit board 210 from being separated from each other by a stress due to a difference in respective coefficients of thermal expansion between the flip chip device 100 and the circuit board 210.

[0053] The cover 230 may be attached to the circuit board 210 and also approximately surround the flip chip device 100. Thus, the flip chip device 100 may be protected against external environments by the cover 230. The cover may, for example, be formed of a metal, ceramic, or its equivalent to improve heat dissipation performance, but the present disclosure is not limited thereto.

[0054] The thermal conductive adhesive 240 is disposed between the flip chip device 100 and the cover 230 and between the cover 230 and the circuit board 210. The thermal conductive adhesive 240 may quickly transfer heat generated from the flip chip device 100 into the cover 230. Also, the

thermal conductive adhesive 240 may fix the cover 230 to the flip chip device 100 and the circuit board 210.

[0055] The solder ball 250 is connected to a bottom surface of the circuit board 210. That is, the solder ball 250 is electrically connected to the circuit pattern 211 of the circuit board 210. Due to the solder ball 250, the semiconductor device 200 according to the current embodiment may, for example, be mounted on a mother board or main board of electronic equipment such as a computer, a smart phone, and the like.

[0056] Therefore, the current embodiment may, for example, provide a 2.5D semiconductor device including the semiconductor device 100 (flip chip device) having the interposer 110 having a relatively thin thickness without through silicon vias. Also, since, for example, the current embodiment uses a silicon oxide layer or a silicon nitride layer which are formed of a nonorganic material, a redistribution layer 111 having a fine pitch with a submicron unit may be provided. Also, the current embodiment may provide the semiconductor device 200 including the semiconductor device 100 including the interposer 110 which may be realized in an embedded passive structure.

[0057] FIGS. 3A to 3F illustrate cross-sectional views sequentially showing a method of manufacturing a semiconductor device according to another embodiment.

[0058] Referring to FIGS. 3A to 3F, a method of manufacturing a semiconductor device 100 according to an embodiment includes forming an interposer 110 on a dummy substrate 310, connecting a semiconductor die 120 to the interposer 110, encapsulating the semiconductor die 120 by using an encapsulant 140, grinding the encapsulant 140, grinding the dummy substrate 310, and connecting a bump 150. This will now be described in detail.

[0059] As shown in FIGS. 3A and 3B, in the forming of the interposer 110 on the dummy substrate 310, the interposer 110 is directly formed on the dummy substrate 310. That is, the interposer 110 including a redistribution layer 111 and a dielectric layer 112 is directly formed on the dummy substrate 310. As described above, the redistribution layer 111 may, for example, have a multi-layered structure. The redistribution layer 111 (which may be defined as a pad or land) having a relatively large width may be formed on each of top and bottom surfaces of the dielectric layer 112. Here, the redistribution layer 111 may, for example, be formed of one selected from copper,

aluminum, and their equivalents. Also, the dielectric layer 112 may, for example, be formed of one selected from a silicon oxide layer, a silicon nitride layer, a polymer layer, and their equivalents. However, the present disclosure is not limited to these materials. Furthermore, a solder 122 may, for example, be previously formed on the redistribution layer 111 (a pad or land) formed on a top surface of the dielectric layer 112 to easily electrically connect the semiconductor die 120 thereto later. Here, the dummy substrate 310 may, for example, be formed of one of silicon, glass, and their equivalents. However, the present disclosure is not limited to a kind of dummy substrate 310. As described above, since, for example, a silicon oxide layer or a silicon nitride layer that is formed of a nonorganic material is used as the dummy substrate 310, the redistribution layer 111 having a fine pitch and fine width may be formed.

[0060] As shown in FIG. 3C, in the connecting of the semiconductor die 120 to the interposer 110, the semiconductor die 120 is electrically connected to the interposer 110. That is, a connection terminal 121 (a copper pillar 121a and a solder cap 121b) of the semiconductor die 120 is electrically connected to the solder 122 which is previously formed on the interposer 110. Furthermore, an underfill 130 is filled between the interposer 110 and the semiconductor die 120. The underfill 130 covers a lower region of a side surface of the semiconductor die 120.

[0061] As shown in FIG. 3D, in the encapsulating of the semiconductor die 120 by using the encapsulant 140, the semiconductor die 120 is encapsulated on the interposer 110 by using the encapsulant 140. That is, surfaces of the underfill 130 and the semiconductor die 120 which are formed on the interposer 110 may be surrounded by the encapsulant 140.

[0062] As shown in FIG. 3E, in the grinding of the encapsulant 140, the encapsulant 140 formed on the semiconductor die 120 is ground and removed by a predetermined thickness. For example, the encapsulant 140 may be ground and removed until a top surface of the semiconductor die 120 is exposed to the outside.

[0063] As shown in FIG. 3F, in the grinding of the dummy substrate 310, the dummy substrate 310 disposed under the interposer 110 is ground and/or etched, and thus removed. Thus, the redistribution layer 111 (the pad or land) is exposed to the outside through a lower portion of the interposer 110.

[0064] Although not shown, an under bump metal 113 may be formed on the redistribution layer 111 exposed through the lower portion of the interposer 110 as described above, and the bump 150 may be connected to the under bump metal 113. (see FIG. 1)

[0065] Furthermore, in the formed semiconductor device 100, i.e., the flip chip device 100, the bump 150 may be mounted on the circuit board 210. Also, an underfill 220 may, for example, be formed between the flip chip device 100 and the circuit board 210. Furthermore, a cover 230 may, for example, be attached to the flip chip device 100 and the circuit board 210 through a thermal conductive adhesive 240. Also, the solder ball 250 may be connected to a bottom surface of the circuit board 210, which may, for example, form the 2.5D package device 200. (see FIG. 2)

[0066] Therefore, the current embodiment may, for example, provide the method of manufacturing the semiconductor device 100 having the interposer 110 having a relatively thin thickness without through silicon vias and the semiconductor device 200 including the semiconductor device 100. Also, since, for example, the interposer 110 is formed on the dummy substrate 310 formed of silicon or glass, the redistribution layer 111 having a fine pitch with a submicron unit may be formed. In addition, the current embodiment may provide the method of manufacturing the semiconductor device 100 including the interposer 110 which may, for example, be formed using various materials and realized in an embedded passive structure and the semiconductor device 200 including the semiconductor device 100.

[0067] FIGS. 4A to 4D illustrate cross-sectional views of a method of manufacturing a front part of an interposer 110 in a method of manufacturing a semiconductor device 100 according to another embodiment. FIGS. 5A to 5E illustrate cross-sectional views of a method of manufacturing a rear part of the interposer 110 in the method of manufacturing the semiconductor device 100 according to another embodiment.

[0068] As shown in FIGS. 4A to 4D and 5A to 5E, the method of forming the interposer 110 includes forming a seed layer 311 on a dummy substrate 310, patterning a redistribution layer 111, etching the seed layer 311, forming a dielectric layer 112, removing the dummy substrate 310, and removing the seed layer 311. This will now be described in detail.

[0069] As shown in FIG. 4A, in the forming of the seed layer 311 on the dummy substrate 310, a titanium layer 311a/copper layer 311b or a titanium/tungsten layer 311a/copper layer 311b may, for example, be formed on an entire top surface of the dummy substrate 310 to provide the seed layer 311 that will be used for plating the redistribution layer 111 later.

[0070] As shown in FIG. 4B, in the patterning of the redistribution layer 111, the redistribution layer 111 is patterned and formed on the seed layer 311. That is, after a copper layer or an aluminum layer is plated on an entire top surface of the seed layer 311, a photolithography process is performed to form the redistribution layer 111 having a predetermined pattern. Here, the seed layer 311 formed outside the redistribution layer 111 is not removed yet.

[0071] As shown in FIG. 4C, in the etching of the seed layer 311, for example, the copper layer 311b of the seed layer 311 formed outside the redistribution layer 111 is etched and removed. That is, the titanium layer or the titanium/tungsten layer 311a remains still.

[0072] As shown in FIG. 4D, in the forming of the dielectric layer 112, the dielectric layer 112 is formed around the redistribution layer 111. Furthermore, the forming of the redistribution layer 111 and the dielectric layer 112 may be performed several times. That is, the redistribution layer 111 and the dielectric layer 112 may build up on the dummy substrate 310 several times. On the other hand, since, for example, the redistribution layer 111 and the dielectric layer 112 alternately build up, the required redistribution layer 111 may be formed. Thus, the interposer 110 may have a small size and thin thickness. In addition, a passive structure may be embedded in the interposer 110.

[0073] Here, the redistribution layer 111 formed on each of the uppermost and lowermost portions of the dielectric layer 112 may, for example, have a relatively wide width (pad or land).

[0074] As shown in FIGS. 5A to 5C, in the removing of the dummy substrate 310, the dummy substrate 310 on which the interposer 110 is mounted is removed. That is, as shown in FIGS. 5A and 5B, a portion of the dummy substrate 310 having a relatively thick thickness is removed by the grinding process, and then, a remaining portion having a relatively thin thickness is removed by the etching process. As a result, as shown in FIGS. 5C, the titanium layer or the titanium/tungsten layer 311a of the seed layer 311 is exposed to the outside.

[0075] As shown in FIG. 5D, in the removing of the seed layer 311, the seed layer 311 remaining on the interposer 110, i.e., the titanium layer or the titanium/tungsten layer 311a is removed. Thus, the redistribution layer 111 having a relatively wide width in the interposer 110 is exposed to the outside through the dielectric layer 112.

[0076] Furthermore, as shown in FIG. 5E, after the seed layer 311 is removed, an under bump metal 113 may be formed on the redistribution layer 111 exposed through the dielectric layer 112, and then, a bump 150 may be connected to the under bump metal 113. Thus, the under bump metal 113 protrudes from the dielectric layer 112, and the bump 150 approximately surrounds the under bump metal 113.

[0077] FIGS. 6A to 6D illustrate cross-sectional views of a method of manufacturing a front part of an interposer 110 in a method of manufacturing a semiconductor device 100 according to another embodiment. FIGS. 7A to 7E illustrate cross-sectional views of a method of manufacturing a rear part of the interposer 110 in the method of manufacturing the semiconductor device 100 according to another embodiment.

[0078] As shown in FIGS. 6A to 6D and 7A to 7E, the method of forming the interposer 110 includes forming a seed layer 311 on a dummy substrate 310, forming an under bump metal 113 on the seed layer 311, etching the seed layer 311, forming a redistribution layer 111, forming a dielectric layer 112, removing the dummy substrate 310, and removing the seed layer 311. This will now be described in detail.

[0079] As shown in FIG. 6A, in the forming of the seed layer 311 on the dummy substrate 310, a titanium layer 311a/copper layer 311b or a titanium-tungsten layer 311a/copper layer 311b may, for example, be formed on an entire top surface of the dummy substrate 310 to provide the seed layer 311.

[0080] As shown in FIG. 6B, in the forming of the under bump metal 113 on the seed layer 311, for example, a gold layer 113a, a nickel layer 113b, and a copper layer or an aluminum layer 113c are sequentially formed on the seed layer 311 to form the under bump metal 113.

[0081] As shown in FIG. 6C, in the etching of the seed layer 311, for example, the copper layer of the seed layer 311 remaining outside the under bump metal 113 is etched and removed. That is, the titanium layer or the titanium-tungsten layer 311a remains still.

[0082] As shown in FIG. 6D, in the forming of the redistribution layer 111 and the forming of the dielectric layer 112, the redistribution layer 111 is patterned on the under bump metal 113, and also the dielectric layer 112 is formed therearound. That is, after a copper layer or an aluminum layer is plated on the under bump metal 113, a photolithography process is performed to form the redistribution layer 111 having a predetermined pattern. Also, the dielectric layer 112 is formed around the redistribution layer 111. Furthermore, the forming of the redistribution layer 111 and the dielectric layer 112 may be performed several times. That is, the above-described build up process may be performed.

[0083] Here, the redistribution layer 111 formed on the uppermost surface of the interposer 110 and having a relatively wide width may, for example, be defined as a pad or land.

[0084] As shown in FIGS. 7A to 7C, in the removing of the dummy substrate 310, the dummy substrate 310 on which the interposer 110 is mounted is removed. That is, as shown in FIGS. 7A and 7B, a portion of the dummy substrate 310 having a relatively thick thickness is removed by the grinding process, and then, a remaining portion having a relatively thin thickness is removed by the etching process. As a result, as shown in FIGS. 7C, the titanium layer or the titanium/tungsten layer 311a of the seed layer 311 is exposed to the outside.

[0085] As shown in FIG. 7D, in the removing of the seed layer 311, the seed layer 311 remaining on the interposer 110, i.e., the titanium layer or the titanium/tungsten layer 311a is removed. Thus, the under bump metal 113 is exposed to the outside through the dielectric layer 112. That is, bottom and side surfaces of the under bump metal 113 are disposed within the dielectric layer 112. Also, only a top surface of the under bump metal 113 is exposed to the outside through the dielectric layer 112. That is to say, the exposed surface of the under bump metal 113 is flush with the exposed surface of the dielectric layer 112.

[0086] Furthermore, as shown in FIG. 7E, after the seed layer 311 is removed, a bump 150 is connected to the under bump metal 113 exposed through the dielectric layer 112. That is, since, for example, the under bump metal 113 is previously formed in the forming of the interposer 110, it may be unnecessary to form the under bump metal 113 through a separate process for connecting the bump

150 later. Alternatively, due to these process characteristics, the under bump metal 113 is not disposed inside the bump 150.

[0087] FIGS. 8A to 8D illustrate cross-sectional views of a method of manufacturing a front part of an interposer 110 in a method of manufacturing a semiconductor device 100 according to another embodiment. FIGS. 9A to 9E illustrate cross-sectional views of a method of manufacturing a rear part of the interposer 110 in the method of manufacturing the semiconductor device 100 according to another embodiment.

[0088] As shown in FIGS. 8A to 8D and 9A to 9E, the method of manufacturing the interposer 110 according to the current embodiment is similar to that according to the foregoing embodiments. However, as shown in FIG. 8C, the method of manufacturing the interposer 110 according to the current embodiment is different from that according to the foregoing embodiments in that a seed layer 311 formed outside an under bump metal 113 is completely removed in etching of the seed layer 311. That is, as shown in FIG. 8C, the seed layer 311 does not remain outside the under bump metal 113. Also, as shown in FIGS. 9C and 9D, it may be that the seed layer 311 formed on the under bump metal 113 is removed before a solder is connected to a bump. Thus, an exposed surface of the under bump metal 113 is not flush with an exposed surface of a dielectric layer 112. That is, the exposed surface of the under bump metal 113 is disposed at a position lower than that of the exposed surface of the dielectric layer 112. Thus, a side portion of the bump 150 contacts the dielectric layer 112.

[0089] Embodiments provide the semiconductor device including the interposer having a relatively thin thickness without through silicon vias and the method of manufacturing the same.

[0090] Also, since, for example, the interposer is formed on the dummy substrate formed of silicon or glass, for example, the redistribution layer having the fine pitch with a submicron unit may be formed. In addition, the embodiments may provide the method of manufacturing the semiconductor device including the interposer which may be formed using various materials and realized in the embedded passive structure and the semiconductor device including the same.

[0091] Exemplary embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that

various changes in form and details may be made without departing from the spirit and scope of the present disclosure as set forth in the following claims.

What is claimed is

1. A method of manufacturing a semiconductor device, the method comprising:
forming an interposer comprising a redistribution layer and a dielectric layer on a dummy substrate;
connecting a semiconductor die to the redistribution layer facing an upper portion of the interposer;
encapsulating the semiconductor die by using an encapsulation; and
removing the dummy substrate from the interposer.
2. The method as claimed in claim 1, wherein the dummy substrate comprises at least one of: silicon and/or glass.
3. The method as claimed in claim 1, wherein the dielectric layer comprises at least one of: a silicon oxide layer, a silicon nitride layer, and/or a polymer layer.
4. The method as claimed in claim 1, comprising forming a solder on the redistribution layer facing the upper portion of the interposer, and wherein said connecting a semiconductor die comprises connecting the semiconductor die to the solder.
5. The method as claimed in claim 1, comprising, after said connecting the semiconductor die, filling an underfill between the semiconductor die and the interposer.
6. The method as claimed in claim 1, comprising, after said encapsulating the semiconductor die, grinding the encapsulant to expose a top surface of the semiconductor die.

7. The method as claimed in claim 1, wherein said removing the dummy substrate comprises grinding and etching the dummy substrate to expose a portion of the redistribution layer facing a lower portion of the interposer.

8. The method as claimed in claim 1, comprising connecting a bump to the redistribution layer facing a lower portion of the interposer, said connecting a bump comprising: forming an under bump metal on the redistribution layer facing the lower portion of the interposer; and connecting the bump to the under bump metal.

9. The method as claimed in claim 1, wherein said forming the interposer comprises forming an under bump metal on which at least a portion of the redistribution layer will be formed.

10. The method as claimed in claim 8, comprising mounting the connected bump to a circuit board.

11. The method as claimed in claim 10, comprising filling an underfill between the interposer and the circuit board.

12. The method as claimed in claim 10, comprising attaching a cover to the circuit board to cover the semiconductor die.

13. The method as claimed in claim 1, wherein said forming the interposer comprises:
forming a seed layer on the dummy substrate;
forming and patterning the redistribution layer on the seed layer;
forming the dielectric layer outside the redistribution layer; and
removing the seed layer.

14. The method as claimed in claim 1, wherein the forming of the interposer comprises:
forming a seed layer on the dummy substrate;
forming an under bump metal on the seed layer;
forming and patterning the redistribution layer on the under bump metal;
forming the dielectric layer outside the redistribution layer; and
removing the seed layer.

15. The method as claimed in claim 14, wherein said forming an under bump metal comprises removing the seed layer formed outside the under bump metal.

16. A method of manufacturing a semiconductor device, the method comprising:
forming an interposer comprising a redistribution layer and a dielectric layer on a dummy substrate; and
removing the dummy substrate from the interposer.

17. The method as claimed in claim 16, wherein said removing the dummy substrate comprises grinding and etching the dummy substrate to expose a portion of the redistribution layer.

18. The method as claimed in claim 16, wherein said forming the interposer comprises forming an under bump metal on which at least a portion of the redistribution layer will be formed.

19. A semiconductor device comprising:
an interposer comprising a redistribution layer and a dielectric layer;
a semiconductor die connected to the redistribution layer facing an upper portion of the interposer;

encapsulant encapsulating the semiconductor die; and
a bump connected to the redistribution layer facing a lower portion of the interposer.

20. The semiconductor device as claimed in claim 19, wherein under bump metal is disposed inside the interposer.