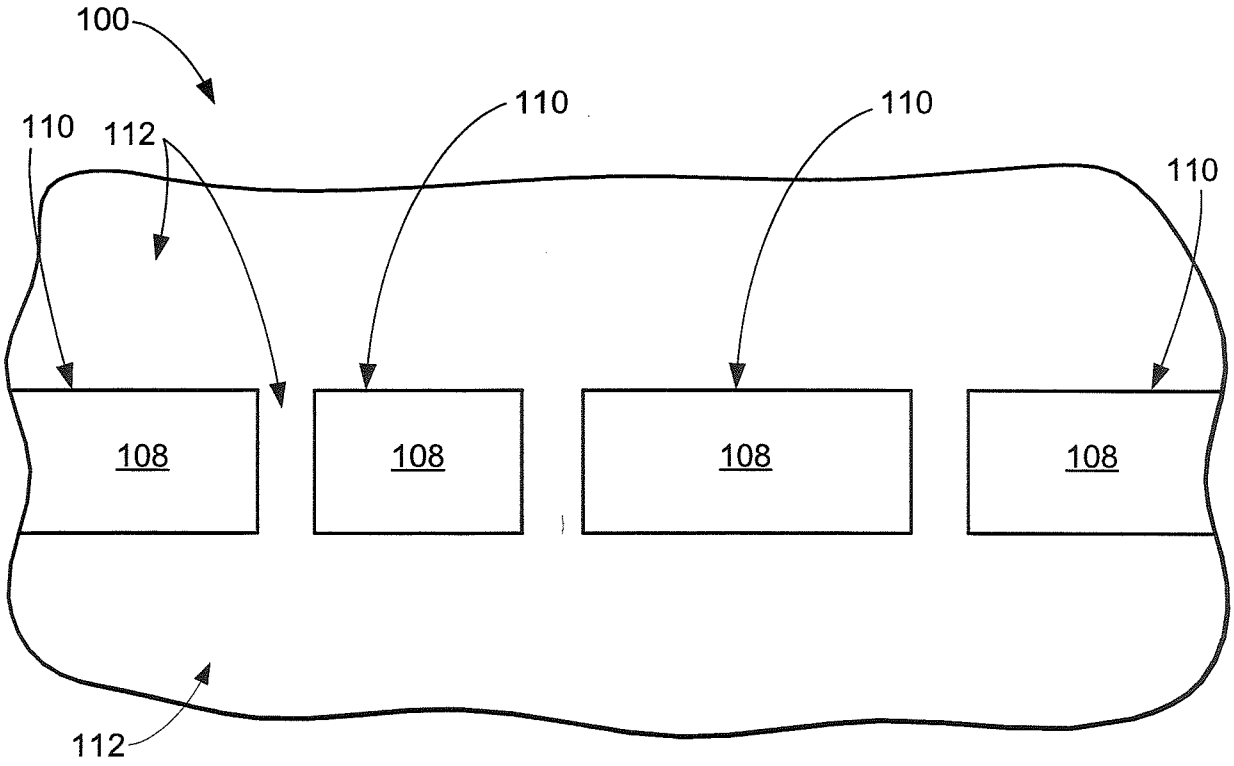

100
110
112
110
110
110
108
108
108
108
112

FIG. 1B

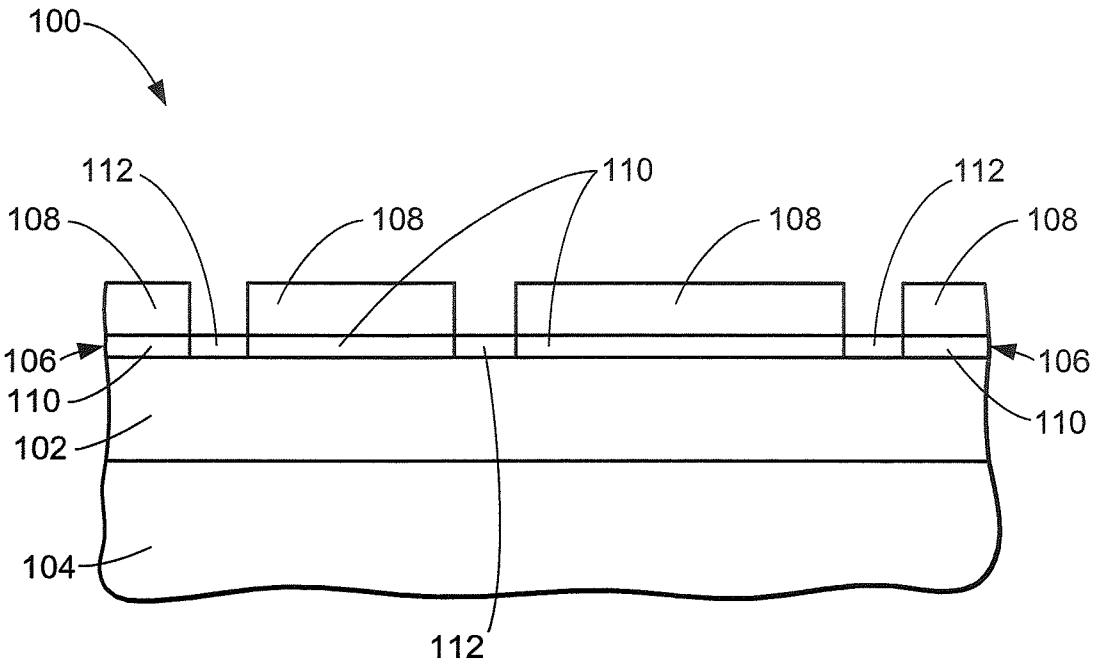

100
112
110
112
108
108
108
108
106
106
110
110
102
104
112

FIG. 1A

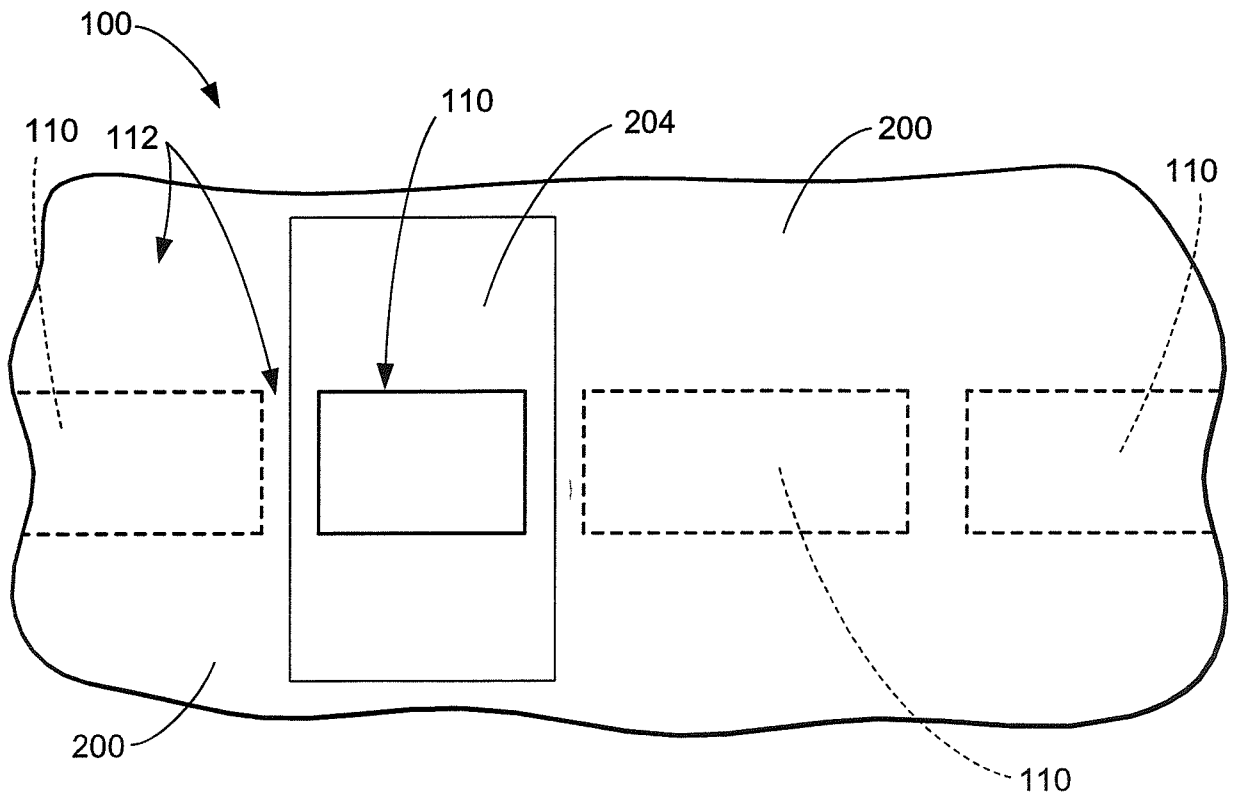

100
110
110
112
204
200
110
200
110

FIG. 2B

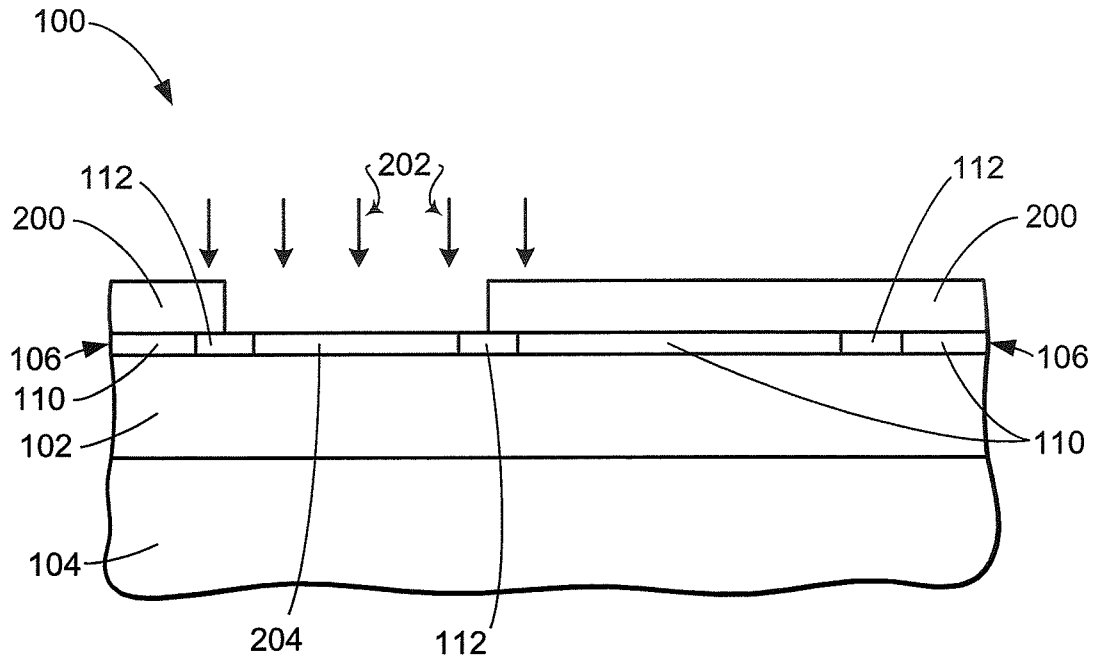

100
112
202
112
200
200
106
106
110
110
102
104
204
112

FIG. 2A

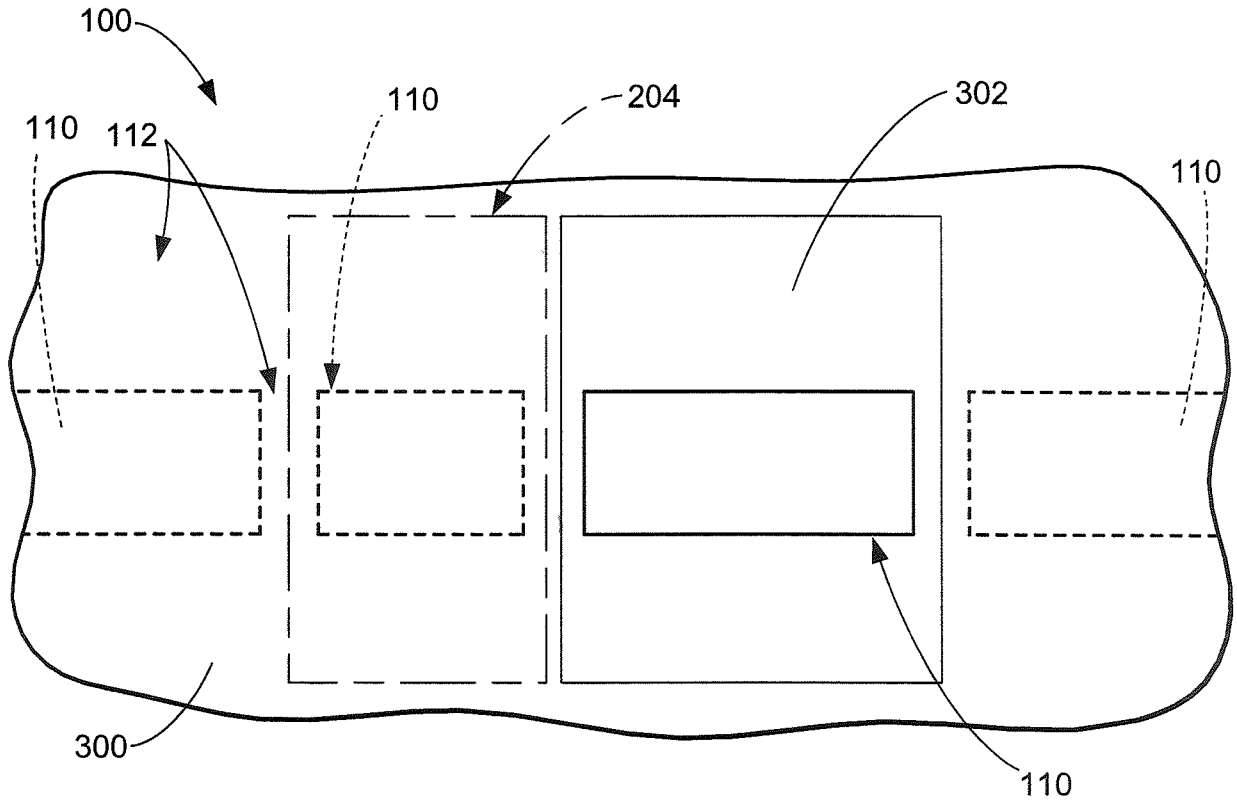

100
110
112
110
204
302
110
300
110

FIG. 3B

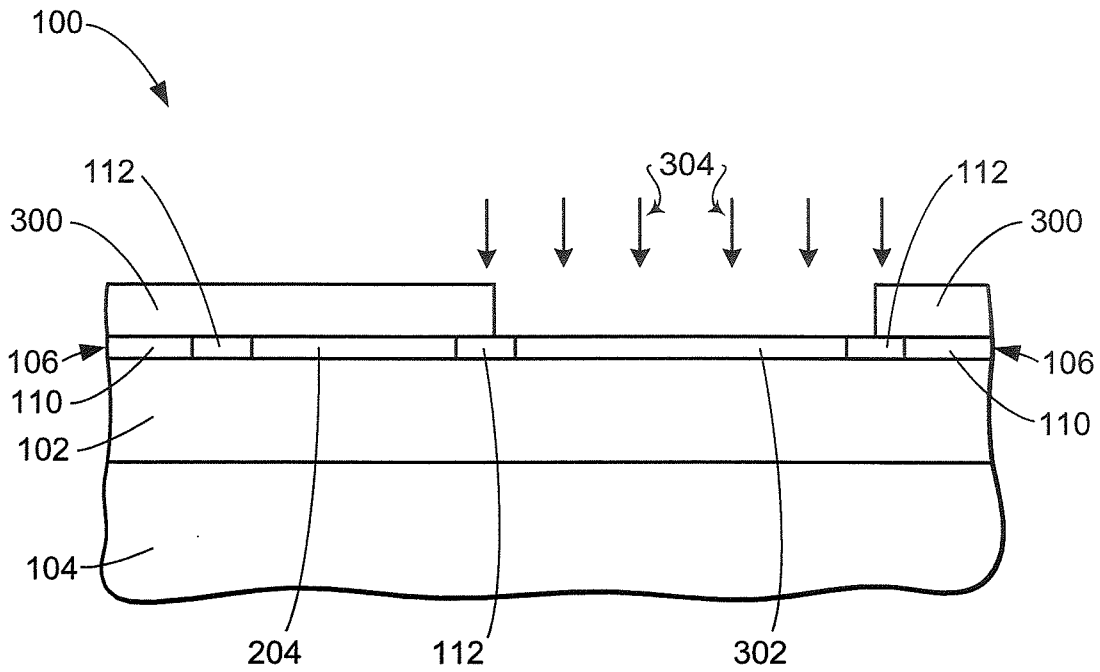

100
112
304
112
300
300
106
110
102
106
110
104
204
112
302

FIG. 3A

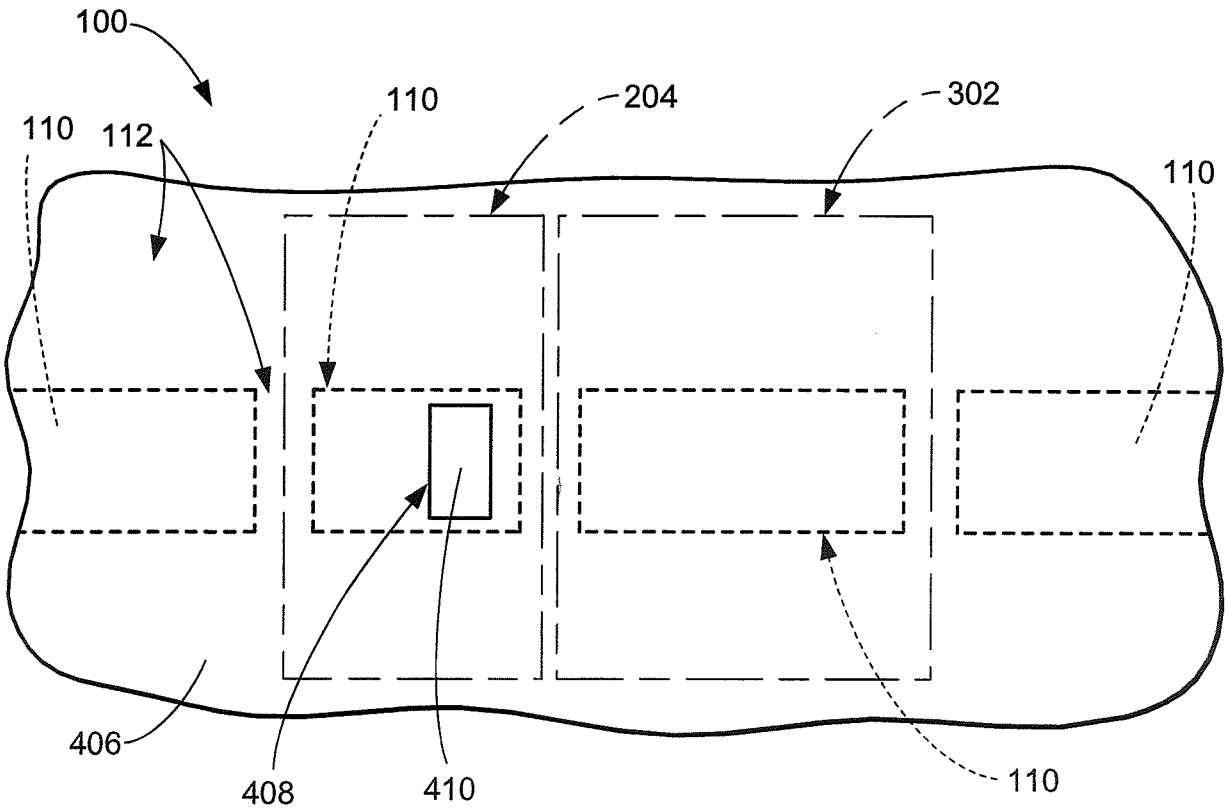

100
110
112
110
204
302
110
406
408
410
110

FIG. 4B

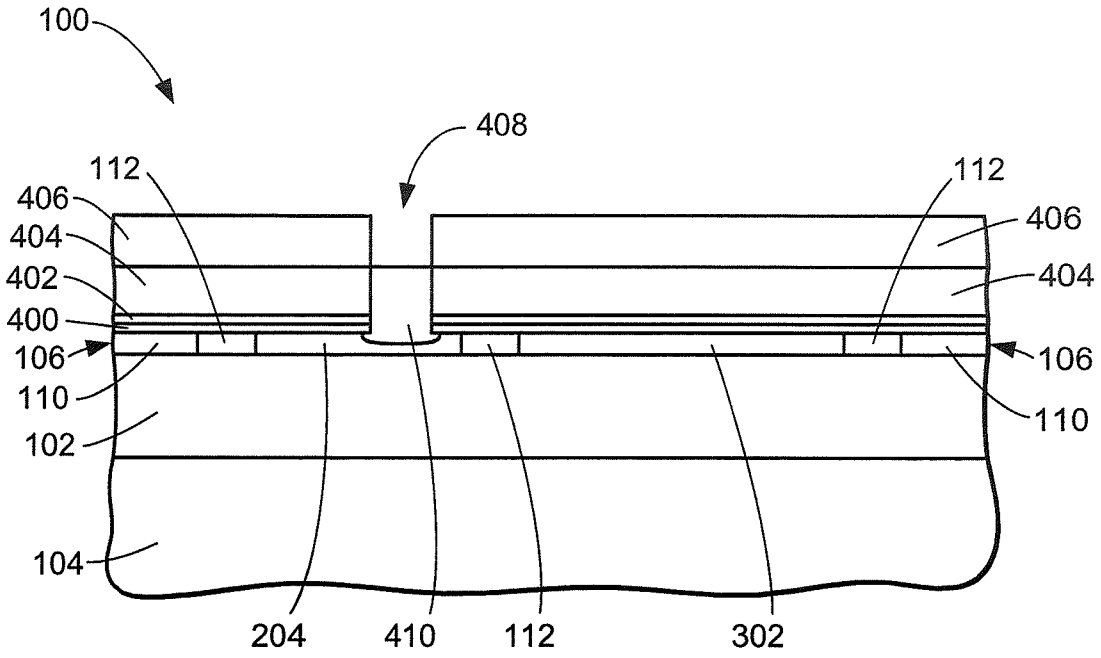

100
408
112
112
406
404
402
400
106
110
102
104
406
404
106
110
204
410
112
302

FIG. 4A

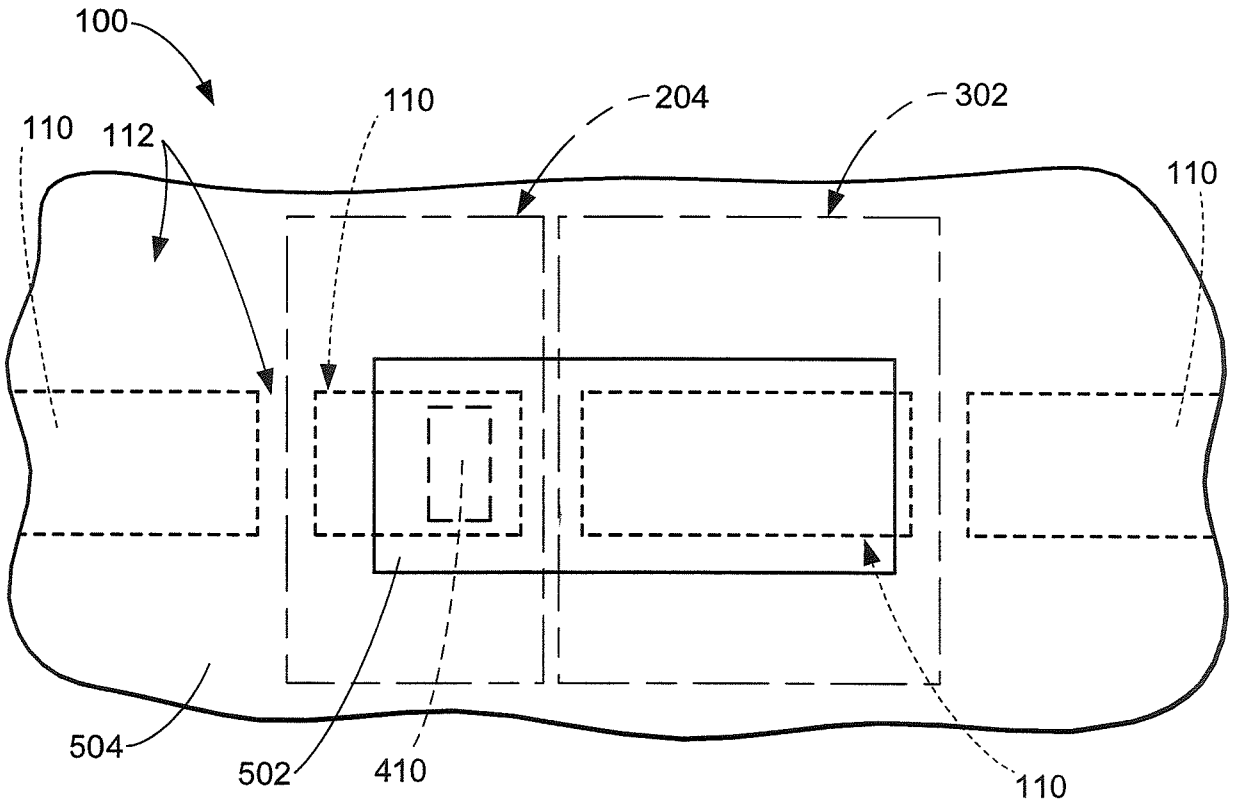

100
110
112
110
204
302
110
504
502
410
110

FIG. 5B

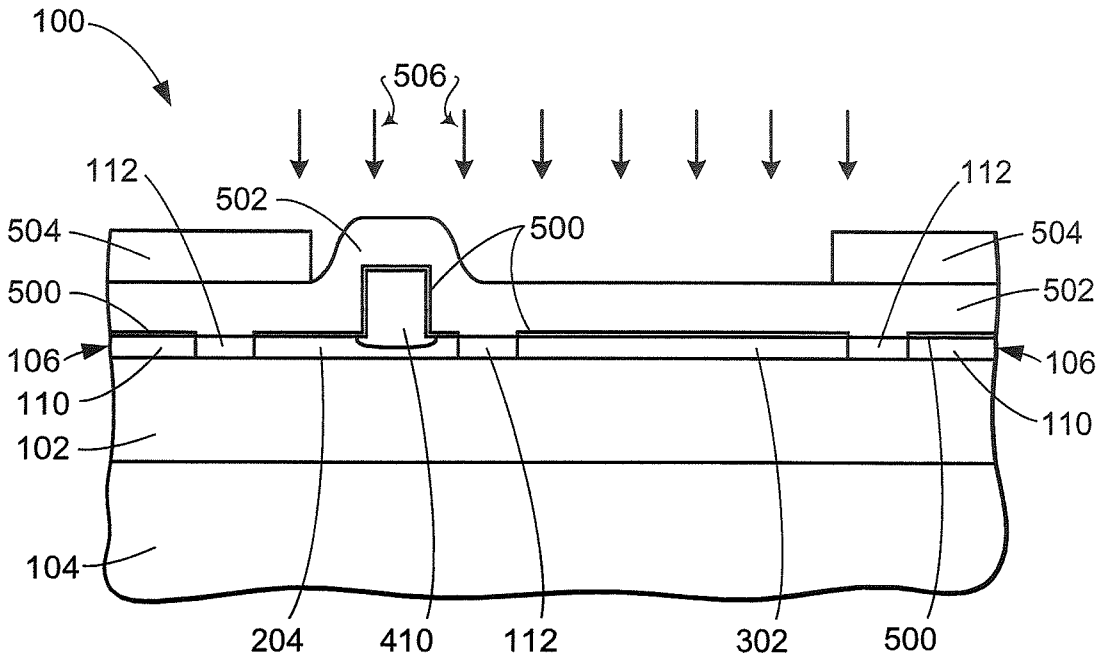

100
506
112
502
504
500
106
110
102
104
112
504
502
106
110
204
410
112
302
500

FIG. 5A

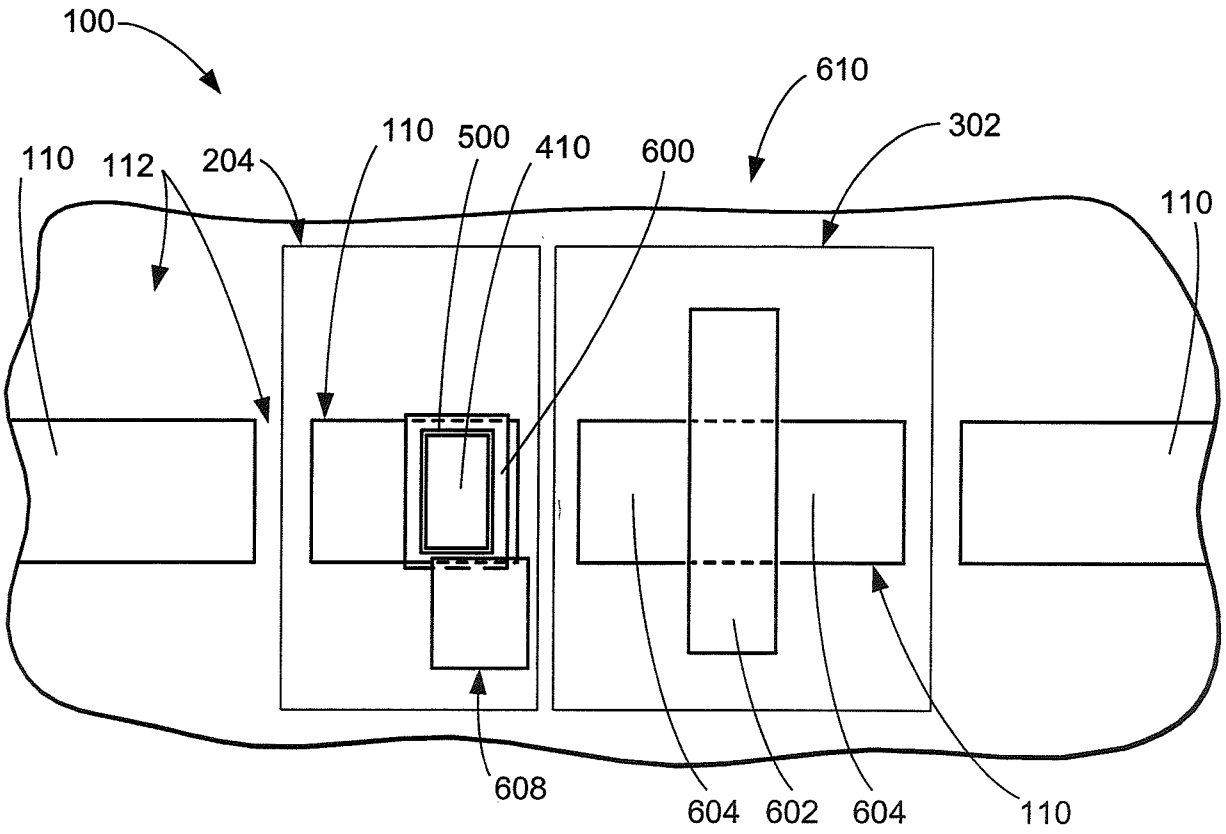

100
610
110
112
204
110
500
410
600
302
110
608
604
602
604
110

FIG. 6B

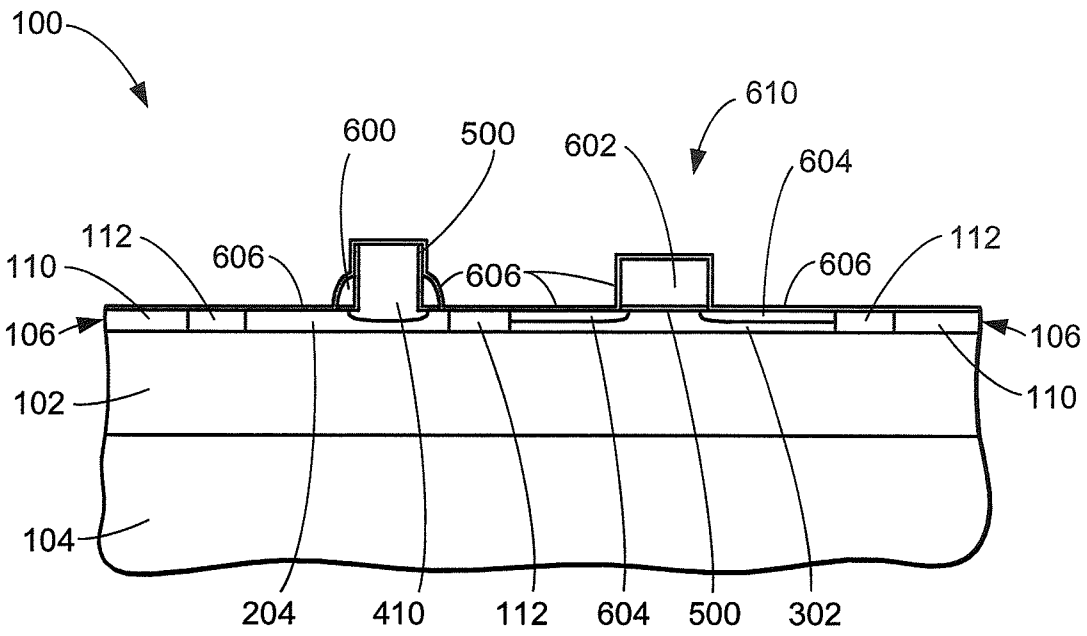

100
610
600
500
602
604
112
606
606
606
112
110
106
106
102
110
104
204
410
112
604
500
302

FIG. 6A

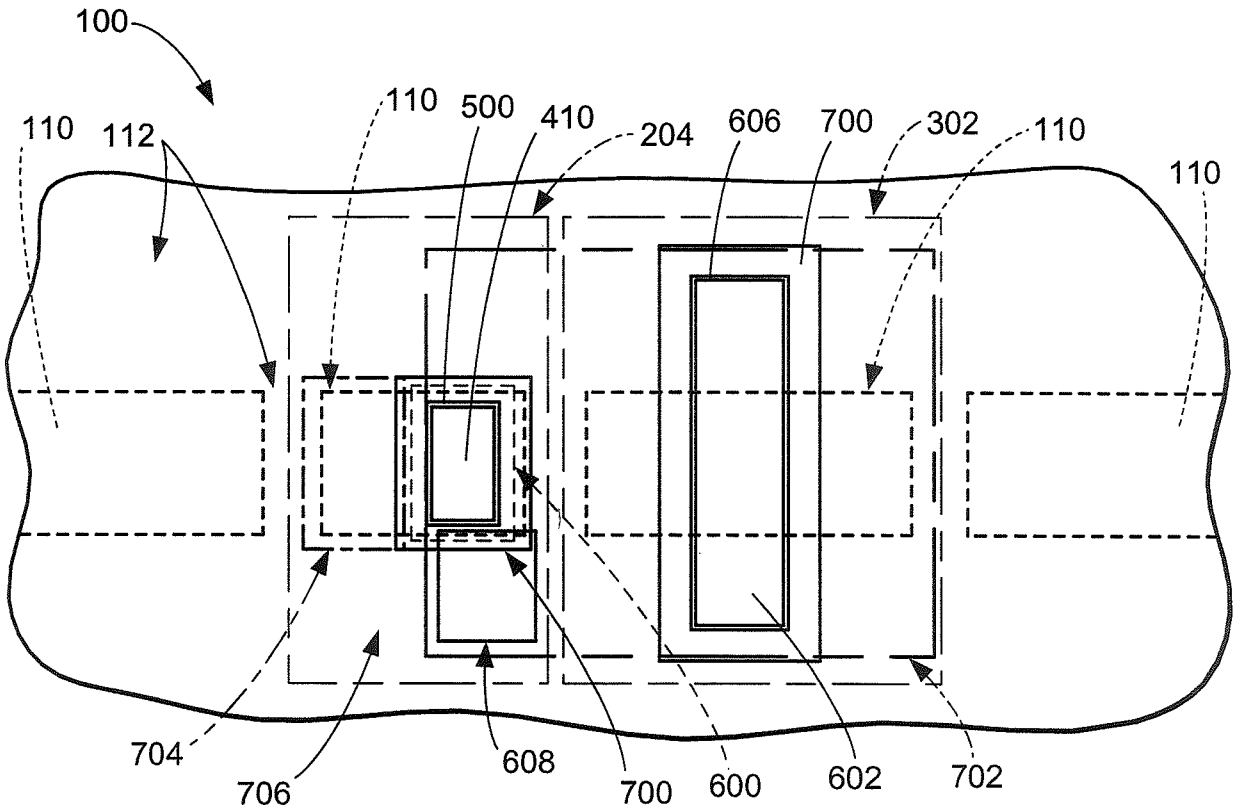

100
110
112
110
500
410
204
606
700
302
110
110
704
706
608
700
600
602
702

FIG. 7B

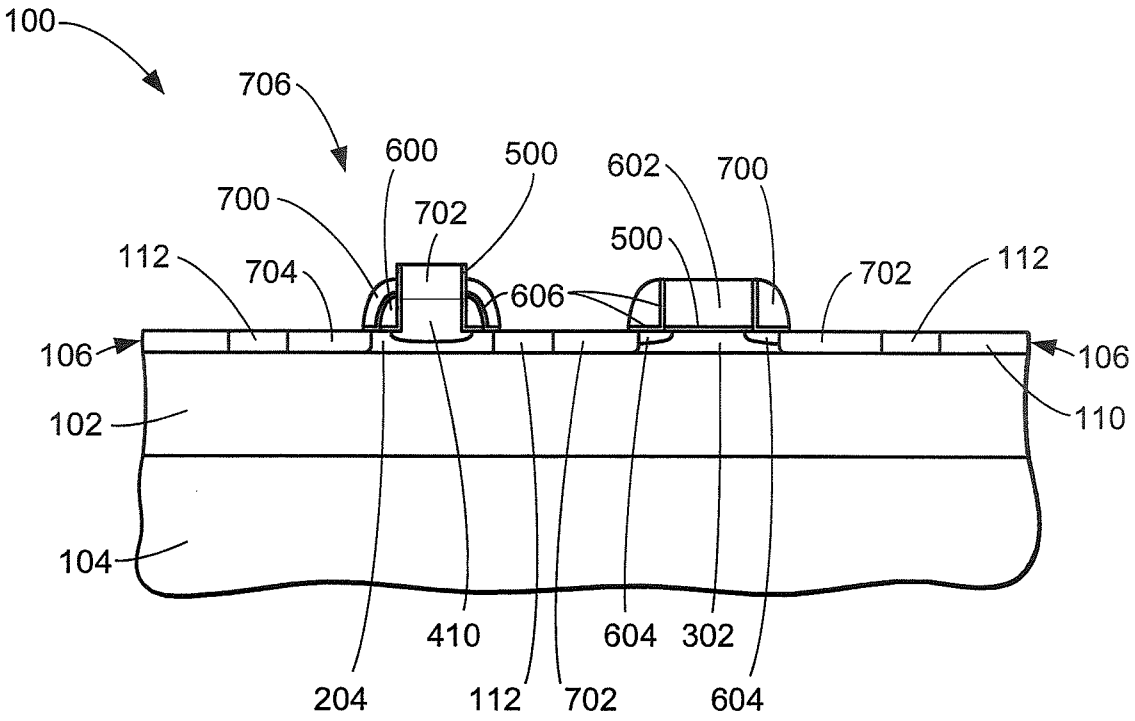

100
706
600
500
602
700
700
702
500
112
704
606
702
112
106
106
102
110
104
410
604
302
204
112
702
604

FIG. 7A

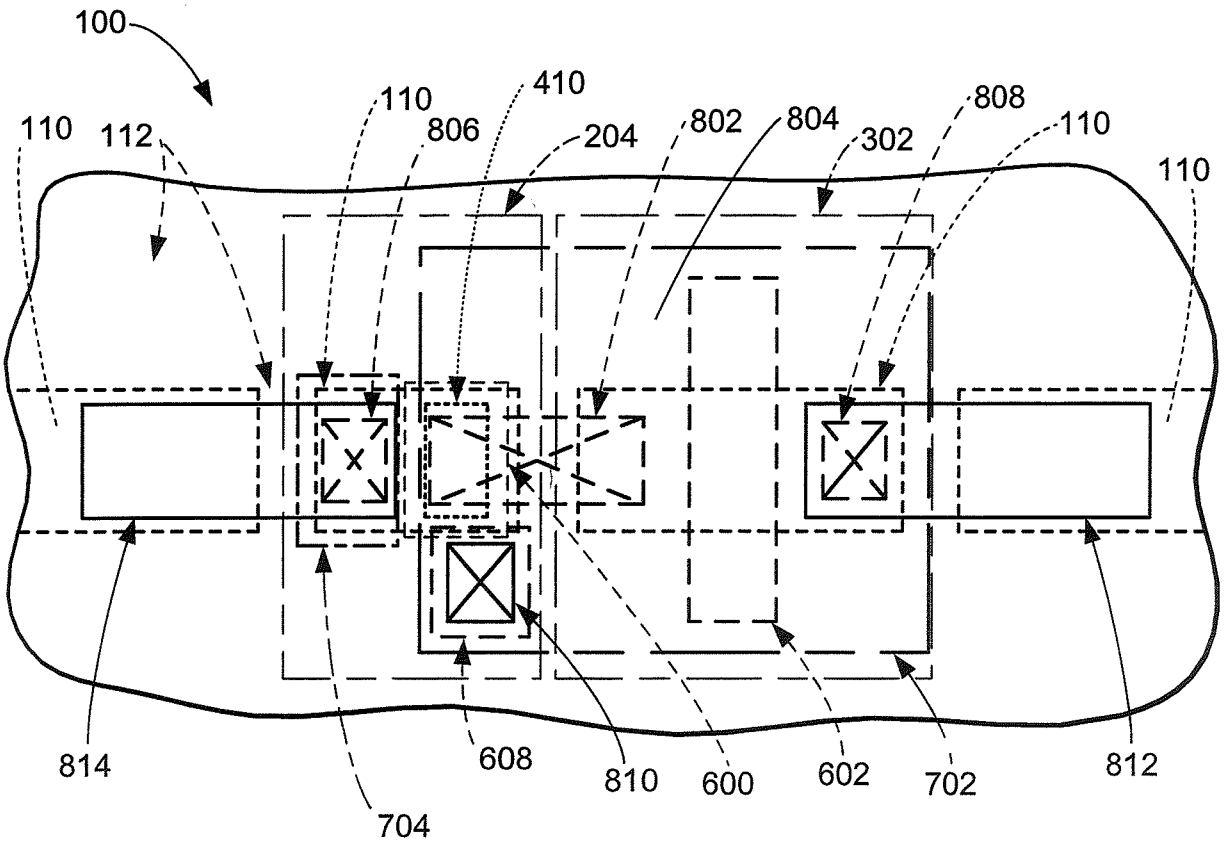

100
110
112
110
806
410
204
802
804
302
808
110
110
814
704
608
810
600
602
702
812

FIG. 8B

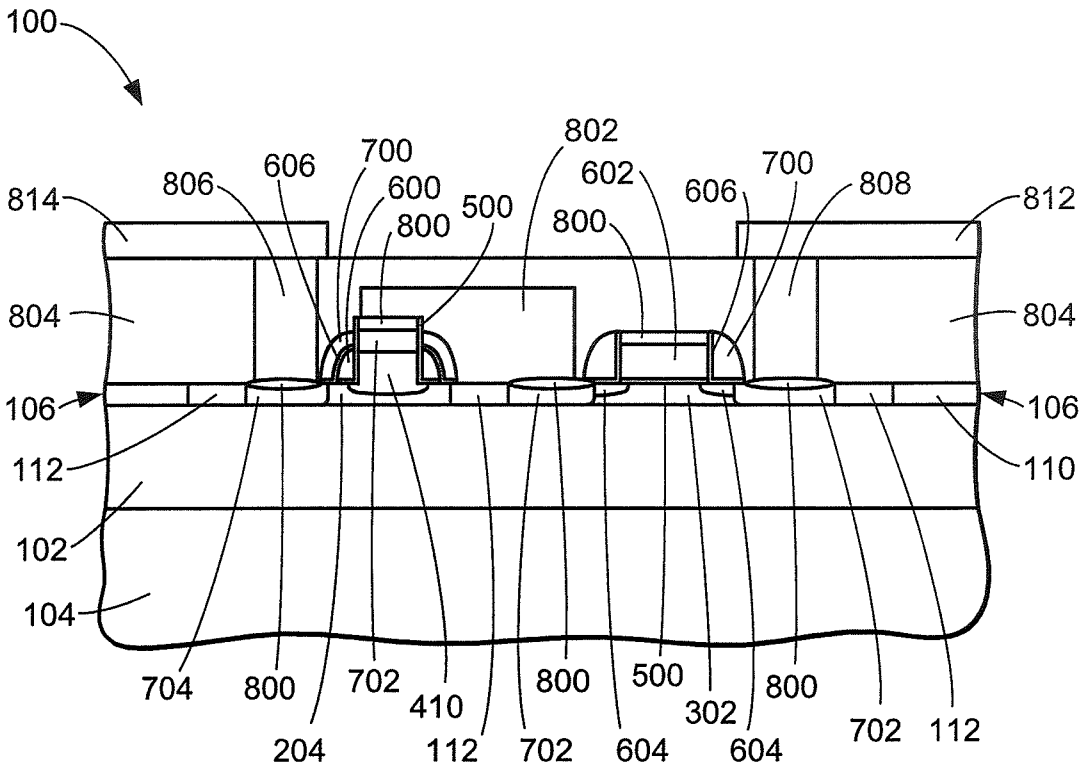

100
814
806
606
700
600
800
500
802
602
800
606
700
808
812
804
804
106
106
112
110
102
104
704
800
702
410
204
112
800
702
500
604
302
604
800
702
112

FIG. 8A

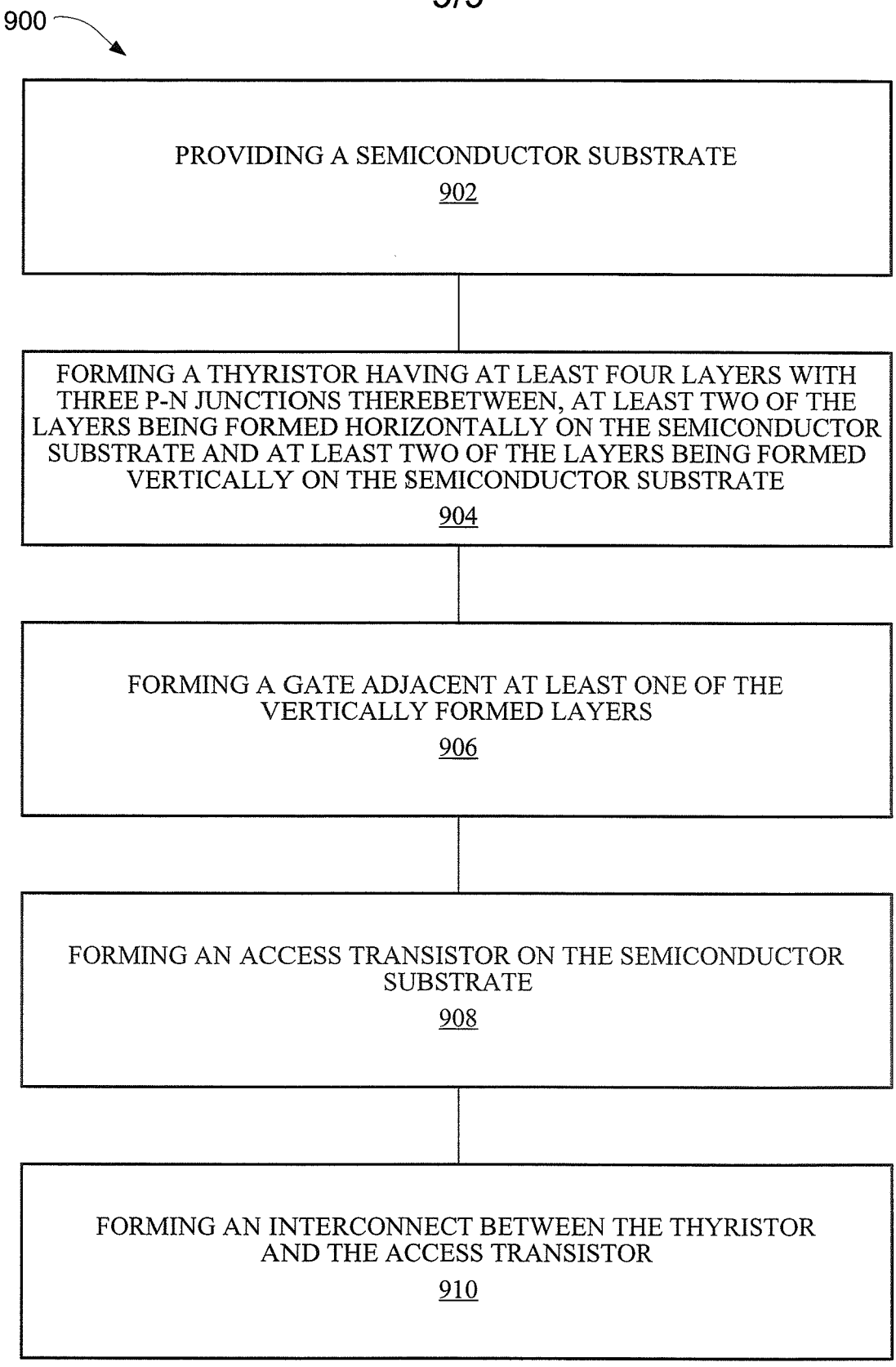

900
PROVIDING A SEMICONDUCTOR SUBSTRATE
902
FORMING A THYRISTOR HAVING AT LEAST FOUR LAYERS WITH THREE P-N JUNCTIONS THEREBETWEEN, AT LEAST TWO OF THE LAYERS BEING FORMED HORIZONTALLY ON THE SEMICONDUCTOR SUBSTRATE AND AT LEAST TWO OF THE LAYERS BEING FORMED VERTICALLY ON THE SEMICONDUCTOR SUBSTRATE
904
FORMING A GATE ADJACENT AT LEAST ONE OF THE VERTICALLY FORMED LAYERS
906
FORMING AN ACCESS TRANSISTOR ON THE SEMICONDUCTOR SUBSTRATE
908
FORMING AN INTERCONNECT BETWEEN THE THYRISTOR AND THE ACCESS TRANSISTOR
910

FIG. 9