



# CLAIMS (AMENDED)

1. A delta-sigma modulator comprising;
  - a first and a second integrators coupled in  
5 series between an analog input node and a first  
analog output node,
    - a first summing node coupled between said analog  
input node and said first integrator,
    - a second summing node coupled between said first  
10 integrator and said second integrator,
    - a local feedback loop including a first  
quantizer for quantizing a signal at said first  
analog output node, and a first reference voltage  
selector for providing said second summing node with  
15 a first analog feedback signal based upon an output  
from said first quantizer,
    - a plural-order feedback loop including a second  
quantizer for quantizing said signal at said first  
analog output node, and a second reference voltage  
20 selector for providing at least said first summing  
node with a second analog feedback signal based upon  
an output from said second quantizer,
    - a third summing node coupled to said first  
analog output node,
    - 25 a circuit-stage, coupled subsequently to said  
third summing node, including at least a third



integrator and a second output node coupled  
succeedingly in series, and,

a feedback loop including a third quantizer for  
quantizing a signal at said second analog output  
5 node, and a third reference voltage selector for  
providing said third summing node with a third  
analog feedback signal based upon an output from  
said third quantizer.

10 2. canceled

3. canceled

4. A delta-sigma modulator set forth in claim 1;  
15 further comprising an interstage summing node,  
coupled between said first analog output node and  
said third summing node, for adding an output signal  
at said first analog output node to said second  
analog feedback signal.

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5. A delta-sigma modulator set forth in claim 1;  
further comprising an amplifier with a scale factor  
of less than one, coupled between said first analog  
output node and said third summing node.

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6. A delta-sigma modulator set forth in claim 1;



further comprising a noise cancellation circuit for receiving outputs from said first quantizer and said second quantizer and said third quantizer, wherein said noise cancellation circuit has a function of  
5 canceling quantization noises generated by said first and second quantizers.

7. A delta-sigma modulator comprising;  
a first, a second and a third integrators  
10 sequentially coupled in series between an analog input node and a first analog output node,  
a local feedback loop including a first quantizer for quantizing a signal at said first analog output node, and a first reference voltage  
15 selector for providing a first analog feedback signal based upon an output from said first quantizer, wherein said local feedback loop adds said first analog feedback signal to an input of said third integrator,  
20 a plural-order feedback loop including a second quantizer for quantizing said signal at said first analog output node, and a second reference voltage selector for providing a second analog feedback signal based upon an output from said second  
25 quantizer, wherein said plural-order feedback loop



adds said second analog feedback signal at least to  
an input signal of said first integrator,

an interstage summing node for adding said  
signal at said first output node to said second  
5 analog feedback signal,

a circuit-stage, subsequently coupled to said  
interstage summing node, including a third summing  
node and at least a fourth integrator and a second  
output node coupled succeedingly in series, and,

10 a feedback loop including a third quantizer for  
quantizing a signal at said second analog output  
node, and a third reference voltage selector for  
providing third analog feedback signal based upon an  
output from said third quantizer, wherein said  
15 feedback loop adds said third analog feedback signal  
at least to said third summing node.

8. A delta-sigma modulator comprising;

plural integrators coupled in series between an  
20 analog input node and an analog output node,

a quantizer for quantizing a signal at said  
analog output node,

a reference voltage selector for providing an  
analog signal based upon an output from said  
25 quantizer, and,



a summing node for adding said analog signal from said reference voltage selector to at least one of said plural integrators inputs;

wherein said at least one integrator is composed  
5 of a switched capacitor integrator and said switched capacitor integrator samples said analog signal from said reference voltage selector in utilizing a capacitor in common for sampling said input signal.