

SHADOW RING KIT FOR PLASMA ETCH WAFER SINGULATION PROCESS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Non-provisional Application No. 17/064,470, filed on 06
5 October 2020, the entire contents of which are hereby incorporated by reference herein.

FIELD

Embodiments of the present disclosure pertain to the field of semiconductor processing and, in
particular, to apparatuses for and methods of dicing semiconductor wafers, each wafer having a
10 plurality of integrated circuits thereon.

DESCRIPTION OF RELATED ART

In semiconductor wafer processing, integrated circuits are formed on a wafer (also referred to as
a substrate) composed of silicon or other semiconductor material. In general, layers of various
15 materials which are either semiconducting, conducting or insulating are utilized to form the
integrated circuits. These materials are doped, deposited and etched using various well-known
processes to form integrated circuits. Each wafer is processed to form a large number of
individual regions containing integrated circuits known as dice.

Following the integrated circuit formation process, the wafer is "diced" to separate the individual
20 die from one another for packaging or for use in an unpackaged form within larger circuits. The
two main techniques that are used for wafer dicing are scribing and sawing. With scribing, a
diamond tipped scribe is moved across the wafer surface along pre-formed scribe lines. These
scribe lines extend along the spaces between the dice. These spaces are commonly referred to as
"streets." The diamond scribe forms shallow scratches in the wafer surface along the streets.
25 Upon the application of pressure, such as with a roller, the wafer separates along the scribe lines.
The breaks in the wafer follow the crystal lattice structure of the wafer substrate. Scribing can be
used for wafers that are about 10 mils (thousandths of an inch) or less in thickness. For thicker
wafers, sawing is presently the preferred method for dicing.

With sawing, a diamond tipped saw rotating at high revolutions per minute contacts the wafer
30 surface and saws the wafer along the streets. The wafer is mounted on a supporting member
such as an adhesive film stretched across a film frame and the saw is repeatedly applied to both
the vertical and horizontal streets. One problem with either scribing or sawing is that chips and
gouges can form along the severed edges of the dice. In addition, cracks can form and propagate
from the edges of the dice into the substrate and render the integrated circuit inoperative.
35 Chipping and cracking are particularly a problem with scribing because only one side of a square

or rectangular die can be scribed in the <110>direction of the crystalline structure.

Consequently, cleaving of the other side of the die results in a jagged separation line. Because of chipping and cracking, additional spacing is required between the dice on the wafer to prevent damage to the integrated circuits, e.g., the chips and cracks are maintained at a distance from the

5 actual integrated circuits. As a result of the spacing requirements, not as many dice can be formed on a standard sized wafer and wafer real estate that could otherwise be used for circuitry is wasted. The use of a saw exacerbates the waste of real estate on a semiconductor wafer. The blade of the saw is approximately 15 to 60 microns thick. As such, to insure that cracking and other damage surrounding the cut made by the saw does not harm the integrated circuits, from 60
10 to three to five hundred microns often must separate the circuitry of each of the dice.

Furthermore, after cutting, each die requires substantial cleaning to remove particles and other contaminants that result from the sawing process.

Plasma dicing has also been used, but may have limitations as well. For example, one limitation hampering implementation of plasma dicing may be cost. A standard lithography operation for
15 patterning resist may render implementation cost prohibitive. Another limitation possibly hampering implementation of plasma dicing is that plasma etching of commonly encountered metals (e.g., copper) in dicing along streets can create production issues or throughput limits.

SUMMARY

20 Embodiments of the present disclosure include methods of, and apparatuses for, dicing semiconductor wafers.

In an embodiment, an etch apparatus includes a chamber, and a plasma source within or coupled to the chamber. An electrostatic chuck is within the chamber, the electrostatic chuck including a conductive pedestal to support a substrate carrier sized to support a wafer having a first diameter.

25 A shadow ring assembly is between the plasma source and the electrostatic chuck, the shadow ring assembly sized to process a wafer having a second diameter smaller than the first diameter.

In another embodiment, a method of dicing a semiconductor wafer having a plurality of integrated circuits includes forming a mask above the semiconductor wafer, the mask being or including a layer covering and protecting the integrated circuits, and the semiconductor wafer
30 supported by a substrate carrier sized to support a wafer having a first diameter. The method also involves patterning the mask with a laser scribing process to provide a patterned mask with gaps exposing regions of the semiconductor wafer between the integrated circuits. The method also involves etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits while the semiconductor wafer is supported by the substrate

carrier and while the substrate carrier is partially covered by a shadow ring assembly sized to process the semiconductor wafer having a second diameter smaller than the first diameter.

In another embodiment, a system for dicing a semiconductor wafer having a plurality of integrated circuits includes a factory interface. A laser scribe apparatus is coupled with the factory interface and includes a laser. An etch apparatus is coupled with the factory interface, the etch apparatus including a chamber, a plasma source within or coupled to the chamber, an electrostatic chuck within the chamber, the electrostatic chuck including a conductive pedestal to support a substrate carrier sized to support a wafer having a first diameter, and a shadow ring assembly between the plasma source and the electrostatic chuck, the shadow ring assembly sized to process a wafer having a second diameter smaller than the first diameter.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A illustrates an angled view of components of a shadow ring kit, in accordance with an embodiment of the present disclosure.

Figure 1B illustrates cross-sectional views of a chuck including a shadow ring kit in a raised position and in a seated position, and an angled view of a substrate carrier, in accordance with an embodiment of the present disclosure.

Figure 1C illustrates an angled view and a cross-sectional view of a chuck including a shadow ring kit, and cross-sectional views of the shadow ring kit, in accordance with an embodiment of the present disclosure.

Figure 1D illustrates cross-sectional views of a portion of a shadow ring assembly for accommodating a 200mm wafer, in accordance with an embodiment of the present disclosure.

Figure 1E illustrates cross-sectional views of a portion of a shadow ring assembly for accommodating a 200mm wafer, in accordance with an embodiment of the present disclosure.

Figure 1F illustrates an angled view of an assembly including a lift hoop assembly and a supported shadow ring assembly, in accordance with an embodiment of the present disclosure.

Figure 2A illustrates an angled cross-sectional view of an electrostatic chuck, in accordance with an embodiment of the present disclosure.

Figure 2B illustrates a plan view of a substrate carrier suitable for supporting a thin wafer during a singulation process, in accordance with an embodiment of the present disclosure.

Figure 2C illustrates an angled view of various aspects and portions of an electrostatic chuck, in accordance with an embodiment of the present disclosure.

Figures 3A-3C illustrate a plan view, a cross-sectional view, and an angled view of various aspects and portions of an electrostatic chuck, in accordance with an embodiment of the present disclosure.

Figure 4 illustrates a cross-sectional view of a plasma etch apparatus, in accordance with an embodiment of the present disclosure.

Figure 5 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present disclosure.

- 5 Figures 6A-6C illustrate cross-sectional views representing various operations a method of dicing a semiconductor wafer, in accordance with an embodiment of the present disclosure.

Figure 7 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present disclosure.

- 10 Figures 8A-8D illustrate cross-sectional views of various operations in a method of dicing a semiconductor wafer, in accordance with an embodiment of the present disclosure.

Figure 9 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present disclosure.

15 **DETAILED DESCRIPTION**

Methods of, and apparatuses for, dicing semiconductor wafers are described. In the following description, numerous specific details are set forth, such as electrostatic chuck configurations, laser scribing conditions, and plasma etching conditions and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known aspects, such as integrated circuit fabrication, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

- 20 One or more embodiments are directed particularly to a 200mm wafer plasma dicing shadow ring kit. Embodiments may be suitable for plasma dicing using a shadow ring kit for processing a 200mm wafer in a 300mm etch chamber. Embodiments may be applicable to laser and etch wafer dicing approaches and tooling for singulation or dicing of electronic device wafers.

- To provide context, currently, 200mm wafers are being processed using 200mm wafer mounting tape frame using a 200mm etch chamber. Embodiments described herein can be implemented to enable mounting of 200mm wafer on an approximately 400mm wafer mounting frame and process the 200mm wafer using a 300mm etch plasma dicing chamber. Furthermore, shadow ring kits described herein can be customized to accommodate a different thickness of a wafer for further process enhancement and yield improvement.
- 30

- One or more embodiments are directed to a shadow ring process kit design that enables running a 200mm wafer mounted on tape frame sized to support a 300mm wafer using a 300mm etch plasma dicing chamber. Embodiments described herein can be implemented to enable running a 200mm wafer in a 300mm plasma dicing etch chamber. Embodiments described herein can be implemented to reduce cost and foot print by not requiring a dedicated 200mm etch chamber. Embodiments described herein can be implemented to provide flexibility to use a “standard 400mm tape frame” for both 200 and 300mm wafer dicing and/or processing. In an embodiment, switching between a 300mm and a 200mm wafer for processing is easier with minimal setup change and tool down time.
- To provide further context, during singulation of a wafer into individual die, the wafer is cut or sectioned along dicing streets between the dies. Traditionally, dicing has been performed with a mechanical saw. Mobile devices and other technology drivers may require more advanced singulation approaches to reduce cracking, delamination, and chipping defects. A laser and etch wafer dicing approach may involve applying a water soluble protective coating to a substrate, removing the coating any device test layers in the street regions removed by laser scribing to open up the underlying substrate material, which is typically silicon (Si). The exposed Si is then plasma etched through its entire thickness to singulate the wafer into the individual die. The protective coating is removed in a deionized (DI) water based cleaning operation. Water soluble protective coatings may be desirable due to environmental considerations and ease of processing.
- Such a water soluble coating may primarily be used as an etch mask during the plasma etching step, and also as a layer that collects any debris generated during laser scribing.
- To provide yet further context, femtosecond lasers may be preferred in the laser scribing portion of the process. Unlike nanosecond and other long pulse lasers, femtosecond lasers have little heat effect because of the associated ultra-short pulses. Another advantage of femtosecond lasers may be the capability to remove most materials including absorptive, reflective and transparent materials. On typical wafers, there are metals which are reflective and absorptive, the dielectrics which are transparent, and the silicon substrate which is absorptive to most laser light. The water-soluble protective coating is totally or mostly transparent, or can be partially absorbing, e.g., if including a dye additive. These listed materials can be ablated by femtosecond lasers. It is to be appreciated that although many embodiments described below are associated with femtosecond laser scribing, in other embodiments, laser scribing with other laser beam types may also be compatible with masking materials described herein. It is also to be appreciated that although many embodiments described below are associated with scribing streets having metallized features, in other embodiments, metal free scribing streets may also be considered. It is also to

be appreciated that although many embodiments described below are associated with water soluble dicing masks, in other embodiments, other mask materials may also be considered.

In accordance with one or more embodiments of the present disclosure, a 300mm wafer mounting frame is used to mount a 200mm wafer and process in an existing 300mm etch plasma dicing chamber. Embodiments can be implemented to enable switching between a 200mm wafer and a 300mm wafer with minimum setup time. In an embodiment, a shadow ring kit includes a carrier, an insert ring, and a heat shield. A shadow ring kit such as described herein can be used to help in preventing tape heating and burn during an etching process. The insert ring can act as an independent “floating” part without touching a carrier and heat shield during wafer processing (e.g., by being supported by an outermost portion of the processed wafer or substrate). The arrangement can prevent heat transfer from wafer to carrier. The heat shield can help to prevent heat transfer to carrier while processing. In an embodiment, the insert ring and heat shield profile provides an edge exclusion on the wafer during etching processing.

As an exemplary assembly, Figure 1A illustrates an angled view of components of a shadow ring kit 100, in accordance with an embodiment of the present disclosure.

Referring to Figure 1A, the shadow ring kit includes a heat shield 102, an insert ring 104, and a carrier 106. In an embodiment, the heat shield, 102, the insert ring 104, and the carrier 106 are all composed of solid alumina. In an embodiment, the heat shield 102 includes a pocket therein to accommodate the insert ring 104 without contacting the insert ring 104, e.g., to avoid thermal contact. In an embodiment, the insert ring 104 is sized to accommodate a 200mm wafer. In one such embodiment, the insert ring 104 has an inner opening with a diameter of about 197 mm to leave an outermost about 1.5mm perimeter of the 200mm wafer covered by the insert ring 104. In one such embodiment, the insert ring 104 rests on the about 1.5mm perimeter of the 200mm wafer covered by the insert ring 104.

Figure 1B illustrates cross-sectional views of a chuck including a shadow ring kit in a raised position and in a seated position, and an angled view of a substrate carrier, in accordance with an embodiment of the present disclosure.

Referring to part (i) of Figure 1B, a chuck assembly 110A includes a shadow ring kit 112 in a raised position. In one embodiment, the shadow ring kit 112 is an assembly such as shadow ring kit 100 described above. The shadow ring kit 100 is above a substrate carrier assembly 114, which can include a tape frame supporting a 200mm wafer. The substrate carrier assembly 114 is supported by an electrostatic chuck (ESC), such as an ESC sized to typically support a 300mm wafer or a substrate carrier of a 300 mm wafer. The chuck assembly 110A also includes a lift hoop assembly 118. Referring to part (ii) of Figure 1B, a chuck assembly 110B includes the shadow ring kit 112 in a seated position. Referring to both parts (i) and (ii) of Figure 1B, nail

head lift pins 119 are included for lifting up and down between positions 110A and 110B.

Referring to part (iii) of Figure 1B, an exemplary substrate carrier assembly 114 is shown including a wafer tap frame 114A (which may be sized to accommodate a 300 mm wafer), a dicing tape 114B, and a 200mm wafer (e.g., in a location where a 300 mm wafer would typically be seated).

Figure 1C illustrates an angled view 120 and a cross-sectional view 122 of a chuck including a shadow ring kit, and cross-sectional views of the shadow ring kit, in accordance with an embodiment of the present disclosure.

Referring to Figure 1C, an electrostatic chuck assembly 122 includes an electrostatic chuck (ESC) 121. A shadow ring assembly is over the ESC 121 of the electrostatic chuck assembly 122. The shadow ring assembly includes a heat shield 102, an insert ring 104, and a carrier 106. In an embodiment, when in position for processing, the insert ring 104 is accommodated within a pocket in the heat shield 102 without contacting the heat shield 102, as is depicted. In one embodiment, the insert ring 104 interlocks with the carrier 106, as is depicted.

In a first specific example, Figure 1D illustrates cross-sectional views of a portion of a shadow ring assembly for accommodating a 200mm wafer, in accordance with an embodiment of the present disclosure.

Referring to Figure 1D, a shadow ring assembly 130A includes a heat shield 102A, an insert ring 104A, and a carrier 106A. In an embodiment, when in position for processing, the insert ring 104A is accommodated within a pocket in the heat shield 102A without contacting the heat shield 102A, as is depicted. In one embodiment, the insert ring 104A interlocks with the carrier 106A, as is depicted.

In a second specific example, Figure 1E illustrates cross-sectional views of a portion of a shadow ring assembly for accommodating a 200mm wafer, in accordance with an embodiment of the present disclosure.

Referring to Figure 1E, a shadow ring assembly 130B includes a heat shield 102B, an insert ring 104B, and a carrier 106B. In an embodiment, when in position for processing, the insert ring 104B is accommodated within a pocket in the heat shield 102B without contacting the heat shield 102B, as is depicted. In one embodiment, the insert ring 104B interlocks with the carrier 106B, as is depicted. In comparison to the carrier 106A of the shadow ring assembly 130A, the shape of the carrier 106B of the shadow ring assembly 130B may provide a larger gap between the carrier 106B and a dicing tape of a substrate carrier, which can aid in avoiding tape sticking issues.

As an exemplary supporting and/or moving mechanism, Figure 1F illustrates an angled view of an assembly 140 including a lift hoop assembly and a supported shadow ring assembly, in accordance with an embodiment of the present disclosure.

Referring to Figure 1F, a lift hoop assembly 142 includes a lift hoop 144, lift pins 146, and a
5 servo motor 148. The supported shadow ring assembly includes a heat shield 102, an insert ring (not seen in this view), and a carrier 106, such as described in association with Figure 1A.

In another aspect, Figure 2A illustrates an angled cross-sectional view of an electrostatic chuck, in accordance with an embodiment of the present disclosure. The electrostatic chuck can be paired with a shadow ring assembly such as described in association with Figures 1A, 1D and
10 1E.

Referring to Figure 2A, an electrostatic chuck assembly 200 includes a shadow ring or heat shield 202 and associated shadow ring insert 204 and shadow ring carrier 206. It is to be appreciated that the shadow ring or heat shield 202 and associated shadow ring insert 204 and shadow ring carrier 206, as depicted, are sized to accommodate 300mm wafer processing.
15 However, in other embodiments, a shadow ring or heat shield 102 and associated shadow ring insert 104 and shadow ring carrier 106, such as described in Figure 1A, are instead included in order to accommodate 200mm wafer processing. In one embodiment, all of the shadow ring or heat shield 202, shadow ring insert 204 and shadow ring carrier 206 are composed of a ceramic material such as alumina. A substrate on the substrate carrier may be included beneath the
20 shadow ring, and a tape frame 208 of a substrate carrier may be included beneath the heat shield, as is depicted in Figure 2A. The tape frame 208 may be composed of stainless steel. An adjustable lift pin 207 is included for lifting the shadow ring, and may be composed of aluminum.

The electrostatic chuck assembly 200 further includes an edge insulator ring 210 around a
25 conductive pedestal 212. A bottom insulator ring 218 is beneath the conductive pedestal 212. The edge insulator ring 210 and the bottom insulator ring 218 may be composed of a ceramic material such as alumina, and the conductive pedestal 212 may be composed of aluminum. The conductive pedestal 212 may be electrically coupled to ground and/or to a DC voltage.

The electrostatic chuck assembly 200 further includes a plasma screen segment 214 and a plasma
30 screen basket 216, both of which may be composed of aluminum. The electrostatic chuck assembly 200 further includes a cathode insulator 220, a facilities insulator 222, and a cathode liner 224. The cathode insulator 220 may be composed of silicon dioxide, and the cathode liner 224 may be composed of aluminum. The electrostatic chuck assembly 200 further includes a support pedestal 226 and a gas feedthrough 228, such as a helium feedthrough.

A lift pin 230 and lift pin finger 232 are included in the electrostatic chuck assembly 200. The lift pin 230 may be composed of alumina, and the lift pin finger 232 may be composed of aluminum. It is to be appreciated that a plurality of such lift pins 230 may be included in the electrostatic chuck assembly 200. In an embodiment, such a plurality of lift pins 230 is located
5 outside of a perimeter of a processing region of the conductive pedestal 212. In one such embodiment, the plurality of lift pins 230 is arranged for contacting a tape frame 208 of a substrate carrier.

In an embodiment, an exposed surface 260 and a covered surface 270 of the conductive pedestal 212 are coated with a ceramic material, such as alumina. In an embodiment, each lift pin 230 is
10 included in an opening 250. In one such embodiment, opening 250 is a hole included in conductive pedestal 212, as is depicted in Figure 2A and described in greater detail below in association with Figure 2C. The hole may not be coated with a ceramic material and may be a location susceptible to current leakage from the electrostatic chuck assembly. In another such embodiment, opening 250 is a notch included at a circumferential edge a conductive pedestal, as
15 is described in greater detail below in association with Figures 3A-3C. The notches of the embodiment of Figures 3A-3C may be coated with a ceramic material and may mitigate current leakage from the electrostatic chuck assembly relative to the holes of the embodiment of Figures 2A-2C.

In an aspect of the present disclosure, a thin substrate (e.g., with a thickness of approximately
20 100 microns or less) is accommodated in a hybrid laser ablation and plasma etching singulation process. In one such embodiment, the thin substrate is supported on a substrate carrier. For example, Figure 2B illustrates a plan view of a substrate carrier suitable for supporting a thin wafer during a singulation process, in accordance with an embodiment of the present disclosure. Referring to Figure 2B, a substrate carrier 280 includes a layer of backing tape 282 surrounded
25 by a tape ring or frame 284. A wafer or substrate 286, such as a thin wafer or substrate, is supported by the backing tape 282 of the substrate carrier 280. In one embodiment, the wafer or substrate 286 is attached to the backing tape 282 by a die attach film. As shown with the solid line, wafer or substrate 286 is a 300 mm wafer, i.e., the substrate carrier 280 is sized to accommodate a 300 mm wafer. However, in accordance with an embodiment of the present
30 disclosure, a 200mm wafer (dashed line 287) is supported by the substrate carrier 280, even the substrate carrier 280 is sized for a 300 mm wafer. In one embodiment, the tape ring or frame 284 is composed of stainless steel. In an embodiment, an electrostatic chuck described in association with Figures 1B, 1C, 2A, 2C or 3A-3C accommodates an assembly such as substrate carrier 280. In an embodiment, a singulation process can be accommodated in a system sized to receive a
35 substrate carrier such as the substrate carrier 280. In one such embodiment, a system such as

system 400 or 500 described below can accommodate a thin wafer frame without impact on the system footprint that is otherwise sized to accommodate a substrate or wafer not supported by a substrate carrier. In one embodiment, system 400 or 500 is sized to accommodate 300 millimeter-in-diameter wafers or substrates; however, in an embodiment, 200mm wafer are processed therein. The same system can accommodate a wafer carrier approximately 380 millimeters in width by 380 millimeters in length, as depicted in Figure 2B.

Figure 2C illustrates an angled view 290 of various aspects and portions of an electrostatic chuck, in accordance with an embodiment of the present disclosure. Like numbers from Figures 2A are as described above in association with Figure 2A. The electrostatic chuck can be paired with a shadow ring assembly such as described in association with Figures 1A, 1D and 1E.

Referring to Figure 2C, an electrostatic chuck includes a conductive pedestal 212 having a plurality of holes 294 near a circumferential edge thereof. The electrostatic chuck can accommodate a plurality of lift pins corresponding to ones of the plurality of holes 294. In an embodiment, the conductive pedestal 212 is coated with a ceramic material such as alumina, but inner surfaces of each of the plurality of holes are not coated with the ceramic material.

In an embodiment, the electrostatic chuck further includes an edge insulator ring 210 laterally around the conductive pedestal 212. In an embodiment, the electrostatic chuck further includes a bottom insulator ring 218 beneath the conductive pedestal 212, the bottom insulator ring 218 having a plurality of openings 246 in Figure 2C corresponding to ones of the plurality of lift pins.

In an embodiment, the plurality of lift pins is located outside of a perimeter of a processing region 292 of the conductive pedestal 212, and the plurality of lift pins is arranged for contacting a substrate carrier. In an embodiment, the electrostatic chuck is included in a process chamber together with a shadow ring, shadow ring assembly, or shadow ring kit positioned over the plurality of lift pins, as is described in association with Figure 1A-1F. In one such embodiment, the shadow ring, shadow ring assembly, or shadow ring kit is sized for etching 200mm wafers.

Figures 3A, 3B and 3C illustrate a plan view 300, a cross-sectional view 320, and an angled view 340, respectively, of various aspects and portions of an electrostatic chuck, in accordance with another embodiment of the present disclosure. Like numbers from Figures 2A are as described above in association with Figure 2A. The electrostatic chuck can be paired with a shadow ring assembly such as described in association with Figures 1A, 1D and 1E.

Referring to Figures 3A-3C, an electrostatic chuck includes a conductive pedestal 312 having a plurality of notches 302 at a circumferential edge thereof. The electrostatic chuck also includes a plurality of lift pins 230 corresponding to ones of the plurality of notches 302. In an embodiment, the conductive pedestal 312 and surfaces of the plurality of notches 302 are coated

with a ceramic material. In one such embodiment, wherein the ceramic material is or includes alumina.

In an embodiment, the electrostatic chuck further includes an edge insulator ring 310 laterally around the conductive pedestal 312. The edge insulator ring 310 has a plurality of inner
5 protrusions 362 corresponding to ones of the plurality of notches 302. Each of the plurality of inner protrusions 362 has an opening there through to accommodate corresponding ones of the plurality of lift pins 230.

In an embodiment, the electrostatic chuck further includes a bottom insulator ring 318 beneath the conductive pedestal 312. The bottom insulator ring 312 has a plurality of openings (322 in
10 Figure 3B, and 346 in Figure 3C) corresponding to ones of the plurality of lift pins.

In an embodiment, the edge insulator ring 310 and the bottom insulator ring 318 are composed of a ceramic material such as alumina, and the conductive pedestal 312 is composed of aluminum.

The conductive pedestal 312 may be electrically coupled to ground and/or a DC voltage.

In an embodiment, the plurality of lift pins 230 is located outside of a perimeter of a processing
15 region 342 of the conductive pedestal 312. In one such embodiment, the plurality of lift pins 230 is arranged for contacting a substrate carrier. In an embodiment, the electrostatic chuck further includes a shadow ring or shadow ring assembly positioned over the plurality of lift pins 230, as is described in association with Figure 2A.

In an aspect of the present disclosure, a substrate carrier is accommodated in an etch chamber
20 during a singulation process. In an embodiment, the assembly including a thin wafer or substrate on the substrate carrier is subjected to a plasma etch apparatus without affecting (e.g., etching) the film frame (e.g., tape ring or frame 284) and the film (e.g., backing tape 282). Furthermore, aspects of the disclosure address transfer and support a wafer or substrate supported by a combination film and film frame (substrate carrier) during the etch process. In particular, an etch
25 apparatus may be configured to accommodate etching of a thin wafer or substrate supported by a substrate carrier. For example, Figure 4 illustrates a cross-sectional view of an etch apparatus, in accordance with an embodiment of the present disclosure.

Referring to Figure 4, an etch apparatus 400 includes a chamber 402. An end effector 404 is included for transferring a substrate carrier 406 to and from chamber 402. An inductively
30 coupled plasma (ICP) source 408 is positioned above the chamber 402. The chamber 402 is further equipped with a throttle valve 410 and a turbo molecular pump 412. In an embodiment, the etch apparatus 400 also includes an electrostatic chuck assembly 414, such as an electrostatic chuck described above. In an embodiment, the etch apparatus 400 also includes a lift pin actuator 416 and/or a shadow mask or ring actuator 1418, as is depicted.

A single process tool may be configured to perform many or all of the operations in a hybrid laser ablation and plasma etch singulation process. For example, Figure 5 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present disclosure. It is to be appreciated that, in light of the disclosure below, in other embodiments, coat/bake/clean (CBC) processing chambers may instead be included on a separate tool or as separate tools. In other embodiments, a plasma etch chamber and a laser scribe apparatus are stand-alone tools.

Referring to Figure 5, a process tool 500 includes a factory interface 502 (FI) having a plurality of load locks 504 coupled therewith. A cluster tool 506 is coupled with the factory interface 502.

The cluster tool 506 includes one or more plasma etch chambers, such as plasma etch chamber 508. A laser scribe apparatus 510 is also coupled to the factory interface 502. The overall footprint of the process tool 500 may be, in one embodiment, approximately 3500 millimeters (3.5 meters) by approximately 3800 millimeters (3.8 meters), as depicted in Figure 5. In an embodiment, the laser scribe apparatus 510 is configured to perform laser ablation of streets between integrated circuits of a semiconductor wafer, and the plasma etch chamber 508 is configured to etch the semiconductor wafer to singulate the integrated circuits subsequent to the laser ablation.

In an embodiment, the laser scribe apparatus 510 houses a laser assembly configured to provide a femto-second based laser beam. In one such embodiment, the femtosecond-based laser has a wavelength of approximately less than or equal to 530 nanometers with a laser pulse width of approximately less than or equal to 400 femtoseconds. In an embodiment, the laser is suitable for performing a laser ablation portion of a hybrid laser and etch singulation process, such as the laser ablation processes described below. In one embodiment, a moveable stage is also included in laser scribe apparatus 510, the moveable stage configured for moving a wafer or substrate (or a carrier thereof) relative to the laser. In a specific embodiment, the laser is also moveable. The overall footprint of the laser scribe apparatus 510 may be, in one embodiment, approximately 2240 millimeters by approximately 1270 millimeters, as depicted in Figure 5.

In an embodiment, the one or more plasma etch chambers 508 is configured for etching a wafer or substrate through the gaps in a patterned mask to singulate a plurality of integrated circuits. In one such embodiment, the one or more plasma etch chambers 508 is configured to perform a deep silicon etch process. In a specific embodiment, the one or more plasma etch chambers 508 is an Applied Centura® Silvia™ Etch system, available from Applied Materials of Sunnyvale, CA, USA. The etch chamber may be specifically designed for a deep silicon etch used to create singulate integrated circuits housed on or in single crystalline silicon substrates or wafers. In an embodiment, a high-density plasma source is included in (or is coupled to) the plasma etch

chamber 508 to facilitate high silicon etch rates. In an embodiment, more than one etch chamber is included in the cluster tool 506 portion of process tool 500 to enable high manufacturing throughput of the singulation or dicing process.

Plasma etch chamber 508 may include an electrostatic chuck therein. In an embodiment, the electrostatic chuck includes a conductive pedestal having a plurality of notches at a circumferential edge thereof, and a plurality of lift pins corresponding to ones of the plurality of notches, as described above. In one embodiment, the conductive pedestal and surfaces of the plurality of notches of the electrostatic chuck are coated with a ceramic material. In one embodiment, the electrostatic chuck further includes an edge insulator ring (e.g., 310) laterally around the conductive pedestal (e.g., 312), the edge insulator ring having a plurality of inner protrusions (e.g., 362) corresponding to ones of the plurality of notches (e.g., 302), each of the plurality of inner protrusions having an opening there through to accommodate corresponding ones of the plurality of lift pins. In one embodiment, the electrostatic chuck further includes a bottom insulator ring (e.g., 318) beneath the conductive pedestal (e.g., 312), the bottom insulator ring having a plurality of openings (e.g., 346) corresponding to ones of the plurality of lift pins. In one embodiment, the plurality of lift pins of the electrostatic chuck of the plasma etch chamber 508 is located outside of a perimeter of a processing region (e.g., 342) of the conductive pedestal (e.g., 312), the plurality of lift pins arranged for contacting a substrate carrier (e.g., for contacting the tape ring or frame 284 of the substrate carrier assembly 280 described in association with Figure 2B).

The factory interface 502 may be a suitable atmospheric port to interface between an outside manufacturing facility with laser scribe apparatus 510 and cluster tool 506. The factory interface 502 may include robots with arms or blades for transferring wafers (or carriers thereof) from storage units (such as front opening unified pods) into either cluster tool 506 or laser scribe apparatus 510, or both.

Cluster tool 506 may include other chambers suitable for performing functions in a method of singulation. For example, in one embodiment, a deposition and/or bake chamber 512 is included. The deposition and/or bake chamber 512 may be configured for mask deposition on or above a device layer of a wafer or substrate prior to laser scribing of the wafer or substrate. Such a mask material may be baked prior to the dicing process, as is described above. Such a mask material may be water soluble, as is also described below.

In an embodiment, referring again to Figure 5, a wet station 514 is included. The wet station may be suitable for cleaning performing a room temperature or a hot aqueous treatment for removing a water soluble mask, as is described below, subsequent to a laser scribe and plasma etch singulation process of a substrate or wafer, or subsequent to a laser scribe-only singulation

process. In an embodiment, although not depicted, a metrology station is also included as a component of process tool 500. The cleaning chamber can include atomized mist and/or megasonics nozzle hardware that adds a physical component to the cleaning process, enhancing the dissolution rate of the mask.

- 5 In another aspect, Figures 6A-6C illustrate cross-sectional views representing various operations a method of dicing a semiconductor wafer, in accordance with an embodiment of the present disclosure.

Referring to Figure 6A, a mask 602 is formed above a semiconductor wafer or substrate 604. The mask 602 covers and protects integrated circuits 606 formed on the surface of

- 10 semiconductor wafer 604. The mask 602 also covers intervening streets 607 formed between each of the integrated circuits 606.

In an embodiment, the semiconductor wafer or substrate 604 is supported by a substrate carrier (such as a substrate carrier described in association with Figure 2B) during the forming of the mask 602. In an embodiment, forming the mask 602 above the semiconductor wafer 604

- 15 includes spin-coating the mask 602 on the semiconductor wafer 604. In a specific embodiment, prior to coating, a plasma or chemical pre-treatment is performed to enable better wettability and coating of the wafer.

In an embodiment, mask 602 is a water soluble mask in that it is readily dissolvable in an aqueous media. For example, in one embodiment, the as deposited water-soluble mask 602 is composed of a material that is soluble in one or more of an alkaline solution, an acidic solution, or in deionized water. In a specific embodiment, the as-deposited water-soluble mask 602 has an etch or removal rate in an aqueous solution approximately in the range of 1 – 15 microns per minute. In one embodiment, mask 602 is a polyvinyl alcohol (PVA)-based water soluble mask.

- 20 In an embodiment, semiconductor wafer or substrate 604 is composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably be disposed. For example, in one embodiment, semiconductor wafer or substrate 604 is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing semiconductor wafer 604 includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, semiconductor wafer or substrate 604 is composed of a III-V material such as, e.g., a III-V material substrate used in the fabrication of light emitting diodes (LEDs).

- 25 In an embodiment, semiconductor wafer or substrate 604 has disposed thereon or therein, as a portion of the integrated circuits 606, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-
- 35

oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits 606. Materials making up the streets 607
5 may be similar to or the same as those materials used to form the integrated circuits 606. For example, streets 607 may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the streets 607 includes test devices similar to the actual devices of the integrated circuits 606.

In an optional embodiment, the mask 602 is baked prior to laser patterning of the mask. In an
10 embodiment, the mask 602 is baked to increase the etch resistance of the mask 602. In a specific embodiment, the mask 602 is baked at a relatively high temperature approximately in the range of 50 to 130 degrees Celsius. Such higher temperature baking may cause crosslink of the mask 602 so as to significantly increase etch resistance. In one embodiment, baking is performed using a hot plate technique or a heat (light) radiation applied from the wafer front side (e.g., non-
15 tape mounted side in the case of the use of a substrate carrier) or other suitable techniques.

Referring to Figure 6B, the mask 602 is patterned with a laser scribing process to provide patterned mask 608 with gaps 610, exposing regions of the semiconductor wafer or substrate 604 between the integrated circuits 606. As such, the laser scribing process is used to remove the material of the streets 607 originally formed between the integrated circuits 606. In accordance
20 with an embodiment of the present disclosure, patterning the mask 602 with the laser scribing process further includes forming trenches 612 partially into the regions of the semiconductor wafer 604 between the integrated circuits 606, as is also depicted in Figure 6B. In an embodiment, the semiconductor wafer or substrate 604 is supported by a substrate carrier (such as a substrate carrier described in association with Figure 2B) during the laser scribing process.

In an embodiment, the mask 602 is patterned with a Gaussian laser beam, however, non-Gaussian beams may also be used. Additionally, the beam may be stationary or rotating. In an embodiment, a femtosecond-based laser is used as a source for a laser scribing process. For example, in an embodiment, a laser with a wavelength in the visible spectrum plus the ultra-violet (UV) and infra-red (IR) ranges (totaling a broadband optical spectrum) is used to provide a
30 femtosecond-based laser, i.e., a laser with a pulse width on the order of the femtosecond (10^{-15} seconds). In one embodiment, ablation is not, or is essentially not, wavelength dependent and is thus suitable for complex films such as films of the mask 602, the streets 607 and, possibly, a portion of the semiconductor wafer or substrate 604.

It is to be appreciated that by using a laser beam profile with contributions from the femtosecond
35 range, heat damage issues are mitigated or eliminated versus longer pulse widths (e.g.,

nanosecond processing). The elimination or mitigation of damage during laser scribing may be due to a lack of low energy recoupling or thermal equilibrium. It is also to be appreciated that laser parameter selection, such as beam profile, may be critical to developing a successful laser scribing and dicing process that minimizes chipping, microcracks and delamination in order to achieve clean laser scribe cuts. The cleaner the laser scribe cut, the smoother an etch process that may be performed for ultimate die singulation. In semiconductor device wafers, many functional layers of different material types (e.g., conductors, insulators, semiconductors) and thicknesses are typically disposed thereon. Such materials may include, but are not limited to, organic materials such as polymers, metals, or inorganic dielectrics such as silicon dioxide and silicon nitride.

A street between individual integrated circuits disposed on a wafer or substrate may include the similar or same layers as the integrated circuits themselves. For example, Figure 7 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present disclosure.

Referring to Figure 7, a street region 700 includes the top portion 702 of a silicon substrate, a first silicon dioxide layer 704, a first etch stop layer 706, a first low K dielectric layer 708 (e.g., having a dielectric constant of less than the dielectric constant of 4.0 for silicon dioxide), a second etch stop layer 710, a second low K dielectric layer 712, a third etch stop layer 714, an undoped silica glass (USG) layer 716, a second silicon dioxide layer 718, and a scribing and/or etch mask 720 (such as a mask described above in association with mask 602). Copper metallization 722 is disposed between the first and third etch stop layers 706 and 714 and through the second etch stop layer 710. In a specific embodiment, the first, second and third etch stop layers 706, 710 and 714 are composed of silicon nitride, while low K dielectric layers 708 and 712 are composed of a carbon-doped silicon oxide material.

Under conventional laser irradiation (such as nanosecond-based irradiation), the materials of street 700 behave quite differently in terms of optical absorption and ablation mechanisms. For example, dielectrics layers such as silicon dioxide, is essentially transparent to all commercially available laser wavelengths under normal conditions. By contrast, metals, organics (e.g., low K materials) and silicon can couple photons very easily, particularly in response to nanosecond-based irradiation. In an embodiment, a femto-second based laser scribing process is used to pattern a layer of silicon dioxide, a layer of low K material, and a layer of copper by ablating the layer of silicon dioxide prior to ablating the layer of low K material and the layer of copper. In case that the laser beam it is a femtosecond-based laser beam, in an embodiment, suitable femtosecond-based laser processes are characterized by a high peak intensity (irradiance) that usually leads to nonlinear interactions in various materials. In one such embodiment, the

femtosecond laser sources have a pulse width approximately in the range of 10 femtoseconds to 500 femtoseconds, although preferably in the range of 100 femtoseconds to 400 femtoseconds. In one embodiment, the femtosecond laser sources have a wavelength approximately in the range of 1570 nanometers to 200 nanometers, although preferably in the range of 540 nanometers to 250 nanometers. In one embodiment, the laser and corresponding optical system provide a focal spot at the work surface approximately in the range of 3 microns to 15 microns, though preferably approximately in the range of 5 microns to 10 microns or between 10 – 15 microns. In an embodiment, the laser source has a pulse repetition rate approximately in the range of 200 kHz to 10 MHz, although preferably approximately in the range of 500kHz to 5MHz. In an embodiment, the laser source delivers pulse energy at the work surface approximately in the range of 0.5 uJ to 100 uJ, although preferably approximately in the range of 1uJ to 5uJ. In an embodiment, the laser scribing process runs along a work piece surface at a speed approximately in the range of 500mm/sec to 5m/sec, although preferably approximately in the range of 600mm/sec to 2m/sec.

The scribing process may be run in single pass only, or in multiple passes, but, in an embodiment, preferably 1-2 passes. In one embodiment, the scribing depth in the work piece is approximately in the range of 5 microns to 50 microns deep, preferably approximately in the range of 10 microns to 20 microns deep. In an embodiment, the kerf width of the laser beam generated is approximately in the range of 2 microns to 15 microns, although in silicon wafer scribing/dicing preferably approximately in the range of 6 microns to 10 microns, measured at the device/silicon interface.

Laser parameters may be selected with benefits and advantages such as providing sufficiently high laser intensity to achieve ionization of inorganic dielectrics (e.g., silicon dioxide) and to minimize delamination and chipping caused by underlayer damage prior to direct ablation of inorganic dielectrics. Also, parameters may be selected to provide meaningful process throughput for industrial applications with precisely controlled ablation width (e.g., kerf width) and depth.

In an optional embodiment, subsequent to the laser scribing process and prior to a plasma etching singulation process, an intermediate post mask-opening cleaning operation is performed. In an embodiment, the post mask-opening cleaning operation is a plasma-based cleaning process. In an example, as described below, the plasma-based cleaning process is non-reactive to the trenches 612 of the substrate 604 exposed by the gaps 610.

In accordance with one embodiment, the plasma-based cleaning process is non-reactive to exposed regions of the substrate 604 in that the exposed regions are not or only negligible etched during the cleaning process. In one such embodiment, only non-reactive gas plasma cleaning is

used. For example, Ar or another non-reactive gas (or the mix) is used to perform a highly-biased plasma treatment both for mask condensation and cleaning of scribed openings. The approach may be suitable for water-soluble masks such as mask 602. In another such embodiment, separate mask condensation (densification of the surface layer) and scribed trench cleaning operations are used, e.g., an Ar or non-reactive gas (or the mix) highly-biased plasma treatment for mask condensation is first performed, and then an Ar + SF₆ plasma cleaning of a laser scribed trench is performed. This embodiment may be suitable for cases where Ar-cleaning is not sufficient for trench cleaning due to too thick of a mask material. In this case, metal salts of the mask may provide etch resistance during a plasma cleaning operation including SF₆.

Referring to Figure 6C, the semiconductor wafer 604 is etched through the gaps 610 in the patterned mask 608 to singulate the integrated circuits 606. In accordance with an embodiment of the present disclosure, etching the semiconductor wafer 604 includes ultimately etching entirely through semiconductor wafer 604, as depicted in Figure 6C, by etching the trenches 612 initially formed with the laser scribing process. The patterned mask 608 protects the integrated circuits during the plasma etching.

In an embodiment, the semiconductor wafer or substrate 602 is supported by a substrate carrier (such as a substrate carrier described in association with Figure 2B) during the plasma etching process. In one such embodiment, the substrate carrier is supported by an electrostatic chuck having a conductive pedestal having a plurality of notches at a circumferential edge thereof, as described above in association with Figures 3A-3C. In one such embodiment, the conductive pedestal and surfaces of the plurality of notches are coated with a ceramic material, and the ceramic material prevents current from leaking from the electrostatic chuck during the etching. In an embodiment, patterning the mask 602 with the laser scribing process involves forming trenches in the regions of the semiconductor wafer between the integrated circuits, and plasma etching the semiconductor wafer involves extending the trenches to form corresponding trench extensions. In one such embodiment, each of the trenches has a width, and each of the corresponding trench extensions has the width.

In an embodiment, etching the semiconductor wafer 604 includes using a plasma etching process. In one embodiment, a through-silicon via type etch process is used. For example, in a specific embodiment, the etch rate of the material of semiconductor wafer 604 is greater than 10 microns per minute. An ultra-high-density plasma source may be used for the plasma etching portion of the die singulation process. An example of a process chamber suitable to perform such a plasma etch process is the Applied Centura® Silvia™ Etch system available from Applied Materials of Sunnyvale, CA, USA. The Applied Centura® Silvia™ Etch system combines the capacitive and inductive RF coupling, which gives much more independent control

of the ion density and ion energy than was possible with the capacitive coupling only, even with the improvements provided by magnetic enhancement. This combination enables effective decoupling of the ion density from ion energy, so as to achieve relatively high density plasmas without the high, potentially damaging, DC bias levels, even at very low pressures. This results in an exceptionally wide process window. However, any plasma etch chamber capable of etching silicon may be used. In an exemplary embodiment, a deep silicon etch is used to etch a single crystalline silicon substrate or wafer 604 at an etch rate greater than approximately 40% of conventional silicon etch rates while maintaining essentially precise profile control and virtually scallop-free sidewalls. In a specific embodiment, a through-silicon via type etch process is used. The etch process is based on a plasma generated from a reactive gas, which generally a fluorine-based gas such as SF₆, C₄F₈, CHF₃, XeF₂, or any other reactant gas capable of etching silicon at a relatively fast etch rate. In another embodiment, the plasma etching operation described in association with Figure 6C employs a conventional Bosch-type dep/etch/dep process to etch through the substrate 604. Generally, a Bosch-type process consists of three sub-operations: deposition, a directional bombardment etch, and isotropic chemical etch which is run through many iterations (cycles) until silicon is etched through.

As mentioned above, in an embodiment, the semiconductor wafer or substrate 602 is supported by a substrate carrier (such as a substrate carrier described in association with Figure 2B) during the plasma etching process, and the substrate carrier is supported by an electrostatic chuck having a conductive pedestal having a plurality of notches at a circumferential edge thereof. In a particular such embodiment, subsequent to the etching, the substrate carrier is removed from the conductive pedestal using a plurality of lift pins corresponding to ones of the plurality of notches of the conductive pedestal.

In an embodiment, following the singulation process, the patterned mask 608 is removed. In an embodiment, the patterned mask 608 is a water soluble patterned mask. In an embodiment, the patterned mask 608 is removed using an aqueous solution. In one such embodiment, the patterned mask 608 is removed by a hot aqueous treatment, such as a hot water treatment. In a specific embodiment, the patterned mask 608 is removed in a hot water treatment at a temperature approximately in the range of 40 – 100 degrees Celsius. In a particular embodiment, the patterned mask 608 is removed in a hot water treatment at a temperature approximately in the range of 80 – 90 degrees Celsius. It is to be appreciated that the hotter the temperature of the water, the less time may be needed for the hot water treatment. In accordance with an embodiment of the present disclosure, a plasma cleaning process can also be performed after etching to aid in the removal of the patterned mask 608.

- It is to be appreciated that other circumstances may benefit from a lower water treatment temperature. For example, in the case that a wafer for dicing is supported on a dicing tape that may be impacted by a higher temperature water treatment (e.g., through loss of adhesion), a relatively lower water treatment temperature may be employed, albeit for a longer duration than a relatively higher water treatment temperature. In one such embodiment, the water treatment is between room temperature (i.e., the water is un-heated), but below a temperature of approximately 40 degrees Celsius. In a specific such embodiment, the patterned mask 608 is removed in a warm water treatment at a temperature approximately in the range of 35 – 40 degrees Celsius.
- Referring again to Figures 6A-6C, wafer dicing may be preformed by initial ablation to ablate through a mask, through wafer streets (including metallization), and partially into a silicon substrate. Die singulation may then be completed by subsequent through-silicon deep plasma etching. A specific example of a materials stack for dicing is described below in association with Figures 8A-8D, in accordance with an embodiment of the present disclosure.
- Referring to Figure 8A, a materials stack for hybrid laser ablation and plasma etch dicing includes a mask 802, a device layer 804, and a substrate 806. The mask layer 802, device layer 804, and substrate 806 are disposed above a die attach film 808 which is affixed to a backing tape 810. In other embodiments, direct coupling to a standard dicing tape is used. In an embodiment, the mask 802 is one such as described above in association with mask 602. The device layer 804 includes an inorganic dielectric layer (such as silicon dioxide) disposed above one or more metal layers (such as copper layers) and one or more low K dielectric layers (such as carbon-doped oxide layers). The device layer 804 also includes streets arranged between integrated circuits, the streets including the same or similar layers to the integrated circuits. The substrate 806 is a bulk single-crystalline silicon substrate. In an embodiment, the mask 802 is fabricated using a thermal treatment or bake 899, such as described above. In an embodiment, the mask 802 is a water mask.
- In an embodiment, the bulk single-crystalline silicon substrate 806 is thinned from the backside prior to being affixed to the die attach film 808. The thinning may be performed by a backside grind process. In one embodiment, the bulk single-crystalline silicon substrate 806 is thinned to a thickness approximately in the range of 30 - 200 microns. It is important to note that, in an embodiment, the thinning is performed prior to a laser ablation and plasma etch dicing process. In an embodiment, the mask 802 has a thickness approximately in the range of 3-100microns and the device layer 804 has a thickness approximately in the range of 2-20 microns. In an embodiment, the die attach film 808 (or any suitable substitute capable of bonding a thinned or

thin wafer or substrate to the backing tape 810, such as dicing tapes consisting of an upper adhesive layer and a base film) has a thickness approximately in the range of 10-200 microns. Referring to Figure 8B, the mask 802, the device layer 804 and a portion of the substrate 806 are patterned with a laser scribing process 812 to form trenches 814 in the substrate 806.

- 5 Referring to Figure 8C, a through-silicon deep plasma etch process 816 is used to extend the trench 814 down to the die attach film 808, exposing the top portion of the die attach film 808 and singulating the silicon substrate 806. The device layer 804 is protected by the mask 802 during the through-silicon deep plasma etch process 816.

- Referring to Figure 8D, the singulation process may further include patterning the die attach film 10 808, exposing the top portion of the backing tape 810 and singulating the die attach film 808. In an embodiment, the die attach film is singulated by a laser process or by an etch process. Further embodiments may include subsequently removing the singulated portions of substrate 806 (e.g., as individual integrated circuits) from the backing tape 810. In one embodiment, the singulated die attach film 808 is retained on the back sides of the singulated portions of substrate 806. In an 15 alternative embodiment, in the case that substrate 806 is thinner than approximately 50 microns, the laser scribing process 812 is used to completely singulate substrate 806 without the use of an additional plasma process. Embodiments may further include removing the mask 802 from the device layer 804. Removal of the mask 802 can be as described above for removal of the patterned mask 608.

- 20 Embodiments of the present disclosure may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present disclosure. In one embodiment, the computer system is coupled with process tool 500 described in association with Figure 5 or with etch chamber 400 25 described in association with Figure 4. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a 30 machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

- Figure 9 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 900 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein, may be executed. In alternative 35 embodiments, the machine may be connected (e.g., networked) to other machines in a Local

Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular
5 telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term “machine” shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described
10 herein.

The exemplary computer system 900 includes a processor 902, a main memory 904 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 906 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 918 (e.g., a
15 data storage device), which communicate with each other via a bus 930.

Processor 902 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 902 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor
20 implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 902 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 902 is configured to execute the processing logic 926 for performing the operations described herein.

25 The computer system 900 may further include a network interface device 908. The computer system 900 also may include a video display unit 910 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 912 (e.g., a keyboard), a cursor control device 914 (e.g., a mouse), and a signal generation device 916 (e.g., a speaker).

30 The secondary memory 918 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 932 on which is stored one or more sets of instructions (e.g., software 922) embodying any one or more of the methodologies or functions described herein. The software 922 may also reside, completely or at least partially, within the main memory 904 and/or within the processor 902 during execution thereof by the computer
35 system 900, the main memory 904 and the processor 902 also constituting machine-readable

storage media. The software 922 may further be transmitted or received over a network 920 via the network interface device 908.

While the machine-accessible storage medium 932 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be taken to include a single
5 medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present disclosure. The term “machine-readable storage medium”
10 shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

In accordance with an embodiment of the present disclosure, a machine-accessible storage medium has instructions stored thereon which cause a data processing system to perform a method of dicing a semiconductor wafer having a plurality of integrated circuits, such as one or
15 more of the methods described herein.

Thus, hybrid wafer dicing approaches using a laser scribing process and plasma etch process implementing a shadow ring kit have been disclosed.

CLAIMS

What is claimed is:

1. An etch apparatus, comprising
 - 5 a chamber;
 - a plasma source within or coupled to the chamber;
 - an electrostatic chuck within the chamber, the electrostatic chuck comprising a conductive pedestal to support a substrate carrier sized to support a wafer having a first diameter;
 - and
 - 10 a shadow ring assembly between the plasma source and the electrostatic chuck, the shadow ring assembly sized to process a wafer having a second diameter smaller than the first diameter.
2. The etch apparatus of claim 1, wherein the first diameter is approximately 300mm, and the
15 second diameter is approximately 200mm.
3. The etch apparatus of claim 1, wherein the shadow ring assembly comprises a heat shield, an insert ring, and a carrier.
- 20 4. The etch apparatus of claim 3, wherein the heat shield, the insert ring, and the carrier comprise solid alumina.
5. The etch apparatus of claim 3, wherein the heat shield comprises a pocket therein to accommodate the insert ring without contacting the insert ring.
25
6. The etch apparatus of claim 1, wherein the conductive pedestal has a plurality of holes there through, and the etch apparatus further comprises:
 - a plurality of lift pins corresponding to ones of the plurality of holes, the plurality of lift pins arranged for contacting the substrate carrier beneath the wafer.
30
7. The etch apparatus of claim 1, wherein the conductive pedestal has a plurality of notches at a circumferential edge thereof, and the etch apparatus further comprises:
 - a plurality of lift pins corresponding to ones of the plurality of notches, the plurality of lift pins arranged for contacting a frame of the substrate carrier.

8. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask comprising a layer covering and protecting the integrated circuits, and the semiconductor wafer supported by a substrate

5 carrier sized to support a wafer having a first diameter;

patterning the mask with a laser scribing process to provide a patterned mask with gaps exposing regions of the semiconductor wafer between the integrated circuits; and

10 etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits while the semiconductor wafer is supported by the substrate carrier and while the substrate carrier is partially covered by a shadow ring assembly sized to process the semiconductor wafer having a second diameter smaller than the first diameter.

9. The method of claim 8, wherein the shadow ring assembly comprises a heat shield, an insert ring, and a carrier, wherein the heat shield comprises a pocket therein to accommodate the insert
15 ring without contacting the insert ring to avoid thermal contact during the etching.

10. The method of claim 8, wherein the first diameter is approximately 300mm, and the second diameter is approximately 200mm.

20 11. A system for dicing a semiconductor wafer comprising a plurality of integrated circuits, the system comprising:

a factory interface;

a laser scribe apparatus coupled with the factory interface and comprising a laser; and

25 an etch apparatus coupled with the factory interface, the etch apparatus comprising a chamber, a plasma source within or coupled to the chamber, an electrostatic chuck within the chamber, the electrostatic chuck comprising a conductive pedestal to support a substrate carrier sized to support a wafer having a first diameter, and a shadow ring assembly between the plasma source and the electrostatic chuck, the shadow ring assembly sized to process a wafer having a second diameter smaller than the first diameter.

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12. The system of claim 11, wherein the first diameter is approximately 300mm, and the second diameter is approximately 200mm.

13. The system of claim 11, wherein the shadow ring assembly of the etch apparatus comprises a
35 heat shield, an insert ring, and a carrier.

14. The system of claim 13, wherein the heat shield, the insert ring, and the carrier comprise solid alumina.
15. The system of claim 13, wherein the heat shield comprises a pocket therein to accommodate
5 the insert ring without contacting the insert ring.
16. The system of claim 13, wherein the insert ring has an inner opening with a diameter of about 197 mm.
- 10 17. The system of claim 11, wherein the laser scribe apparatus is configured to perform laser ablation of streets between integrated circuits of a semiconductor wafer, and wherein the etch apparatus is configured to etch the semiconductor wafer to singulate the integrated circuits subsequent to the laser ablation.
- 15 18. The system of claim 11, wherein the etch apparatus is housed on a cluster tool coupled with the factory interface, the cluster tool further comprising:
a deposition chamber configured to form a mask layer above the integrated circuits of the semiconductor wafer.
- 20 19. The system of claim 11, wherein the etch apparatus is housed on a cluster tool coupled with the factory interface, the cluster tool further comprising:
a wet/dry station configured to clean the semiconductor wafer subsequent to the laser ablation or the etching.
- 25 20. The system of claim 11, wherein the laser scribe apparatus comprises a femtosecond-based laser.