FULLY SALICIDED (FUSA) MOSFET STRUCTURE

ABSTRACT

A method is described to form a MOSFET with a fully silicided gate electrode and fully silicided, raised S/D elements that are nearly coplanar to allow a wider process margin when forming contacts to silicided regions. An insulator block layer is formed over STI regions and a conformal silicidation stop layer such as Ti/TiN is disposed on the insulator block layer and active region. A polysilicon layer is deposited on the silicidation stop layer and is planarized by a CMP process to form raised S/D elements. An oxide hardmask on the gate electrode is removed to produce a slight recess between the spacers. A silicidation process yields a gate electrode and raised S/D elements comprised of NiSi. Optionally, a recess is formed in the substrate between an insulator block mask and spacer and a Schottky barrier is used instead of a silicidation stop layer to form a Schottky Barrier MOSFET.

Fig. 7