Assorted Aluminum Wiring Design to Enhance Chip-Level Performance for Deep Sub-Micron Application

Abstract

A method of manufacturing conductive lines that are thicker (not wider) in the critical paths areas. We form a plurality of first level conductive lines over a first dielectric layer. The first conductive lines run in a first direction. The first level conductive lines are comprised of a first level first conductive line and a second first level conductive line. We form a second dielectric layer over the first level conductive lines and the first dielectric layer. Next, we form a via opening in the second dielectric layer over a portion of the first level first conductive line. A plug is formed filling the via opening. We form a trench pattern in the second dielectric layer. The trench pattern is comprised of trenches that are approximately orthogonal to the first level conductive lines. We fill the trenches with a conductive material to form supplemental second lines. We form second level conductive lines over the supplemental second lines and the plug. The second level conductive lines are aligned parallel to the supplemental second lines. The supplemental second lines are formed under the critical path areas of the second level conductive lines. The second level conductive lines are not formed to contact the first level conductive lines where a contact is not desired. In the critical path areas of the second level conductive lines, the supplemental second lines underlie the second level conductive lines thereby increasing the effective overall wiring thickness in the critical path area thereby improving performance.

Fig 5A